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Samuel Vasconcelos Araújo

On the Perspectives of Wide-Band Gap Power Devices in Electronic-Based Power Conversion for Renewable Systems

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Foreword

Power electronics is taking an increasingly important role in our daily lives, as it is the keystone not only to the efficient, but also cost effective and reliable use of electric energy in all possible fields of application; ranging from power supply from renewable energy sources to industry, IT and transportation. The first revolution in this field of technology came in the 1960s with the viability of switched-mode power conversion, owning to the emergence of BJTs operating at higher speeds. The development of MOSFETs and later IGBTs provided a further step in the direction towards higher frequency and power levels.

The advent of power devices based on silicon carbide (SiC) and gallium nitride (GaN) is currently pointing in the direction of a second revolution, where several paradigms concerning the design and performance of power conversion stages will be broken. Such giant leap will nevertheless require, aside from improvements in the chip technology itself, significant developments in device packaging, driving and also on the available materials and design strategies for passive filter elements. This work addresses some of these issues; presenting an overview of device structures, benchmarking and finally discussing issues at application level, with focus on converters for renewable energy sources.

This long path towards my thesis started back with my very first activities in the field of Power Electronics in 2005 in Brazil, as I was a graduation student in the Federal University of Ceará (UFC), working in the GPEC Laboratory. There I met my first mentors, Professor Sérgio Daher and Professor René Bascopé, and also other colleagues like Professor Carlos Gustavo Castelo Branco that gave me an outstanding support in my first steps. Professor Fernando Antunes not only supervised my graduation work, but also supported my scholarship for an exchange program that sent me to Kassel in 2004.

In Kassel, the great colleague Benjamin Sahan supervised my Master Thesis and also supported my application for a position in the former "Institut für Solare Energieversorgungstechnik" (ISET e.V.), now part from Fraunhofer IWES. There I had my first contact with the SiC technology in the beginning of 2008, while working with the colleagues Arno Zimpfer and Thorsten Bülo. Within two very exciting (and also exhausting) weeks, we tested samples from the manufacturer CREE in a prototype three-phase inverter under development for the company SMA Solar Technology AG. Aside from obtaining the "holy grail" (efficiency

record), I myself could still not grasp all the potentials of that new technology at that time.

With the establishment of the Centre of Competence for Distributed Electric Power Technology (KDEE) by Professor Peter Zacharias, I moved to the Department of Electric Power Supply Systems (EVS) in University of Kassel in 2009. Besides the important support not only from the department employees but also from the coworkers Benjamin Sahan and Mehmet Kazanbas, I could meet other outstanding colleagues that always helped me in the path of my work, like Christian Nöding, Lucas Menezes and Thiemo Kleeb.

On the other hand, the continuing cooperation with experienced engineers from SMA like Matthias Viktor, Henrik Wolf, Andreas Falk, Klaus Rigbers and Regine Mallwitz offered me a broad overview of trends and requirements in the field of photovoltaic power converters. In 2010 I could finally focus again on SiC devices thanks to a Joint Research Program funded by the European Center for Power Electronics e.V. (ECPE), where most of the literature research and device benchmarking could be performed.

During this project and also in the ensuing years, I could also count with the increasing support from several engineers in the companies Infineon Technologies AG (Peter Friedrichs, Gerald Deboy, Roland Rupp), CREE Inc. (John Palmour, Robert Callanan, Michael O'Neill), Semisouth Labs (Dieter Liesabeths, Nigel Springett) and Transic (Anders Lindgren).

The most important support came surely from Professor Peter Zacharias, who not only supervised my research activities throughout these years but was also an infinite source of interesting discussions and ideas. In my eyes it has been a unique privilege to interact with such a genius mind. I would also like to acknowledge my second supervisor, Professor Andreas Lindemann, for the interest and detailed revision of my work and also to Professor Axel Bangert and Professor Ludwig Brabetz for taking part in the examination board.

All these and many other persons helped me pave the way towards concluding my work. But without two "strong legs" I would not have been able to reach this goal. Such legs I owe to my parents, with their total dedication to my formation and also unconditional support towards my life goals, even it meant leaving my homeland.

Above all, I would like to thank God for giving me the aptitude, health and strength to pursue my dreams.

Kassel, April 24th 2013 *Samuel Vasconcelos Araújo*

Summary

Although being known for more than a century, the application of wide band gap (WBG) materials have only recently gained momentum in the field of power electronics, driven by the increasing interest towards their outstanding material characteristics. The most important among then is the high breakdown field. This allows the construction of unipolar devices with very low specific chip resistance mainly characterized by very low conduction and switching losses, even at high blocking voltages.

A multitude of switch technologies based on Silicon-Carbite (SiC) and Gallium-Nitride (GaN) is currently being commercially introduced by manufactures around the globe. The concepts are ranging from traditional FET structures driven by a MOS interface or a PN-Junction, bipolar devices and even high-electron mobility transistors (HEMT). A detailed revision of the scientific literature will be performed in this work with the objective of providing a broad overview of possible approaches, along with inherent advantages and limitations. In addition to this, a benchmarking of several WBG-based devices technologies rated for 1200V and 1700V will be performed against their state-of-the-art Silicon-counterparts (Si).

Concerning the application of wide band gap devices, renewable energy systems are indeed one of the most promising fields given their high performance requirements, fast market expansion and high level of technical innovation. A significant cost reduction potential is for instance enabled by WBG devices due to smaller expenditure with magnetic filters and cooling, alongside higher efficiency levels. These aspects will be discussed in details in order to identify constraints and bottlenecks at application level with special focus on photovoltaic and wind power systems.

Zusammenfassung

"Wide Band Gap“ (WBG) Materialen sind, wie der Name bereits sagt, Halbleiterelemente mit einer höheren Energie der Bandlücke im Vergleich zum Silizium. Bereits seit mehr als einem Jahrhundert bekannt, erhält der Einsatz dieser Materialien jedoch erst seit Kurzem stärkere Beachtung. Dies liegt vor allem an zahlreichen Entwicklungen im Bereich der Materialverarbeitung, die eine deutliche Verbesserung der Materialqualität durch geringere Defektdichte ermöglicht haben.

WBG Materialien - Eigenschaften und deren Applikation

Für die Leistungselektronik weisen Silizium Karbid (SiC) und Gallium Nitrid (GaN) hervorragenden Eigenschaften auf. Vor allem die erhöhte Durchschlagfestigkeit dieser Materialien ist zukunftsweisen, da hiermit eine Sperrfähigkeit nicht nur mit geringerem Materialeinsatz (kürzere Driftregion), sondern auch mit erhöhten Dotierungssätzen möglich ist. Somit ist der Aufbau von unipolaren und hochsperrenden Bauelementen mit stark reduzierten spezifischen Chipwiderständen möglich.

Ferner ist die Konzentration von intrinsischen Ladungsträgern bei ähnlichen Temperaturwerten um mehrere Größenordnungen geringer als Silizium. Folglich sind Betriebstemperaturen im Bereich von 600°C möglich. Eine weitere Eigenschaft stellt die Wärmeleitfähigkeit dar, welche bei SiC fast genauso gut ist wie bei Kupfer. Nicht zuletzt ist durch die erhöhte Driftgeschwindigkeit der Elektronen der Betrieb bei Funkfrequenzen möglich.

WBG-basierende Bauelemente

Bipolare Strukturen basierend auf Silizium dominieren derzeit die Anwendungen mit Sperrspannungen über 1000V. Ein Beispiel hiervon ist der Einsatz von IGBTs und PiN Dioden sowohl in Antriebsumrichtern der Industrie und dem Verkehr, als auch in der Photovoltaik und Windkraftanlagen.

Im Vergleich hierzu bietet Siliziumkarbit die Möglichkeit, unipolare Strukturen, wie MOSFETs und Schottky-Dioden, mit nur einem Bruchteil des Chipwiderstands aufzubauen. Solche Strukturen sind nicht von der Rekombinationszeit und Durchflutung von Majoritätsladungsträger wie bipolare Bauelemente betroffen. Daher ist eine deutlich bessere dynamische Performance

erreichbar. Bei höheren Spannungen sind zudem weitere bipolare Strukturen auf SiC-Basis, wie BJTs, Thyristor und PiN Diode, einsetzbar.

Im Gegensatz zum SiC sind für GaN weniger unterschiedliche Strukturen vorhanden. Ein erster Grund dafür ist das Fehlen eines nativen Oxids, wie SiO_2. Daher können MOSFETs und IGBTs nur mit erhöhtem Aufwand hergestellt werden. Weiterhin sind P-dotierte Bereiche von geringerer Löcherbeweglichkeit betroffen und die Dotierungskonzentration von N-Bereichen ist begrenzt. Nicht zuletzt ist in der Regel ein leitender Kanal auf Basis von AlN durch die Epitaxie aufgebaut, sodass der Stromfluss in horizontaler Richtung erfolgen muss. Folglich kommen hier nur laterale Strukturen wie der "High-electron mobility"-Transistor (HEMT) in Frage. Aufgrund der oben erwähnten Einschränkungen ist der Einsatz von GaN-Bauelemente eher in geringeren Spannungsklassen geeignet.

Eine detaillierte Übersicht aus der Fachliteratur wird in dieser Arbeit zusammen mit der Identifizierung von inhärenten Vorteilen und Einschränkungen der einzelnen Ausführungsmöglichkeiten vorgestellt. Ein Benchmarking ausgewählter Bauteile wird schließlich auf Basis experimenteller Ergebnisse gegenüber dem Stand der Technik von Silizium-Bauelementen durchgeführt.

Applikation von WBG-basierenden Bauelementen

Mit den zuvor erwähnten Eigenschaften von WBG Bauelementen sind zukunftsweisende Bauteile für die Leistungselektronik erreichbar. Die Senkung der Verluste, Erhöhung der Schaltfrequenz und Betrieb bei höheren Junction-Temperaturen seien lediglich mögliche Beispiele. Hinsichtlich der Anwendung solcher Bauelemente sind erneuerbare Energien in der Tat die vielversprechendsten Gebiete, besonders aufgrund ihrer hohen Leistungsanforderungen, schneller Marktexpansion und des hohen technischen Innovationsgrades.

Auf Applikationsniveau hat die Erhöhung der Schaltfrequenz eine Reduzierung von passiven Filterelementen direkt als Folge. Mit den aktuell vorhandenen SiC Schaltern ist eine Reduzierung der Schaltenergie um bis zu 75% gegenüber der neusten Si-IGBTs möglich. Als Folge ist eine Vervierfachung der Schaltfrequenz erreichbar. Eine weitere Senkung um 50% bietet sich durch eine Erhöhung der Schaltflanken, wobei Aspekte wie die Isolationsfestigkeit, Oszillationen und EM-Störungen zunehmend kritisch werden. Die tatsächliche Senkung des Bauvolumens der Filterelemente ist dennoch stark von den Eigenschaften der Kernmaterialen beeinflusst. Heutige Materialien für den Einsatz bei 16kHz sind z.B. für den Betrieb oberhalb 50kHz nicht geeignet. Folglich sind die weitere Entwicklung und der Einsatz von hochwertigen Kernmaterialen erforderlich. Eine Übersicht über vorhandenen Materialen und deren Anwendungsbereiche werden in Rahmen dieser Arbeit analysiert und vorgestellt. Eine weitere untersuchte Alternative zur

Einsparung von Filterelemente ist der Betrieb mit höherer Stromwelligkeit, da gleichzeitig eine Senkung der gesamten Schaltverluste möglich ist. Dies lässt sich durch die Tatsache erklären, dass die Einschaltverluste eindeutig höher als die Ausschaltverluste sind.

Einsparungen im Bereich der Kühlung können durch zwei unterschiedliche Strategien erreicht werden. Zunächst können die WBG Bauelemente bei deutlich höheren Junction-Temperaturen betrieben werden. Wegen der Erhöhung der Durchlassverluste mit zunehmender Temperatur ist aber zu erkennen, dass eine optimale Chipausnutzung, d.h. maximale Strombelastbarkeit, eher unter 250°C liegt. Interessanter ist daher die Senkung der Verluste, die durch die geringere Chipfläche natürlich erreichbar ist.

Wegen der noch hohen Materialkosten spielt der geringere Aufwand bei der Chipfläche eine wesentliche Rolle in der Wettbewerbsfähigkeit von WBG Bauelemente. Einsparungen von über 50% sind dank des geringeren spezifischen Chipwiderstandes möglich. Weitere Einsparung können nicht nur durch Verbesserung der Wärmespreizung im Betrieb bei höherer Verlustdichte, sondern auch mit einer weiteren Erhöhung der Flankensteilheit beim Schalten und folglich durch geringere Schaltenergie erreicht werden.

Mögliche Einsparungen in Umrichter für erneuerbaren Energien

WBG-Bauelemente ermöglichen ein signifikantes Kostensenkungspotenzial durch geringeren Aufwand bei magnetischen Filtern und Kühlung, sowie höheren Wirkungsgraden. Es lässt sich dadurch eine klare Entwicklung in Richtung einer höheren Leistungsdichte zeigen.

Durch die Analyse der Kostenstruktur von Umrichter für Photovoltaik und Windkraftanlagen und unter Berücksichtigung der oben erwähnten Einsparpotenziale sind zwei Szenarien untersucht worden: die Erhöhung der Nennleistung bei gleicher Baugröße, sowie die Senkung der Baugröße bei fester Nennleistung. Die erste Methode ist für modulare Systeme wie Photovoltaik besser geeignet.

Allgemein ist zu erkennen, dass die höheren spezifischen Kosten von WBG-Materialen immer noch eine überwiegende Rolle in den Einsparungspotenzialen spielen. Zum Beispiel erhöhen sich mit zunehmenden Schaltfrequenzen auch der Aufwand in Bezug auf die Chipfläche. Daher sind höhere Schaltfrequenzen unter aktuellen Bedingungen nur sehr begrenzt attraktiv. Nur wenn die Chipfläche-Kosten von WBG-Materialen um einen Faktor 5 gegenüber denen von Si größer werden können, sind Kosteneinsparungen von 5% bis 10% zu erwarten.

Zusätzliche Einsparungen können dann nicht nur durch geringere Halbleitermaterialkosten, sondern auch durch eine verbesserte Ausnutzung der WBG Technologie erzielt werden. Dafür sind weitere Entwicklungen im Bereich Aufbau- und Verbindungstechnik (AVT) dringend erforderlich, um z.B. eine Erhöhung der Verlustdichte und Schaltsteilheit zu verwirklichen.

Experimenteller Einsatz von WBG Bauelemente

Alle experimentellen Untersuchungen in dieser Arbeit fokussieren lediglich auf SiC Bauelementen, da zum Zeitpunkt der Arbeit keine GaN-Halbleiter mit geeigneten Sperrspannungen vorhanden und lieferbar waren. Mit verschiedenen getesteten Schaltungen und Bauelementen war zunächst zu erkennen, dass es bereits mit der Kombination von neusten Si-Schalter und SiC-Dioden sehr hohe Wirkungsgrade erreichbar sind. Es besteht also wenig Raum zur Verbesserungen in diesem Aspekt.

Eine sehr interessante Aussicht besteht darin, die Betriebsspannungen von Hochleistungsumrichter zu erhöhen, um hierdurch Einsparungen auf Systemebene zu erreichen. Besonders große PV-Anlagen sind hiervon betroffen. Bei solchen Bedingungen bieten SiC-Hochspannungsbauelemente einen klaren Vorteil gegenüber der Si-Technologie, insbesondere in Bezug auf die Schaltperformance.

Schlussendlich ist auch zu erkennen, dass derzeit noch keine Aussage möglich ist, welche Schalterstruktur den Markt zeitnah dominieren wird. Grund dafür sind die sehr unterschiedlichen Eigenschaften der untersuchten Bauelemente, welche eine Palette von Steuerungsanforderungen (Selbstleitend, Strom- und Spannungsgesteuert) und Zuverlässigkeitsmerkmale (Gate-Oxid Lebensdauer, bipolare Degradation) aufweisen.

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1 Introduction

Band gap is defined as the amount of energy (normally measured in eV, corresponding to 1,6 x 10^{-19}J) required to move one electron from the valence to the conduction band, being a key property for drawing the boundaries between conductors, semiconductors and insulators. The so-called wide band-gap (WBG) semiconductors have band gap values higher than Silicon (Si), with Silicon Carbide (SiC) and Gallium Nitride (GaN) being the most significant materials in the field of electronics. Some of the most interesting properties of these materials are normalized against Si and presented in the graph below with logarithmic scale, followed by a brief explanation in the following table.

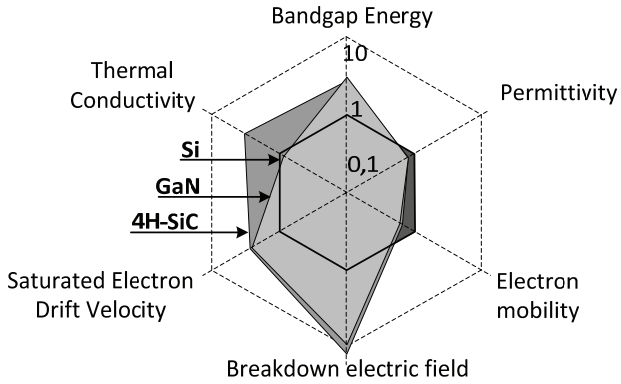


Fig. 1: Key-features of semiconductor materials normalized to the values of Si on a logarithmic scale.

From the below listed properties, it is possible to identify two main general prospects regarding the performance of WBG-based devices, as explained in the following items.

Table 1 – Explanation and technical potential of selected material properties.

Property [unit]	**Explanation**	**Technical importance**
Critical electric field (E_{crit}) [V/m]	Maximum electrical field intensity before the onset of avalanche breakdown	Higher critical field capability allows simultaneously shorter drift widths and higher doping concentrations, thus reducing device resistance
Relative permittivity (ε_r)	Permittivity to electrical field	Factor necessary for determining the applicable doping concentration of drift regions given a certain field limit and layer width
Electron mobility (μ_n) [m^2/Vs]	Relation between the electron speed and applied electrical field. Strongly affected by temperature and doping concentration	Directly affecting the resistivity of a given semiconductor area
Electron saturated drift velocity (v_{sat}) [m/s]	Maximum electron speed for an upper limit of electrical field	Affecting the semiconductor device maximum limit of speed of response and frequency, fundamental for RF/microwave applications
Thermal conductivity (λ) [W/m·K]	Heat conduction capability	Higher power dissipation capability per chip area, reduction of chip size, increase of power density.
Intrinsic carrier concentration (n_i) [cm^{-3}]	Volumetric concentration of free inherent carriers, at 300K. Strongly affected by temperature.	Directly related to high temperature operation capability due to lower leakage current.

- Low losses at high blocking voltages

The most notable characteristic of WBG materials is the very high critical field strength (E_{crit}); more than 10 times the value of silicon. As a consequence, the width of the drift-layer (w_{drift}) can be reduced by a similar order of magnitude for comparable values of breakdown voltages (V_{br}), as deduced by the equation below.

$$V_{br} = 0.5 \cdot w_{drift} \cdot E_{crit} \quad (1)$$

At the same time, the doping concentration (N_D) can be increased approximately 100 times under the above cited conditions. Such relation can be indirectly asserted with the equation below, with q being the electron charge.

$$q \cdot N_D = \varepsilon_o \cdot \varepsilon_r \cdot E_{crit} / w_{drift} \quad (2)$$

For unipolar devices, the impact of such characteristic on theoretical specific on-state resistance (R_{on_sp}) can be evaluated by division between width of the drift-zone and respective conductivity. Such relation is demonstrated in the equation below, having as parameters the electron mobility (μ_n) and doping concentration (N_D).

$$R_{on\_sp} = w_{drift} / (q \cdot \mu_n \cdot N_D) \quad (3)$$

By rearranging the equation above with relations given in the Poisson equation, the dependence on breakdown voltage and material properties like relative permittivity (ε_r) is obtained below [69]. In reality, the exponent applied to the breakdown voltage is normally higher, reaching approximately 2,5 due to the doping dependence on the factors μ_n and E_{crit} [70]. Thus independent of the employed material, the relative dependence to the breakdown voltage is practically the same; the major difference lies on the absolute value achievable with each one of them.

$$R_{on\_spec} = \left(4 \cdot V_{br}^{\,2}\right) / \left(\varepsilon_o \cdot \varepsilon_r \cdot \mu_n \cdot E_{crit}^{\,3}\right) \quad (4)$$

The denominator of the equation above with the exclusion of the permittivity of vacuum is normally named the "Baliga figure of merit" (BFoM). Considering the material constants given in [71] the value of BFoM and hence the specific chip resistance deduced for unipolar devices based on SiC and GaN result in theory in values respectively 488 and 2414 lower than Si. Such relations are employed to trace the theoretical technology limit curves, as presented in Fig. 2.

Such low value of specific chip resistance can from one side be translated in a significant reduction of the required chip area for a given current rating, what would be extremely favorable for the economic viability of the devices with the

referred new materials. In addition to this it is possible to assert that on-state losses (conduction losses) under the consideration of similar values of specific loss limits will also be accordingly reduced, enabling higher levels of efficiency.

At least but not last, the possibility of building high voltage blocking devices without conductivity modulation offers the attractive possibility of increasing the switching speed and thus reducing the switching losses.

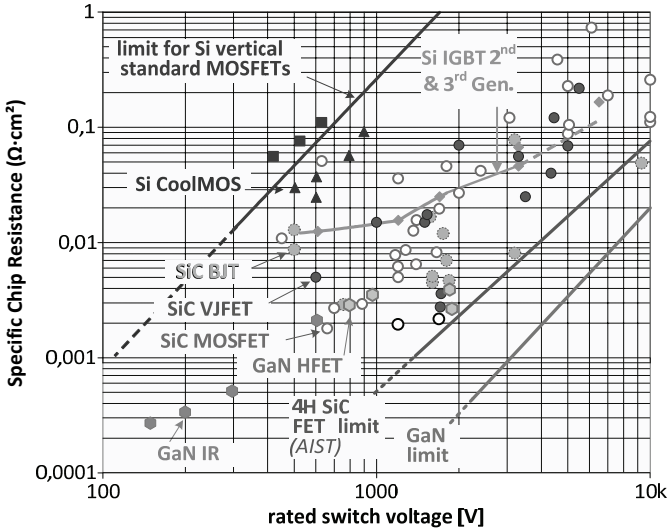


Fig. 2: Specific chip resistance as a function of the blocking voltage for different semiconductor materials and switch technologies.

- High temperature operation

The concentration of intrinsic carriers (n_i) and its exponential dependence on the temperature is a limiting factor for high junction temperature operation mainly due to two reasons. Firstly, in case the concentration of intrinsic carriers becomes larger than the one from the dopant carriers, incorrect operation of the device may occur. Secondly, the leakage current of a blocked junctions is practically exponentially dependant on the intrinsic carrier concentration, so that losses under blocking conditions become significant.

Given their superior bandgap energy, the concentration of intrinsic carriers in WBG materials is several orders of magnitude lower than Si, as can be observed in the graphic below. Hence, operational temperatures as high as 600°C are

achievable for WBG devices, while 200°C is often regarded as the limit for Si devices[72].

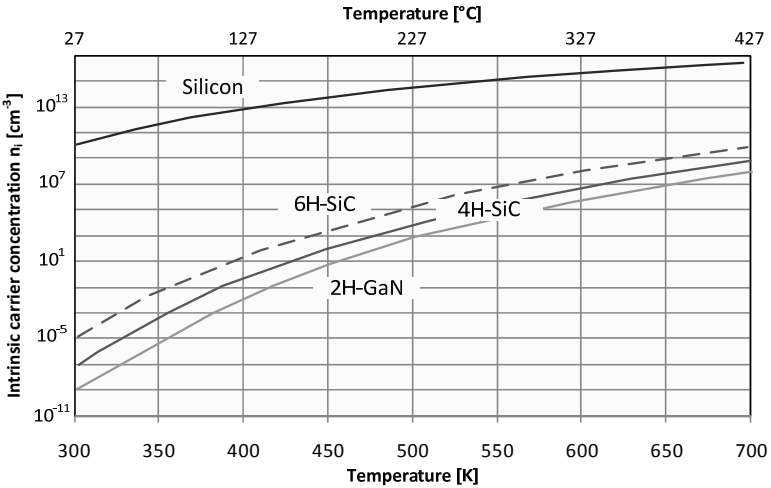


Fig. 3: Intrinsic carrier concentration depending on the temperature.

A higher limit for the maximum junction temperature has several technical advantages. Not only can the devices be applied under extreme harsh ambient conditions (military and space applications) but also the cooling expenditure can be significantly reduced. The overload capability along with loss density per chip is correspondently increased, leading to a possible reduction of the chip size. Exclusive to SiC is the superior thermal conductivity, which is almost as high as the one from cooper and more two times the value from Si and GaN.

1.1. Motivation of the work

Following several years of intensive research, 1200V-rated SiC switches have been newly introduced in the market, with some 1700V devices already available as engineering samples. Meanwhile, GaN devices are for the time being mostly limited to voltage levels below 600V. A multitude of publications have so far identified several outstanding properties of these devices, like the small chip area value with low equivalent resistance and very fast switching behavior.

In face of such diversity of possible alternatives, it is possible to observe in general the lack of a broad and unified overview of existing device technologies alongside a parametric experimental investigation of electrical properties. Without such result

results, it is practically impossible to perform a comparison and benchmarking of technologies in respect of their performance.

On the other hand, investigations at application level have so far relied on a simple exchange of existing devices and demonstration of possible increase of efficiency levels. Important aspects at application level like operation at higher switching speeds and related side-effects along with benchmarking of possible gains besides efficiency have also not been widely addressed.

In the path towards their extensive application, it is therefore necessary to fully understand not only the performance potentials but also limitations at both device and system levels. Due to their inherently higher specific costs, it also becomes mandatory to break some existing paradigms in the design and construction of power electronics systems, especially considering the possibility of operating with low losses even under high blocking voltages.

One of the most promising fields of application of these devices includes power conversion systems for renewable energy sources due to their fast growing rate and high level of technical innovations. They will offer a possible basis for the expansion of production capacity and technology maturation, before their introduction on broader market segments.

1.2. Structure of the work

In a first step, the key properties of existing switch technologies based on SiC and GaN will be presented. A new benchmarking methodology based on experimental results with SiC devices will afterwards be proposed and performed in Chapter 3 in order to identify the most attractive technologies.

The obtained results enable performing a link between the advantages of using WBG materials at device and application levels, as summarized in the picture below.

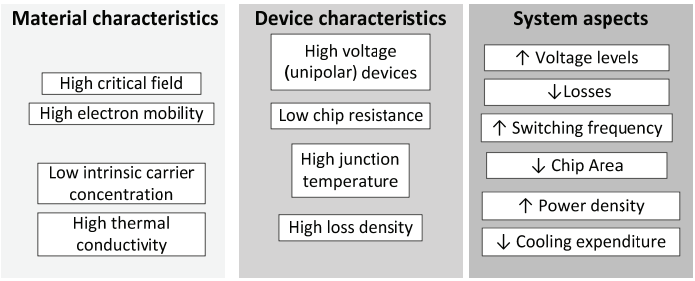


Fig. 4: System aspects abstraction from material and device characteristics.

In the Chapter 4, the drawbacks and limitations of high switching speed will be explored, along with considerations regarding the impact of higher switching frequencies in the design of magnetic filters. Chapter 5 will deal with thermal-related aspects like operation at high temperature and possible savings with cooling. In Chapter 6, the influence of the specific chip resistance value along with low switching energy on expected chip expenditure and losses will be analytically evaluated.

Later in chapter 7, a methodology for the assertion of gains due to the application of WBG devices will be proposed, with benchmarking of power converter specific costs assuming diverse device properties and cost scenarios. Different aspects of the system like cost distribution and original loss profile will also be taken in account in this analysis.

Finally, the chapter 8 will provide an overview of experimental results obtained with the application of SiC devices. Tests results with a multitude of power converters along with efficiency measurements and possible size reductions in the magnetics systems will be discussed, followed by some conclusions.

2 State-of-the-art power devices based on WBG

Below is presented an overview of possible constructive approaches regarding switches and diodes, giving an outline of some of the technologies that will be discussed in the details in the following chapters. As an important remark, focus will be given here only to devices for power conversion, excluding all approaches oriented to RF applications. Diodes are also out of the scope of the current investigation.

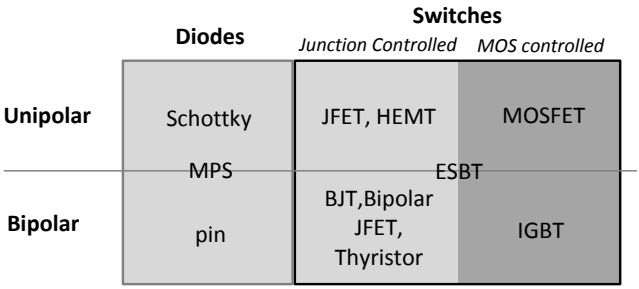


Fig. 5: Roadmap of main existing power devices depending on function and structure.

From the picture above it is possible to identify the two basic structures of semiconductor devices depending on carriers used during conduction. In the unipolar devices only majority carriers are available and hence their resistance is basically dependent on the drift region characteristics. Meanwhile in bipolar devices, minority carriers are injected during conduction, modulating the conductivity of the drift region and enabling low voltage drop under conduction even for high blocking voltages. In the case of switches, the control can be exerted either through a junction or through metal-oxide channel interfaces.

A possible distribution of the voltage classes and device structures is depicted below. Due to the referred reduction of the chip resistance, unipolar devices (in orange color) based on SiC may be employed up to 4kV (with examples in the literature up to 10kV).

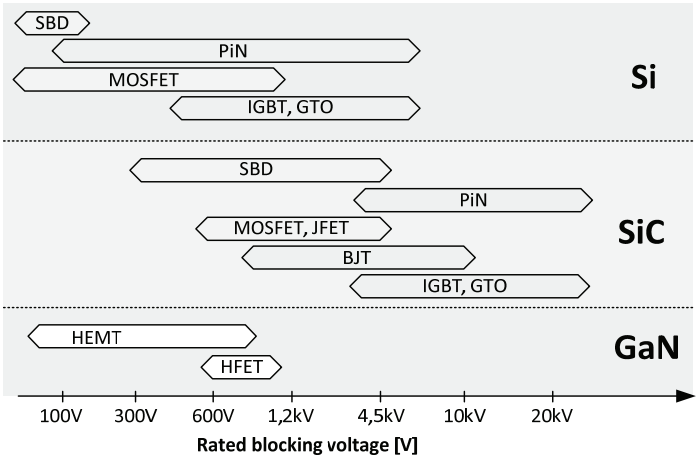


Fig. 6: Possible rated voltage classes for device structures from different semiconductor materials.

Details regarding the structure and operation of the most important SiC and GaN based switches will be presented in the following items. Of interest here is to identify not only specific issues but also requirements for reliable operation.

2.1. SiC-MOSFETs

MOS-driven switches are present nowadays in the majority of power conversion applications. Such popularity against other devices has been mainly justified by the simple and low-loss driving requirements along with robust and reliable operation. Regarding the Si-based technologies, MOSFETs are normally applied below 600V due to the very large chip resistance at higher voltage levels.

The use of SiC material allows a significant extension of the blocking voltage range, due to the massive reduction of the specific chip resistance. For instance, devices rated at 10kV attain similar values of specific chip resistance as their 600V Si-based counterparts. Several MOSFETs structures have been focus of investigations and will be presented in the next items, with a brief discussion of inherent characteristics and potentials.

Issues related to reliability and higher specific resistance against other SiC-designs remain the most significant drawbacks of this approach, as an overview of the latest related research results will be shortly presented.

2.1.1. Device structure and characteristics

A multitude of possible approaches can be found for MOSFET structures, as briefly explained in the following items. Below are depicted the most common structures [73].

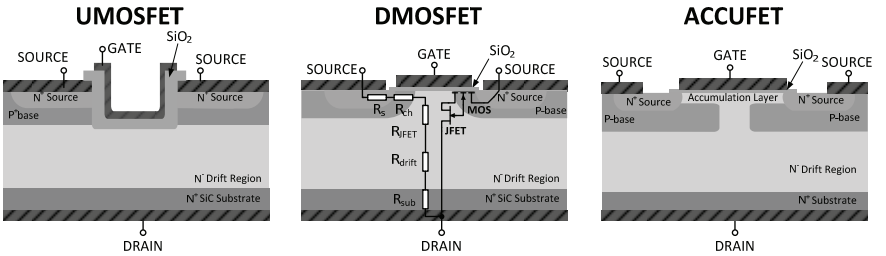


Fig. 7: Basic structures of SiC-MOSFETs.

- **UMOSFET**: Due to its relatively simple production steps without ion-implantation and high-temperature annealing steps, the UMOSFET was the first power MOSFET structure demonstrated with SiC in 1992 [74]. The UMOSFET allows a higher channel periphery density and also avoids the JFET resistance component, enabling lower resistance in devices rated below 3kV. A higher channel resistance is nevertheless obtained because the current flow takes place parallel to the vertical sidewall of the trench structure. This results in low inversion channel mobility because the current flows parallel to the c-axis of crystals and carriers and across alternate planes of Si and C through interface traps and charges. Another drawback is the high electrical field in the gate oxide near the edges of the trench corners; which has been one of the main reasons for the limitation of the blocking voltage in such structure. Possible structures dealing with such limitation added P-implants below the gate region with buffer layers to eliminate the JFET Effect.
- **DMOSFET**: This structure was employed as an alternative to deal with the electric-field crowding in the trench edges of the UMOSFET and is by far the most frequently found in the literature. The total chip resistance has in this case an additional component representing the region between the implanted P-wells, also called JFET component. Though increasing the distance between the wells reduces the referred resistance, it also increases the area of the device and reduces the effect of reducing the electrical field near the gate oxide under blocking conditions. Adding a highly-doped N-layer below the base implant leads to a better distribution

of the electron flow, reducing the current crowding in the top of the drift region and hence reducing the resistance component of this region [75].

- **ACCUFET**: Another possible structure is based on the ACCUFEET principle, where an additional counter-doped layer is placed along the MOS interface, restoring the channel mobility and serving as a shield against high electrical-fields from the bulk SiC in the gate oxide. Hence, under blocking conditions this region is completely depleted by the potential of the nearby P-N junction, while all the blocking voltage is now supported only by the drift region. When activated, an accumulation channel is formed near the SiO_2-SiC interface, reducing the resistance and moving the channel away from the interface, avoiding interface traps and hence increasing the mobility.
- **Other vertical devices**: Several variants of the above referred basic structures can be found in the literature. One first example is the so-called advanced accumulation-channel UMOSFET [76], [77], [78] with a P-layer below the trench structure that shields the gate oxide against high field levels and an N-epilayer between the P-base and N-drift regions that lead to higher current spreading avoiding current crowding in the trench corners. A similar device was presented in [79] and employs a second buffer layer up to the level of the P-implant below the gate trench. Another variant is the so-called triple-implanted MOSFET where a double P-implantation along with a buried source contacts decouple the problematic relation between the doping concentration of the P-base region with the channel mobility and threshold voltage. The IEMOSFET as presented in [80], [81] relies on an approach similar to the ACCUFET, but with the difference that half of the P-layer underneath the source contact is created by epitaxy, resulting in a smoother surface with higher channel mobility. In [82], the channel region in the DMOS structure was built with an epilayer, significantly reducing its inherent resistance and obtaining one of the lowest values of specific chip resistance in the voltage class of 1200V.

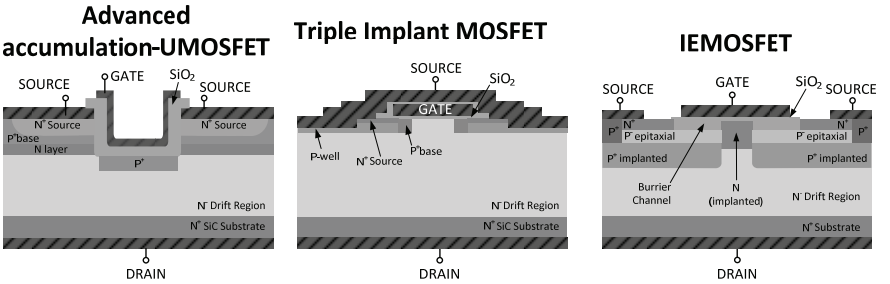


Fig. 8: Other SiC MOSFET structures.

In general, the total resistance of a MOSFET is the sum of the individual values from the channel, JFET region and drift region, though the existence of some of those depends on the employed structure, as already discussed. While in silicon designs, the drift region becomes dominant at higher voltage levels, the same is not valid for SiC devices due to the thinner width and higher doping concentrations. While JFET resistance is affected by the gap between the source cell implantations, the drift layer resistance is affected by the doping and thickness of the layer. Meanwhile the channel resistance is affected by the channel mobility and threshold voltage. These both parameters can be controlled by the nitridation process and are inversely proportional to each other. Hence obtaining a higher threshold voltage requires sacrificing the channel mobility what represents perhaps the major challenge behind the design of the MOSFET structure.

The resistance in practical devices is nevertheless normally higher than theoretical values due to the lower MOS channel inversion layer mobility [83]. A direct reason for this is the production process of the SiO_2 region that relies on thermal oxidation, resulting in a disordered interface containing several silicon oxy-carbides along with high density of interface states. These can in turn either trap electron/hole carriers or act as recombination centers/scattering sites thus reducing the overall carrier mobility [84]. The oxidation process was hence a major focus of research and enhancements in the last years. Alternative for dealing with such problematic is reducing the length of the channel to obtain a high value of transconductance. Additionally, the channel density needs to be kept high.

Regarding the temperature dependence, the channel resistance displays a negative coefficient, while the other two components have a positive coefficient. Hence, in the SiC-MOSFET a lower temperature dependence of the total device resistance can be observed.

In the graphic below are presented the values of specific chip resistance for different MOSFET designs found in the literature. The lowest values were so far

obtained with the DMOSFET structure, while the lateral devices present values almost an order of magnitude higher.

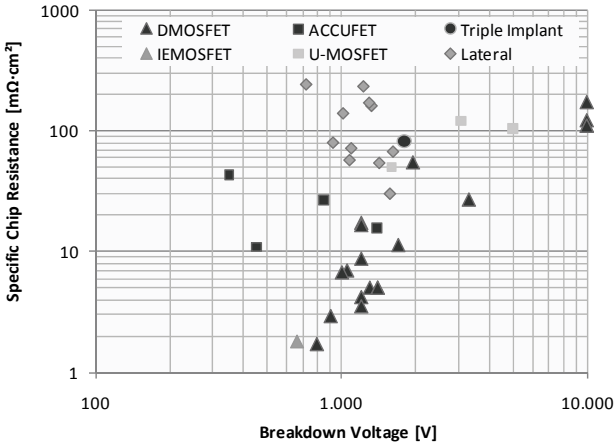


Fig. 9: Specific chip resistance as a function of the device breakdown voltage at room temperature [85],[86],[87],[88],[89],[90]-[95], [96]-[98],[99],[100],[101]-[113].

In contrast with their Si-based counterparts, SiC-MOSFETs display a significantly less clear threshold limit and saturation regions. This is mainly explained by the interface quality in the channel region [114]. As a consequence, not only can the device resistance be strongly affected by the gate voltage, but also the implementation of short-circuit detection becomes more complex. SiC-MOSFETs are also characterized by an output capacitance density approximately 10X higher than Si devices, mainly due to the very thin drift region and higher doping concentrations (100x higher). Such characteristic affects the turn-on under hard-switching conditions, as the output capacitance needs to be discharged through the MOSFET channel. In case of high values of dv/dt, the channel current density may reach very high values [115]. The input capacitance is also larger due to the tight cell geometry for achieving higher channel density [116].

Most SiC MOSFET structures have an intrinsic PiN Diode with an on-state voltage drop around 2,5-2,7V. Due to such high voltage drop, an antiparallel Schottky can be employed in order to attain optimal switching performance. Caution needs nevertheless to be taken at higher temperatures and higher current values, when the intrinsic diode may enter in conduction before the external Schottky. The reverse recovery of the intrinsic diode is nevertheless much lower given the very small minority carrier lifetime and also the thin drift layer [117]. Reverse conduction is

also possible, as the current will go through the same path, given the drain-source voltage with a negative polarity and the gate voltage above the threshold limit. Such possibility becomes interesting when considering applications where synchronous rectifying is possible. The current will then be shared between the MOSFET structure and through the intrinsic diode, reducing the total losses [117].

Concerning reliability, the long-term stability of the gate oxide is normally considered one of the most critical issues in SiC MOSFETs. One first reason for this is that the gate oxide is under increased stress due to the higher values of electrical field. While the device is activated, the electric field remains concentrated on the interface with the N^+ source given the application of a positive gate bias. For off-state, the highest field moves then to the region near the JFET interface and near the edge terminators [118], [119], [120], [121]. Such higher values of stress becomes especially critical here because of the lower barrier height between the interface with the SiO_2 (2,7eV for SiC in comparison to 3,1eV for Si), increasing the probability of electron injection, especially at higher temperatures. As a preventive measure in order to deal with such problematic and avoid tunneling currents, the electrical field is normally kept in the design below 3MV/cm [116]. One possibility to decrease the stress in the oxide interface is reducing the cell pitch. Another effect reported in the literature [122], [123], [124], [125] is the threshold voltage shift, mainly caused when charges are captured in traps found either in the bulk SiO2 or in the interface with SiC that can be later removed by a gate voltage bias in the opposite direction.

2.1.1.1. Operation & Driving

Control of the SiC-MOSFET is basically the same as the one valid for Si-MOSFETs. On first difference is that plateau on the gate voltage cannot be completely observed in some SiC-MOSFETs designs, because of the unclear limit to the saturation region given the higher channel-length modulation coefficient. An important consequence concerning the low transconductance and threshold voltage of SiC-MOSFETs is that these devices may be more susceptible to gate ringing effect, i.e. the direct reflection of oscillations in the device voltage to the gate signal and vice-versa.

2.2.SiC-JFETs

In face of the referred challenges from the SiC-MOSFET, JFETs have regained significant attention due to their simple and robust structure. In contrast with the MOSFET, the JFET is not controlled by an insulated gate structure but rather by a reverse biased p-n junction. Hence the structure presents no interface problems related to gate oxide, increasing the reliability and ruggedness since no aging or

parameter drift may be observed, making the device attractive for operation at high temperatures. In addition to this, punch-through of the gate junction happens only at higher voltages in comparison with Si devices due to the wider band-gap of SiC [127] giving a broader gate voltage range capability.

A final feature here is that most devices have a symmetric channel structure, enabling operation as a synchronous rectifier in the reverse direction. This enables an additional reduction on the conduction losses during freewheeling [128].

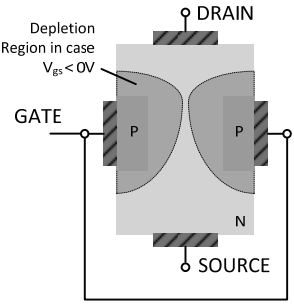


Fig. 10: Basic structure of a JFET.

2.2.1. Device structure and characteristics

Two main constructive approaches can be identified for JFETs, namely the ones with vertical and lateral structures. For the last one all contacts are placed on the upper side, being mainly intended for the so-called power integrated circuits (PICs) [129] where the control, sensors and conversion stage are integrated within the same structure. In order to extend the blocking voltage, such devices require a larger chip area, representing a significant disadvantage against their vertical counterparts, where mainly the drift region height needs to be increased. Hence vertical-JFETs represent the vast majority of designs for high voltage and power applications nowadays. A further division can be identified for such group regarding the orientation of the channel: vertical and lateral. All the referred categories will be briefly discussed in the following items.

2.2.1.1. Lateral-channel vertical-JFETs

Three first approaches, mainly investigated by the company SiCED, can be identified as depicted below [130] [131]. In all designs, one of the gate terminals is connected to the source terminal and hence normally grounded. Due to the high band gap value of SiC, the structure can rely on applying a bias for pinch-off only

in one gate, with a significant safety margin before entering in punch-through due to the material wider bandgap.

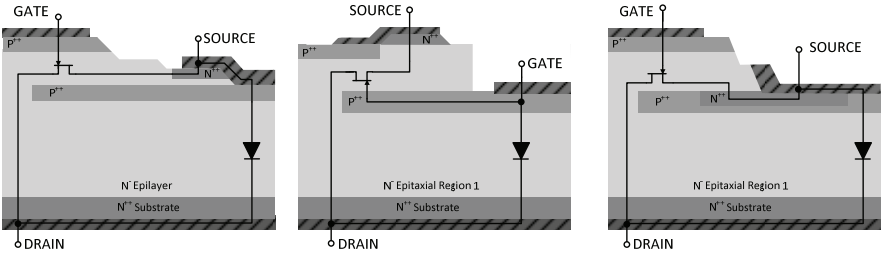


Fig. 11: Half-cells of lateral channel configurations with depiction of intrinsic diodes.

- **Surface-gate variant 1 (S1-gate)**: An upper p-layer assumes the gate function and allows reduced gate resistance due to the distributed ohmic contact. Meanwhile the source contact is smaller. The reduction of the gate-to-drain overlapping area in such design leads to a smaller Miller Capacitance that enables a fast switching behavior [132]. The specific chip resistance is nevertheless increased by almost 50% in comparison with other approaches because part of the region before the channel needs to block the gate-to-source pinch-off voltage. An advantage here is that the blocking performance depends only on the drift region and not on the channel region; hence the same gate structure can be employed for difference voltage ratings. The intrinsic PiN diode in this structure can be used for freewheeling.
- **Burried-Gate (B-gate)**: The controlling gate is composed of a buried p-layer within the structure, what leads to a low specific resistance. Reason for this is that the current flows directly from the source through the channel and then to the drift region. On the other hand, the dynamic behavior is negatively affected by such structure. A high C_{GD} (Miller) capacitance can be observed due to the large area of the gate above the drain, while a high internal gate resistance exists due to the low conductivity of the SiC-based p-type layer that needs to be extended into the device. In this design, the intrinsic diode cannot be used for freewheeling, as it is connected between the gate and drain terminals.
- **Surface-gate variant 2 (S2-gate)**: In this variant of the surface-gate design, the source region was totally shifted to the buried P-gate region. An advantage here is that the gate length can be adjusted with superior precision [131].

Other possible configurations found in the literature are depicted below.

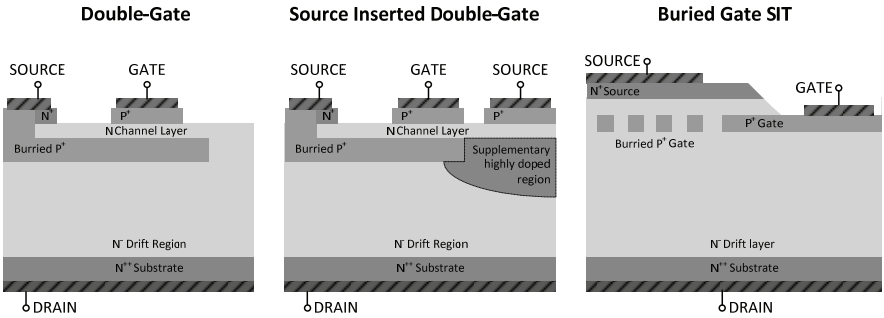


Fig. 12: Half-cells of additional lateral channel configurations.

- **Double-gate (D-gate)**: It is a variant from the surface-gate approach, where the gate is involved only in the lateral JFET, mainly with the objective of normally-off operation. Due to the reduced gate length and gate capacitances, it is possible to attain superior dynamic characteristic. The extension of the buried P-layer plays in this design an important role in order to avoid field crowding in the corner of the shallow PN junction but with the simultaneous drawback of increasing the device resistance. Another variant [133] named source-inserted double-gate limits the extension of the buried P-layer to the edge of the gate P+ axis, but with the addition of an extra source contact with high doping concentration in the channel region.
- **Buried-Gate SiC-SIT**: In this variant of the buried-gate structure, the other P-gate layers is not connected to the source/ground, but rather distributed in a fine trench structure, achieving normally-off behavior with a very low value of specific chip resistance [134].

2.2.1.2. Vertical-channel Vertical-JFETs

The vertical channel is most commonly obtained with trench implanted channel structure. In comparison with the lateral channel devices, the current approach can have simple fabrication steps and also attains lower chip resistance due to the fact that the lateral gate structures are now eliminated [135]. Higher channel mobility is observed with such devices because the electron flow takes place in the vertical direction in parallel with the c-axis. In contrast with the lateral channel devices, the gate region here needs nevertheless to be especially designed for each value of blocking voltage. Furthermore the available pinch-off limit is higher with such design because both regions lie on the same contact.

- **Long-channel enhanced-mode VJFETs**: In this structure, which is mainly employed by the manufacturer Semisouth, the channel is formed between the two p-layers from the buried Gate structures by means of masked plasma etching in a fabrication process based on the Si-trench-MOSFETs. The intrinsic pn-diode in such structure is connected from the gate to drain and source terminals. Given the large gate region overlapping the drain contact, the Miller capacitance is considerably high in such structure. By means of special doping profile and tight cell pitch design it is possible to obtain depletion of the channel at V_{GS} equal to 0V, leading to a normally-off operation. A certain temperature dependence of the threshold voltage is possible to be observed in the presented structure, with a factor around 2,5mV/K [135]. Meanwhile a high value of transconductance is necessary in order to attain the nominal current capability before reaching the built-in voltage of the gate-source diode [136]. Though a higher channel density can be achieved with such design, it is possible to observe a larger contribution of the channel structure to the device resistance due to the thin design and low doping concentration. Other possible optimizations in the structure may consider especial doping profiles leading to higher saturation current densities along with lower specific chip resistances, but simultaneously higher device capacitances and also higher electric field because of higher doping concentrations [136].
- **Trenched-implanted VJFETs**: The most significant difference on this design in comparison with the previous one is that the p-layer is processed with two different doping concentrations. Both normally-on and -off devices with low resistances have been demonstrated, although these values were commonly measured under bipolar operation [135], [138]. Though these devices do not have a body diode, a JBS SiC-diode can be integrated in the same chip structure with minor effort [139].
- **Recessed-implanted-gate VJFETs:** In contrast with the previous approaches, the gate structure is materialized by a single implant. In addition, a buffer layer is placed above the substrate and the sidewalls of the channel mesa regions do not get implanted [140]. Because of this last constructive characteristic, no intrinsic diode between the gate and source exists.

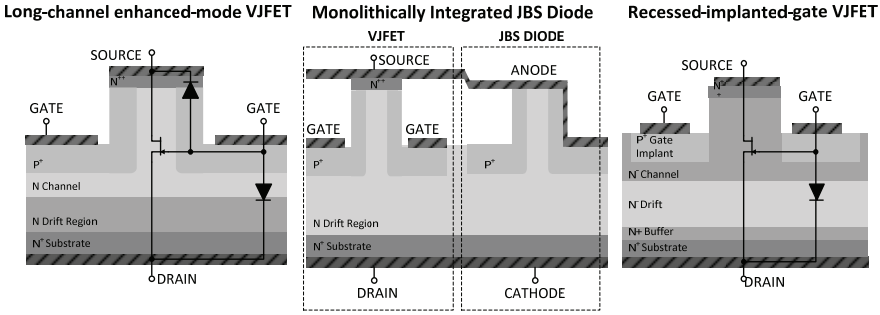


Fig. 13: Vertical Channel VJFET structures.

- **Dual-gated trench VJFET**: In this structure, trenches formed by dry etching process were later filled epitaxially with N and P layers forming the channel and gate regions [141]. Depending on the channel doping concentration, normally-on or –off devices can be obtained. Such structure presents no body-diode between source and drain. These devices suffer nevertheless from the so called DIBL effect (drain induced barrier lowering), when under high values of blocking voltage the depletion region is distorted in the direction of the drain, allowing the flow of the electrons and hence resulting in critical values of leakage current [136].
- **Double-channel**: Optimized for normally-off operation, enables lower resistance with higher channel density. The channels are separated by epitaxially growth p-stripes. The gate drain capacitance is nevertheless higher with such design, what may affect the dynamic behavior of the device [142], [143].

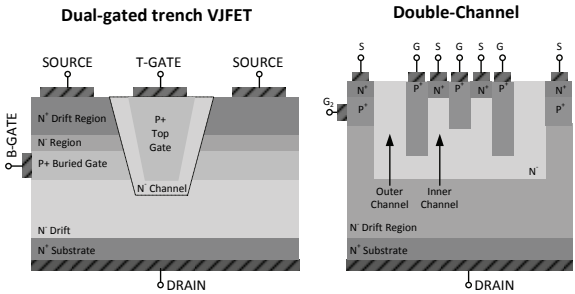


Fig. 14: Vertical Channel VJFET structures.

2.2.1.3. Lateral JFETs

Several lateral designs can be found in the literature, with both lateral [144], [145] and vertical channel structures [146], [147], [148]. The last ones are likewise the vertical-JFETs also commonly designed for normally-off behavior. Practically all the referred devices make use of the RESURF technique to further reduce the chip resistance.

2.2.1.4. Overview of specific chip resistance values

At this point it is necessary to differentiate between the unipolar and bipolar modes of operation of the JFET [149]. When the applied gate voltage rises beyond the built-in potential of the gate-source junction (approximately 2,7V), the injection of minority carriers starts to take place, indicating possible operation under bipolar mode. Such mode was in fact identified in early 80's [150], where it was demonstrated the possibility of reducing the device on-resistance by more than one order of magnitude. The observed reduction was proportional to the square root of the gate current, which in turn was proportional to the n-base concentration. Though the device resistivity can be reduced, this is accompanied by a significant drop in the structure gain with higher driving losses along with low switching speed because of the recombination time of the injected carriers [151]. An issue related to the operation under bipolar mode is the possible degradation of the on-state drain current characteristic due stacking faults promoted by the electron-hole recombination [152]. Below are presented the values of specific chip resistance as a function of the blocking voltage for the investigated structures, with distinction regarding the ones operating in bipolar mode.

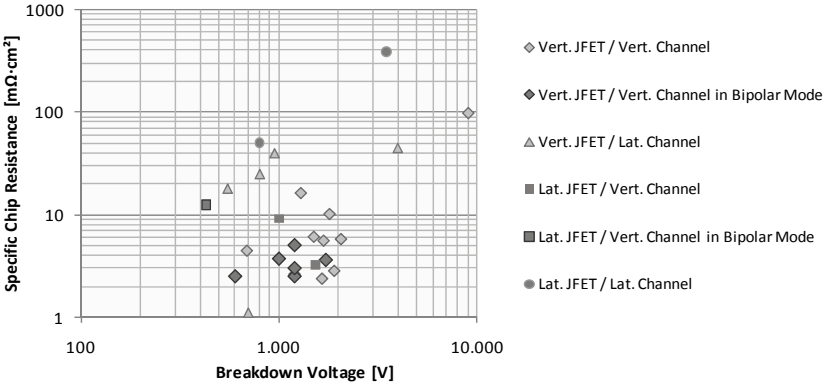


Fig. 15: Specific chip resistance of investigated JFET devices [132], [134]-[141], [143]-[148], [151], [153]-[161].

2.2.2. Operation & Driving

Considering the basic JFET structure, the most significant drawback is the normally-on behavior, as the channel will block only with a continuous negative gate voltage leading to the formation of the depletion region. Given the fact that the normally-on behavior represents an inherent reliability problem for most circuits, especial gate driving circuits and supply strategies were proposed in the literature but still end up increasing the costs and complexity. Another possibility is the use of cascode structures that are nowadays seen as the most promising alternative for the referred problematic. Such driving approaches will be discussed in the following items.

On the other hand, normally-off devices can be obtained by relying on the potential barrier formed by the grounded gate junction (V_{GS}=0V). In order to attain such capability, the channel region needs nevertheless to be very narrow with low doping concentration what results in a higher channel resistance. Another critical issue related to these devices is the reduction of the threshold voltage with increasing temperature values, what leads to the requirement of bipolar gate voltage driving to attain certain immunity against EMI [142].

2.2.2.1. Normally-on devices in stand-alone operation

As already stated before, the basic JFET structure is a normally-on device, i.e., if no voltage is applied between the gate and source terminals (V_{GS}), the device remains active. Under such conditions, the n-channel behaves like a resistor up to a certain drain-source voltage value (V_{DS}). Beyond such level, the current reaches saturation since the increasing voltage drop leads to a reduction of the channel width and increase of the depletion region.

On the other hand, when the negative values of voltage are applied across the gate-source (V_{GS}), the depletion layer of the PN-junction between gate and n-channel is increased, reducing the conductivity of the last one and leading to a total blocking state of the device, if the pinch-off limit is reached. Such level shows practically no temperature dependence and is mainly affected by the channel doping concentration and geometry.

The negative gate voltage for safe turn-off shall nevertheless be significantly lower than the pinch-off value. Reasons for this are the parameter variance between devices, temperature drift and requirement of improved ruggedness against high dv/dt transients. The voltage may nevertheless not surpass the reverse breakdown gate voltage in order to avoid the gate junction breakdown.

During conduction, operation with a slightly positive gate voltage leads to a wider channel and hence a small reduction of the device resistance (in range of 5%, according to [162]). Caution shall be taken with the direct polarization of the Gate-source junction, what would lead to an increase in the gate current and possible operation in bipolar mode, as already previously explained. All the above referred limits regarding the gate voltage are depicted in the graphic below.

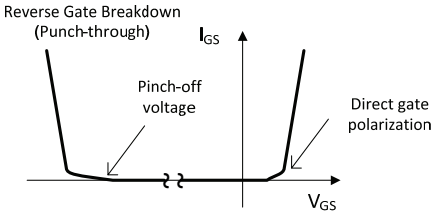


Fig. 16: JFET gate characteristic with limits regarding breakdown and direct polarization.

Considering the above conditions, it is possible to identify two main driving approaches.

In the first group, the gate is driven with fixed voltage levels between the reverse-breakdown and direct polarization limits since no gate current limitation is provided. Selecting the correct levels is nevertheless a difficult task, given the parameter variance due to the maturing technology and also the temperature dependence. Possible configurations are depicted below, mainly relying on a totem pole configuration. In the standard configuration, the upper transistor is connected to the reference ground and source, enabling blocking with V_{supply} and activating with approximately 0V. In the configuration presented in [163] the middle point of the configuration is connected to the JFET-source, enabling the selection of a positive voltage value. Another alternative [164] shifts the whole gate potential by a certain level dictated by the additional source V_{bias}, activating the JFET now with a non-positive voltage. Such solution was proposed with the objective of limiting the maximum voltage class of the driving circuit in order to enable the use of standard products in the market. Other similar solutions were presented in [165], [166] and [167].

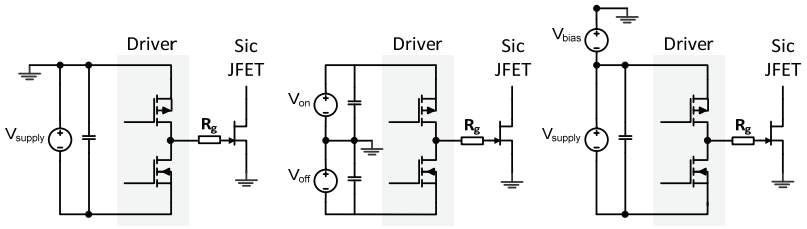


Fig. 17: Driving solutions with traditional totem-pole configurations [163], [164].

The second group of circuits provides a certain limitation to the gate current and hence enables operation with more flexible voltage levels, even over the referred limits, i.e. driving the JFET in avalanche for a brief interval of time. Such possibility allows a significant increase in the switching speed. One first circuit directly controlling the gate current was proposed in [168] and is depicted below. The voltage transients imposed by the totem-pole transistor association T_1/T_2 are translated into peaks of gate current directly controlled by the added transistor T_3. Hence, the gate current is limited while the JFET is deactivated and a gate voltage higher than the pinch-off limit can be employed to increase the switching speed.

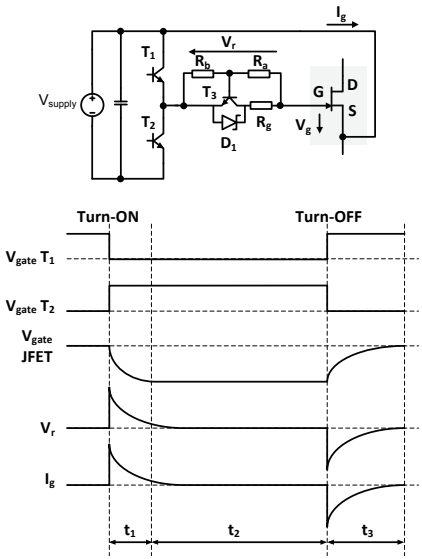


Fig. 18: JFET driving circuit as proposed in [168].

In a simpler variant of the circuit above [170], the extra branch is substituted by a simple parallel association of $C_G/R_s/D_{on}$ with the function of avoiding the

avalanche condition, given the higher level of selected V_{supply}. The referred parallel association also allows high gate current peaks that significantly increase the switching speed of the JFET. The resistor with high value R_p only serves to limit the current while the JFET is deactivated. The size of the capacitor C_g is chosen considering the required peak current transients and also to avoid a longer duration of voltage levels above the breakdown limit. Finally, the diode D_{on} clamps V_{gs} close to zero while the device is activated avoiding oscillations. With such configuration it was possible to achieve (according to the reference) a reduction of almost 50% in the switching losses.

A very similar circuit was presented in [162], with the difference that now the driving branch is directly connected to the gate terminal, while the source is connected to the positive voltage terminal of the supply. In addition, a resistor R_s was added in series with the parallel association $C_g/R_p/D_{on}$, enabling a finer control of the duration of the peak current transients by means of the time constant $R_S \cdot C_g$.

Another class of drivers still belonging to the second group relies on controlled current sources to directly limit the applicable gate current, avoiding the occurrence of avalanche. Advantages of such approach is the free selection of the voltage supplying circuit along with independence from JFET operating conditions like blocking voltage. The use of two separated sources for transient and continuous driving of the JFETs along with a logic inverter to provide the appropriate voltage reference to the gate potential was patented in [171]. In [172] a single current source is employed, while for deactivation the gate-source contacts are simply short-circuited. In the same publication, a virtual gate charge enhancement is applied by means of an additional switch and capacitor.

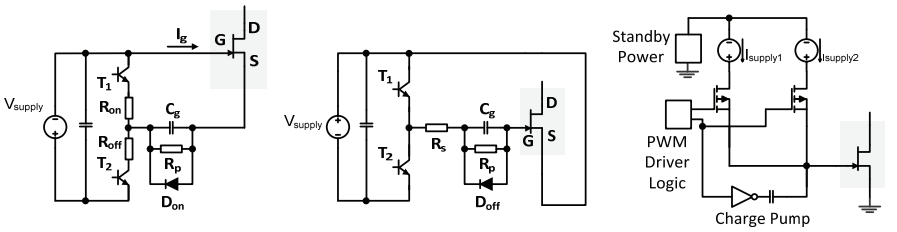


Fig. 19: JFET driving circuits as proposed in [170], [162], [171].

Regarding galvanically-isolated drivers for normally-on devices, several approaches were analyzed in [173]. Using a simple pulse-transformer driven with bipolar voltage cannot be considered as a valid solution due to the fact that depending on the duty cycle value, the negative voltage required to block the JFET will not be maintained for enough time, possibly resulting in a reactivation of the

device. In addition to this, driving the device with similar values of positive and negative gate bias is for normally-on devices not possible because of possible direct polarization. By adding a capacitor and diode to the previous configuration, the so-called DC-restorer is obtained, though the presence of a positive voltage on the secondary side may lead to saturation of the transformer. In order to avoid such limitation, a high frequency carrier signal based on the original PWM can be modulated in the circuit presented in the right-side of the picture below. By applying positive pulses to the primary side, these are rectified and charge the capacitor C_1, providing a negative bias to turn-off the JFET. By interrupting the carrier signals, C_1 is discharged by R_{gs} and the JFET is activated with 0V. Drawback of such configuration is the dynamic of the capacitor discharge, what significantly limits the attainable duty-cycle and frequency values.

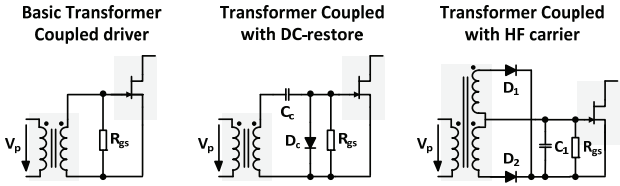


Fig. 20: Transformer-coupled JFET passive driving circuits [173].

Other configurations with inherent galvanic isolation were presented in [174], [175]. For the first one, an additional winding is placed in a buck inductor with a low output voltage (+12V), allowing the use of a normal buck controller (like the UCC3809D-1). Meanwhile the second solution employs a flyback transformer with an especially designed controller to drive the JFET, with the gate-source intrinsic diode operating as the freewheeling output diode. By means of selecting a proper size for C_{gg}, even under failure of the main supply the JFET can remain blocked for a certain interval of time long enough to allow safety switches in the circuit to disconnect the source/load and hence avoid critical failure of the circuit in case normally-on devices are employed.

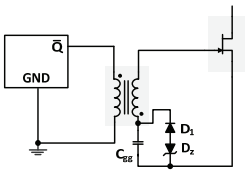


Fig. 21: Isolated gate driver configuration as proposed in [175].

The limitations of the above passive driver circuits can be overcome by using active switches as in the configuration depicted in the left-side of Fig. 22. When

the carrier signals are applied to the primary winding 1, the half-bridge output across C_g is changing between the 0V and high impedance (S_2 off) and hence activating the JFET. In the other way around, the half-bridge output is switched between the voltage of the capacitor C_{bias} and the high impedance (S_1 off). Due to the JFET Gate-source capacitance and also the extra capacitor C_g, the gate-source voltage can be kept at a negative value, hence keeping the JFET deactivated.

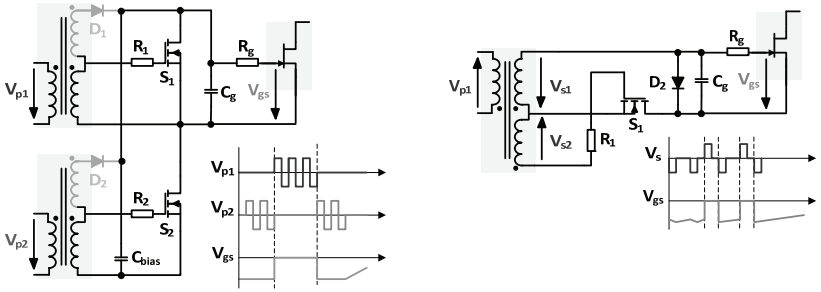


Fig. 22: Transformer-coupled JFET active driving employing phase-difference and edge-triggered circuits with respective control signals [173].

The capacitor C_{bias} is charged by the additional branches of the each transformer through the diodes D_1/D_2. In case no signals are present in both primaries, the gate-source voltage drop to zero with a time constant depending on the time constant C_g/R_g. A simpler configuration with similar functionality is depicted in the right-side of Fig. 22, being called edge-triggered circuit. The number of turns in the first and second secondary windings is chosen in order to obtain respectively the JFET and MOSFET threshold voltages. By means of a negative voltage pulse in V_{S1}, S_1 is deactivated, reversely biasing D_2, and charging C_g through the intrinsic diode of S_1 , hence resulting in the a negatively built voltage across the capacitor that blocks the JFET. In case no pulse is applied, the capacitor C_g is connected to a high impedance value (through the parasitic capacitance of S_1) and is slowly discharged. On the other hand, when a positive voltage is applied to V_{S1}, S_1 is activated and the C_g is discharged, while the gate-source voltage remains clamped by means of the direct polarization of D_2. A major advantage for the operation with short pulses in both circuits referred above is the possibility of reducing the size of the transformer due to the low volt-second product and also avoidance of transformer saturation along with frequency/duty cycle limitation.

Employing stand-alone normally-on devices contradicts nevertheless the common paradigm of only using normally-off switches; as in the case of failure of the control system or power supply and also during start-up, the switches may remain activated. In case the devices are placed in a hard short-circuit path like when

connected to a large DC-link capacitance or to the grid, a critical failure of the system may happen. Examples of such critical applications are the voltage source inverter (VSI) and most DC/DC converters. One approach to deal with such problematic is to employ a charge-pump system that provides a self-protection during power start-up [176], keeping the duration of possible short-circuit-currents below 200µs. The galvanically isolated circuit proposed in [175] may also be used with normally-on devices and by properly designing the capacitor C_{gg} (Fig. 21), a certain time interval can be guaranteed for disconnecting the source/load under failure conditions. In [177], the reliability against failure is provided in a step-down converter by means of a magnetically coupling the driver supply with the main inductor. In [178] is presented an interchangeable system of switches that during start-up immediately provides negative voltage to the drivers avoiding shoot-through. A rather complex solution presented in [179] makes use of the in-rush current from the DC-link to the supply the JFET drivers. A current limiting resistor in parallel with a bypass switch [180] is applied in the middle point of the DC-link and used to limit the DC-link current either at start-up or to avoid shoot-through, protecting the JFETs.

On the other hand, there are several circuits where the application of normally-on devices has no reliability issues. This holds true especially for photovoltaic system applications, where the source, i.e. photovoltaic array, is current-limited. In addition, topologies with series association of switching devices may indirectly provide the required turn-off capability. Additional details about such possibilities will be given in a later chapter.

2.2.2.2. Normally-on devices in switching cascode

In order to obtain a normally-off device, an alternative is to connect a low-voltage Si MOSFET in series forming a cascode association [181]. The voltage rating of the MOSFETs is chosen to be higher than the maximum absolute value of the JFET pinch-off voltage. The driving of the JFET is indirectly performed by the MOSFET. At turn-off, the MOSFET is firstly deactivated what results in an increase of the drain-to-source voltage of the same, proving a negative bias across the gate-source of the JFET and consequently blocking the device. On the other hand, during turn-on the voltage across the MOSFET drops approximately to zero, activating the JFET and hence starting the conduction. In case of freewheeling, the body-diode of the MOSFET is directly polarized, generating a bias across the drain-source voltage that activates the JFET channel. Though the Si-MOSFET is on the main current path, the contribution to the total RDSON is not critical given the inherent resistances values around 3mΩ. More critical here is the area occupied by the MOSFET, which in some cases may be even higher than the one from the JFET.

Regarding the dynamic operation, some drawbacks can be observed for such association. If the switching transient of the JFET at turn-off is not fast enough, the MOSFET may operate under avalanche mode, as it is blocking the maximum voltage and conducting the total current. Such repetitive operation may damage the MOSFET and lead to failure [169]. In addition, since both devices are implemented as discrete chips, ringing in current and voltage waveforms can be observed in the switching transients [168], what increases the losses and may result in EMI-related issues. Another reason for the ringing is the coupling of the device capacitances and the sudden change on the gate charge characteristic immediately after the V_{ds} of the MOSFET reaches the JFET pinch-off voltage [182]. The switching speed is also affected by the presence of the internal body-diode of the MOSFET which is characterized by a low dv/dt-rating.

In fact, only with special gate arrangements as discussed in [183] it is possible to properly control the switching speed of the JFET. Suitable configurations include increasing the drain-gate capacitance of the association or placing a RC network between gate and drain of the JFET and a resistor between gate of the JFET and source of the MOSFET, as depicted below (b). Another possibility (c) that was proposed by the company Semisouth relies on separately driving the JFET alongside the MOSFET as depicted in Fig. 23 c). The path to the JFET gate from the driving MOSFET is now connected through a pump-capacitor and a Zener diode, to limit the charge of the last one. Thy way, the JFET is also directly activated through the main driving bridge enabling faster transients.

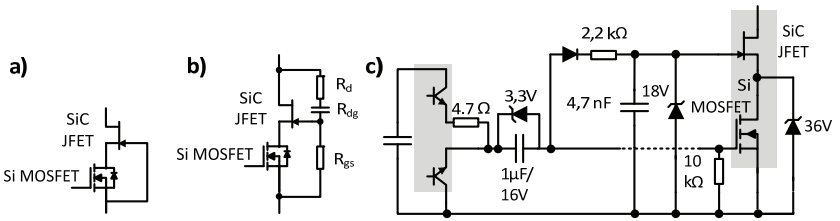


Fig. 23: Cascodes: a) basic; b) variant from [183]; c) variant from the company Semisouth.

Not least, a general drawback of the cascode is that now the maximum operating temperature is limited by the capabilities of the Si device. An alternative is to employ a normally-off low-voltage SiC-JFET instead of the MOSFET as was presented in [159], with the advantage that now the PiN diode of the high-voltage JFET can be used without the influence of the MOSFET's intrinsic diode. In a step further, the reference [184] presents a multiple cascode where the original one is driving a JFET rated at higher voltage. Both JFETs were in this case integrated in

the same chip, as the one with lower blocking voltage was designed with lateral structure.

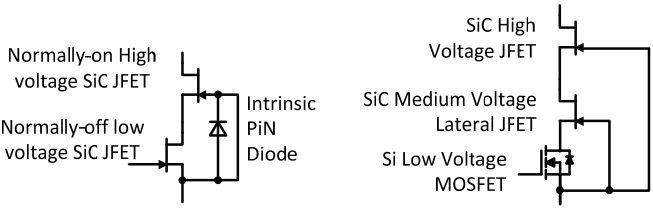


Fig. 24: Cascode structure with two SiC-JFETs.

2.2.2.3. Normally-on devices in static cascode

An alternative to the previously referred cascode configuration is the so-called "light" [182] cascode where the JFET is directly controlled, similarly to the normal stand-alone operation. The low-voltage MOSFET in series has the function of a "safety switch" and allows proper blocking of the structure under power failure or start-up conditions. For normal operation, the MOSFET remains always activate. The diode D_{gs} ensures that the gate potential of the JFET is clamped to V_{DS} of the MOSFET in case of deactivation or power supply failure, leading to an operation similar to the classic cascode. Two separated driving signals are necessary here, though the implementation does not require isolation because both hat the same reference potential. Another cascode light configuration employs P-channel MOSFETs [194] as depicted in the right-side of the picture below. Advantage here is the reduced source inductance of the JFET driver which is directly connected to the JFET source instead of through the MOSFET source. In addition to this, the P-Channel is controlled through a negative gate voltage so that no dual polarity for the power supply is necessary, keeping the driver design simple.

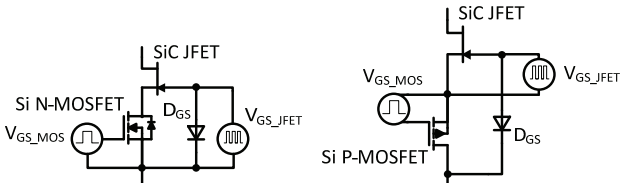


Fig. 25: Cascode light structure with N- (left) and P-channel MOSFETs (right).

The cascode light offers a far superior dynamic behavior when compared with other configurations, having much lower oscillations and also enabling precise control of the JFET switching transient. The drawbacks regarding temperature

limitation and additional parasitics in the current path are nevertheless still valid for this case.

2.2.2.4. Normally-off devices

In normally-off devices, conduction happens only when a positive voltage higher than the threshold value is applied across the gate-source terminals. Such level is nevertheless very low, normally below 1,5V, what makes the device especially susceptible to EMI induced voltages. In order to deal with such problematic, three options are available. The first two are either reducing the switching speed (dv/dt) or placing a capacitor between the gate-source [185]; with the drawback of increasing the switching losses. On the other hand the third option does not affect the losses but rather the driver complexity/expenditure by means of applying a negative gate bias when blocking the device (likewise is made with high power IGBTs) [186].

An especial requirement of some normally-off devices (for example the enhanced mode JFETs from Semisouth) is that the operation with direct polarization of the gate-source diode is advised by the manufacturer in order to attain the nominal values of forward-resistance [195]. Hence a higher value of gate current starts to flow during conduction, as is presented in the graph below for [187]. As can be observed, the temperature dependence is significant and needs to be considered when designing the driver in order to avoid higher losses.

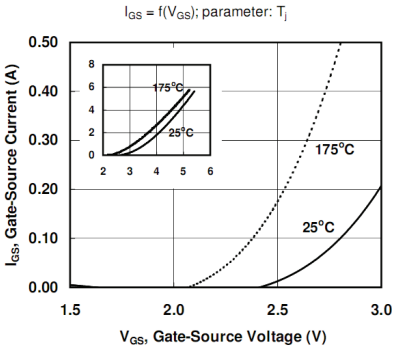


Fig. 26: Gate-source current as a function of gate-source voltage [187].

It becomes mandatory here to employ a driver solution with gate current limitation. In [188] is proposed a simple association with bipolar voltage (±5V) and gate current limiting resistor. The current limiting resistor can be calculated by the following equation, where V_{supply} represents the supply voltage, V_{GS} and I_G respectively the gate-source voltage drop and the respective gate current value.

$$R_g = (V_{supply} - V_{GS}) / I_G \tag{5}$$

The use of charge pumps (capacitors in the gate path) is also employed in majority of configurations here to provide peaks on the gate source current, enabling faster charge/discharge of the device parasitic capacitances and thus faster switching speed. The choice of the capacitance value needs to take in consideration not only the desired pump-effect but also the inherent charge/discharge dynamic since the capacitor needs to be fully charged before the next transient. In case this does not happen, less charge will be available for the next activation, slightly increasing the turn-on losses [186]. Advised is either a value at least 10 times larger than the device Miller capacitance or calculated by the equation below [189].

$$\frac{2 \cdot Q_{Miller}}{V_{supply} - V_{GS}} \leq C_{pump} < \frac{4 \cdot Q_{Miller}}{V_{supply} - V_{GS}} \tag{6}$$

A simple parallel association of the capacitor and gate resistor was presented in [190], while in [137] a resistor in series with the capacitor allows a finer regulation of the RC time constant. A Schottky diode was also added in parallel with the gate resistor in order to enable fast turn-off [191], as depicted in Fig. 27 a).

All the presented circuits employing charge-pump have as critical drawback the dynamic limitations regarding the charging of the capacitor, being therefore unsuitable for certain values of switching frequency and/or duty cycle. In order to address such problematic, another configuration relying on a multi-stage approach was presented in [192], as can be observed in Fig. 27 b). In the beginning of the turn-on transient, the transistor T_1 is briefly activated providing the required peak current through R_1, which has a low resistance value. Afterwards, T2 is activated and remains so during the rest of the active time. The deactivation takes place with T_3 by means of a negative voltage and also low resistance R_3. Circuits with similar operation were presented in [193] and are depicted in Fig. 27 c) and d). The only difference now is that the first one can be arranged with two discrete driver ICs (in totem-pole configuration) and the second one is suited when driving large chip areas.

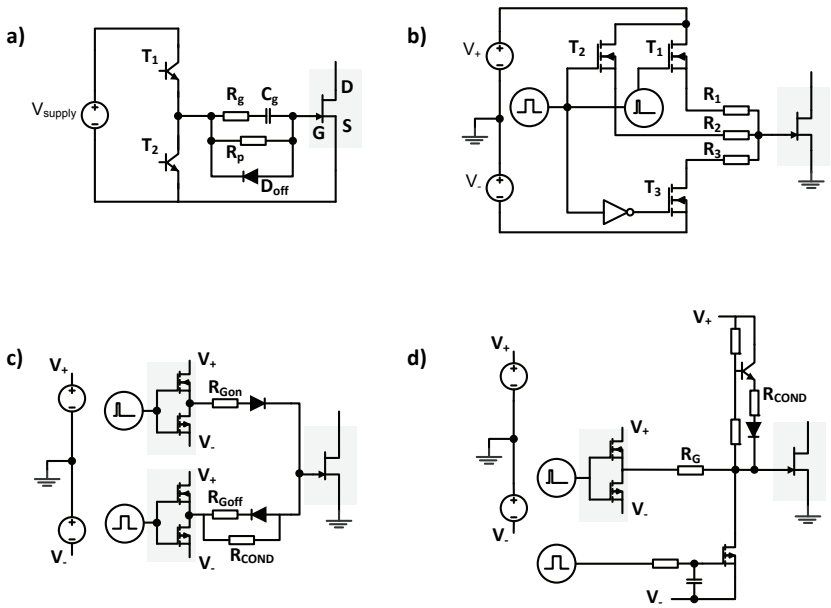


Fig. 27: Driver configurations as proposed in [191], [192] and [193].

2.3. SiC-BJTs

The BJT is the SiC bipolar switch configuration that has been most frequently investigated. Due to the junction voltage cancellation (base-emitter voltage is equal to base-collector voltage), the device resistance can be mainly summarized by contact/bond resistances plus substrate and collector layer resistances. In Si-based devices, this last component can be is reduced by means of employing conductivity modulation. On the other hand due to the outstanding properties of SiC, the plasma injection becomes attractive only at higher voltage levels thus resulting in a bipolar device with a behavior practically identical to a unipolar one in voltage levels around 1kV.

2.3.1. Device structure and properties

The BJT structure itself is known for several decades but the application based on Si was so far limited due to some critical drawbacks like low current gain, poor switching performance, limited safe operation area (SOA) with possible first and second breakdown effects.

Practically all of the referred drawbacks were overcome by the use of SiC. The possible reduction of the drift thickness allows lower excess of charges during conduction, thus enabling considerably faster switching behavior [196]. In comparison with other unipolar structures like MOSFETs, the BJT offers in fact the possibility of reaching one of the lowest specific chip resistance values. Due to the voltage cancelation of both junction voltages ($V_{BE,sat}$-$V_{BC,sat}$=0,1…0,2V), the most significant components are the resistances of the drift region and emitter/base contacts [197]. Other factors leading to low resistance values are the absence of a channel region and finally the possibility of conductivity modulation of the drift region, though this is applied only at very high blocking voltages.

The gain obtained with SiC-BJTs is more than 3 times higher than their best Si-counterparts and is mainly achievable by optimizations related to several constructive aspects like emitter-base geometry [198], surface passivation [199], ion-implantation [200] along with higher minority carrier lifetime in base/emitter layers [201] and finally base ohmic contacts [202]. Obtaining higher gain ($\beta_{current}$) values is nevertheless increasingly difficult for higher blocking voltages, given the semi-empirical relation described in the equation below, where BV_{CEO} and BV_{CBO} are respectively the open-base and collector base breakdown voltage values. The factor n is equal to 4 and 6 respectively for npn and pnp transistors.

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta_{current}}} \tag{7}$$

Breaking such limit would require a novel structure as proposed in [203], where a floating N-type buried layer (FBL) is placed in the middle of the P-region of the base.

In the graphic below is presented an overview of the chip resistance and gain values at room temperature as a function of the rated breakdown voltage for devices presented in scientific publications in the last 10 years. While an increasing tendency of the specific resistance as a function of the breakdown voltage can be clearly observed, no clear pattern is observed for the device gain. An explanation for this lays on the fact that for the presented voltage classes around 1 and 2kV the above referred dependency is not yet critical.

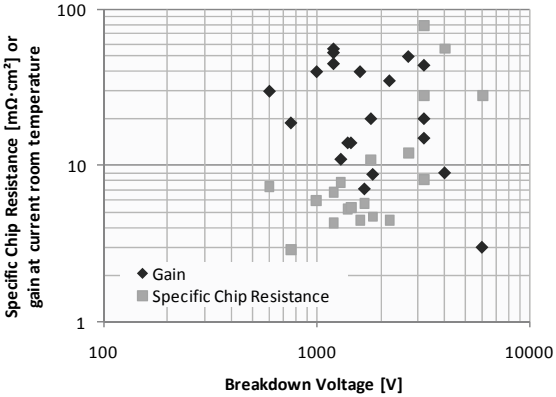


Fig. 28: Specific chip resistance and gain depending on the device breakdown voltage [197], [204],[205], [207]-[219].

The first breakdown is practically inexistent with SiC devices given the fact that the current gain now presents a negative thermal coefficient. Meanwhile, the second breakdown is also much less critical with SiC-based BJTs, since the superior doping concentration (two orders of magnitude higher than with Si) moves the referred phenomenon to much higher current density levels. According to investigations presented in [232], the short-circuit ruggedness of SiC-BJTs is in fact higher than the one observed for IGBTs due the higher junction temperature limit for avalanche injection and also lower saturated short circuit current (2,4 times the rated current against 5-6 times for Si-IGBTs)

The basic structure of the NPN BJT is depicted in the left hand-side of the picture below. The structure is normally obtained with a complete epitaxial construction since in case of ion-implantation for the emitter, the damage results in low lifetime and hence low gain [220]. The base-collector junction is normally terminated by an ion implanted junction (JFET) [221]. Due to the absence of intrinsic diode function, an external freewheeling diode is necessary. Developments in the direction of same chip integration with MPS or PiN diodes have already been investigated [205] and are presented below. One of the main advantages is sparing metallization and contact steps.

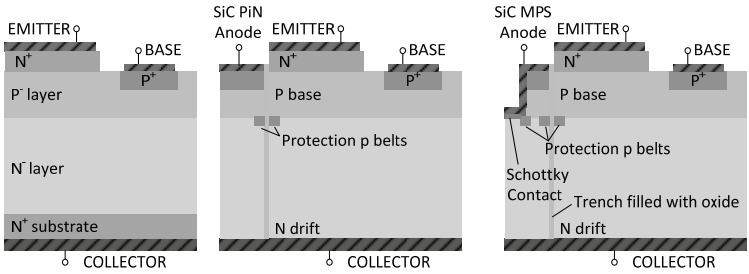


Fig. 29: Basic structure of a NPN BJT (left) and BJTs with respectively PiN (center) and MPS (right) integrated diodes.

Considering the reliability of SiC-BJTs, the so-called bipolar degradation effect was initially observed in several devices and was characterized by certain reduction on the device gain and increase of resistance values. One first reason [223] assumed for such effect considered the interface between the SiC and SiO_2 layer, which is normally employed as an inter-metal dielectric between the emitter and base. The much higher amount of active traps present here could lead to a higher level of surface recombination and could also explain the above referred effects. Another theory considered the stacking faults in the low-doped collector region [224]; in a similar way to what was observed with SiC PiN diodes. Due to the energy liberated during the recombination processes, these faults tend to growth, blocking the vertical current path and thus resulting in higher device resistance [225], [226]. In more recent devices, such effect was practically eliminated by means of materials with low defect ratio (basal dislocations), so that now it is in fact even possible to observe after several hundred hours of operation a slight decrease in the device resistance [225].

2.3.2. Operation & Driving

A vast multitude of driving circuits for Si-BJTs can be found in the literature. Though such topologies are in principle also applicable for their Si counterparts, an important difference now is the lower required value of base current, especially considering devices rated at voltages around 1kV, and the much lower influence of the minority carriers' dynamics.

The optimal driving conditions rely on a high peak of base current at turn-on to minimize the delay and switching energy and within a less extend avoid the dynamic saturation effect. The required peak value depends on the base-collector capacitance C_{bc} and on the expected switching transient time to charge such capacitor, being calculated in the equation below.

$$I_{base\_peak} = \frac{Q_{C_{BC}}}{T_{switching}} \tag{8}$$

Proportionality between base and collector current offers low conduction losses without oversaturation (what would in turn affect the turn-off behavior due to the excess of charges). Finally, a peak of negative base current is required to allow a fast turn-off behavior.

One first possible arrangement is employing a totem-pole configuration with negative voltage to provide a steady and high negative base current at turn-off. Though such requirement is practically imperative when operating Si-BJTs, they can be avoided when operating with SiC devices given the higher Base-Emitter voltage (3V for SiC against 0,7V for Si) that allows a faster removal of stored charges [227]. As depicted in configuration from Fig. 30, the capacitor C_1 provides a low-impedance path during the switching transients, enabling ensuring higher levels of current during activation and deactivation. The resistor R_c can be optionally placed in series with such capacitor in order to damp oscillations and provide a more accurate control over the value of the peaks. The resistor R_{base} is then placed in parallel with such association and limits the maximum base current under static conditions provided by the voltage source.

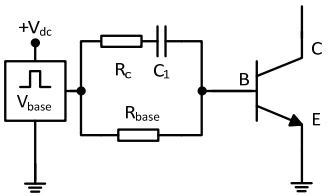


Fig. 30: Basic driver configuration for the SiC-BJT.

Though simple and cost effective, such approach presents some critical drawbacks. Firstly, the injected base current I_{base} depends on the value base-emitter junction voltage V_{be} as demonstrated in the equation below, with V_{supply} being the supply voltage from the driver.

$$I_{base} = \frac{V_{supply} - V_{be}}{R_{base}} \tag{9}$$

Under increasing values of collector current or at higher temperatures, V_{be} will correspondently increase. This will lead to a certain reduction of the base current and thus to higher conduction losses. Such effect can be observed in the graphic below, where the percental change of the base current was plotted for two possible variations of V_{be} along several levels of supply voltage V_{supply}. It becomes clear that

higher levels of supply voltage are necessary in order avoid the above referred drawback, though in turn the driving losses increase given the higher voltage drop across the base resistor. The selection of the optimal supply voltage thus needs to consider the trade-off between those two loss components.

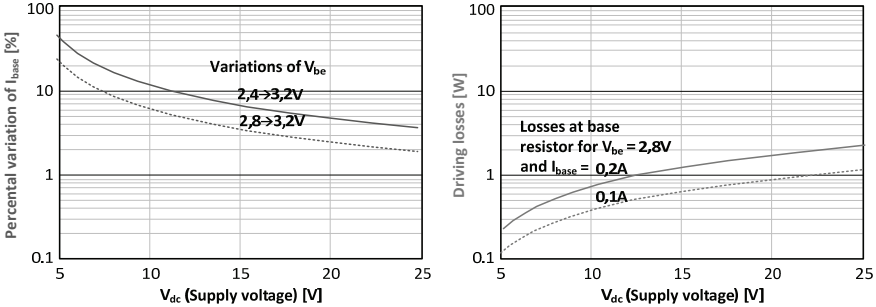


Fig. 31: Variation of I_{base} depending on selected supply voltage for different variations of V_{be} under conduction and correspondent losses on the base resistor.

Besides the above referred losses on the base resistor, another component of the driving losses is caused by the voltage drop across the base-emitter junction. The expected total driving losses can be determined with below, for a given value of duty cycle (D) [228].

$$P_{driver\_BJT} = (I_{base}{}^2 \cdot R_{base} + I_{base} \cdot V_{be}) \cdot D \tag{10}$$

An alternative to reduce the referred driving losses is the well-known Darlington association that allows a significant increase in the current gain. A similar configuration based on the referred approach is presented in [229], where the auxiliary BJT was substituted by a high voltage IGBT, not only resulting in a higher turn-on speed but also enabling the association to be voltage-driven. Considering the coupling between the voltages of the IGBT and BJT, the base current provided by the IGBT keeps certain proportionality with the BJT collector current. A common drawback inherent to the Darlington configurations is nevertheless the higher level of forward voltage drop during conduction.

Given the fact that the optimal base current may nevertheless not be achieved under the conditions, an auxiliary voltage source can be added in series as depicted in left-side of Fig. 32. In order to speed the turn-off up, a low voltage P-MOSFET shorts the base and emitter of the main BJT, reducing the necessary time for the charge combination

The proportionality between the collector and the base current in the Darling configuration can be optimized by means of a current transformer as proposed

[230] as presented in the right-side of Fig. 32. Drawbacks of such solution are nevertheless the increased complexity, along with larger inductance on the commutation path.

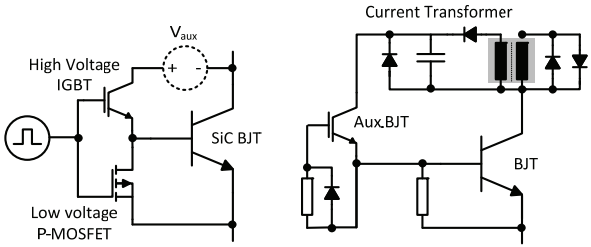


Fig. 32: Darlington-base driver configurations with IGBT/MOSFET association [229] and with current transformer [230].

Another Darlington configuration for proportional base current driving was proposed in [231] and relies on the integration of an N-MOSFET within a single chip structure named as MOS-Gated Bipolar Transistor (MGT).

2.4. GaN devices

GaN-based devices are mainly limited to Schottky and FET structures, with the HEMT (high electron mobility transistor) also called HFET (heterostructure field effect transistor) by far the most common transistor structure. Here, the junction between two materials with different band gaps (heterojunction) is employed as the channel instead of a doped region (in contrast with MOSFETs) [233]. In comparison with the traditional GaAs/AlGaAs devices, the use of GaN offers the prospect of increasing the power and voltage level due to the material especial properties. Such structure along with variants will be briefly presented in the next items, followed by constraints for operation and driving.

2.4.1. Device structure and characteristics

The principle of operation of the HEMT relies on the junction of materials with different band gap values formed, namely a n-type donor-supply layer (AlGaN) and a non-doped channel layer (GaN). In this "heterojunction" a well in the energy states is formed, from where the electrons donated by the donor layer remain trapped and cannot tunnel back, moving in only two dimensions. The current conduction takes place in such region, also called the two dimensional electron gas (2DEG). This contrasts with normal transistors, where the electrons participating in

the current conduction are donated by impurities added in the doping process and carried through these regions.

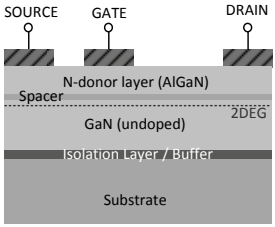


Fig. 33: Basic GaN HEMT structure.

The referred 2DEG region remains inside the non-doped region and is characterized by a high value of electron mobility due to the absence of impurities (dopants), enabling therefore very low resistance and fast dynamic behavior. The intrinsic capacitances C_{GS} and C_{GD} are also significantly smaller than the ones obtained with normal JFET structures [234].

Buffer layers are normally added over the substrate in order to isolate the defects, reduce the lattice structure mismatching and enable a smooth structure for the growing of the upper layers. These are normally intercalated with undoped layers to retain the isolation from the substrate. A very thin undoped layer of the material from the donor-region named spacer is also added above the heterojunction with the objective of isolating the 2DEG from donors generated in the active layer [235].

Due to the lack of a GaN substrate [236], compatible materials like sapphire, Si and SiC have been used. The first one has been a common substrate material for the first devices though the higher lattice mismatch and poor thermal conductivity led to an increased interest on the other two alternatives. Despite the inferior thermal conductivity in comparison with SiC, Si is arising as an attractive alternative to reduce the costs. In order to avoid a reaction between Ga and Si, an AlN isolation layers is directly applied on the surface of the Si-substrate [237].

Another issue related to operation of GaN structures is the so called current dispersion effect that is characterized by temporary increase on the device resistance right after high voltage transients across it, also affecting the dynamic behavior. An explanation for such effect is the existence of deep traps in the AlGaN layer surface. During off-state at pinch-off, these traps are filled with electrons injected through the gate, vertically depleting the channel charge. At turn-on, these electrons need to be removed in order to allow the current flow through the channel and since some are inside within these traps, removal takes

some time, causing the above referred effect [238], [239]. As consequence, under high switching frequencies, the actual device resistance could be up to several times larger than the one observed under non-blocking conditions [240].

Achieving high blocking voltages with HEMTs is another challenge for the further expansion of the technology in the direction of higher power levels. The breakdown mechanism is still under investigation, with the field distribution between gate and drain being considered the most critical element. Most high voltage devices still display high values of leakage current under blocking conditions [241] what results in additional losses [242]. Also unfavorable is the lateral structure and breakdown voltage dependence on the gate-drain spacing (drift region) [243], resulting in an expansion of the chip area in order to block higher voltages, what in turn negatively affects the attainable specific chip resistance. Another decisive aspect is the vertical breakdown against the substrate which is normally electrically grounded. For such case, promising results were presented [244] pointing that increasing the buffer layer thickness and operating with a conductive Si-substrate (resulting in a field-plate effect on the back side) enables blocking voltages as high as 1,8kV.

Several variants found in the literature dealing with some of the referred topics will be discussed in the following items.

- **Insulated gate HEMT**: One possible approach for increasing the breakdown voltage of the traditional HEMT structure is adding a dielectric layer above the heterojunction layers, reducing the gate leakage under high drain bias, alleviating the impact ionization and hence improving the blocking capability [238]. In case SiO_2 is employed, deep traps formed in the interface with GaN may significantly reduce the switching speed and lead to the already referred current dispersion problematic. One first solution to deal with such effect is the combination of SiN and SiO_2, since the first one only forms shallow traps. In [241] was also investigated a doubly isolated gate contact with SiN and HfO_2.
- **Field plate HEMT**: The use of a field plate over the gate electrode, which in turn was slightly extended in the direction of the drain, results in lower e-field concentration on the gate electrode, enabling higher breakdown voltages. Such technique was proposed in [245], [246]. In [247] the source electrode instead was also extended over the gate terminal with a field plate. A similar kind of structure is employed by the manufacturer EPC (Efficient Power Conversion), with the difference that by means of additional process steps a depletion region is formed under the gate, resulting in a normally-off device [248].

- **Insulated recessed gate HEMT**: This technique recesses the 2DEG layer by means of a trench gate structure. Current conduction takes place now only with the formation of a channel under the gate electrode with the application of a positive gate voltage, thus enabling normally-off operation in a similar way like in the MOSFET (or MISFET). Examples of the gate electrode within a recessed trench-structure insulated with Al_2O_3 can be found in [249], [233], with SiO2 in [250], [251] and with SiN in [252]. A drawback of this solution is the slight increased on-state resistance because of the inclusion of the gate channel resistance.

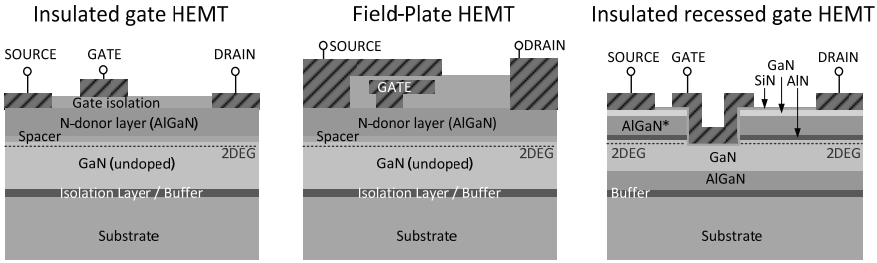


Fig. 34: GaN transistor structures: insulated gate HEMT, Field-place HEMT [245], insulated recessed gate HEMT [252].

- **DHEMT (Double Heterojunction)**: This structure consists in the exchange of the GaN buffer above the substrate by AlGaN, forming a second heterojunction and reducing the punch-through of electrons in the buffer. Such possibility thus increases the voltage limit before the avalanche breakdown [253], [254], [255].
- **HEMTs with widening depletion layer in substrate**: In order to avoid the leakage current in the edges of the interface between the Si substrate and AlN initial layer due to the inversion electrons, p+-regions are formed through doping in the device edges. The depletion region is now extended within the substrate at high blocking voltages enabling almost 100% gain in the breakdown voltage for the same structure [256].
- **MOSFET:** The interest in this structure is increasing, given the possibility of designing normally-off devices with low gate leakage current [257]. One of the main issues still under investigation is the quality of the gate dielectric/GaN interface in order to allow low channel resistance and also stable threshold voltage. The P-GaN layer can be obtained with Mg doping, while the n+ implants with Si-ions in order to form the metal-semiconductor contacts. SiO_2 is the most common gate oxide given the largest conduction band offset (2,3 eV) followed by

AlGaN (1,7 eV). A major drawback of this simple structure is nevertheless the fact that e-field is concentrated in the gate oxide on the drain side, hence limiting the blocking voltage to very low levels. An alternative to avoid the e-field concentration and enable higher blocking voltages is to apply field concentration spots with the RESURF (reduced surface field) technique, enabling devices with higher breakdown voltages [258].

- **Normally-off GIT (Gate injection transistor):** In order to obtain a positive threshold voltage, the 2DEG channel density can be reduced either through the decrease of the thickness of the AlGaN layer or higher concentration of Al atoms. This nevertheless limits the minimum achievable on-state resistance. In order to deal with such limitation, a p-doped AlGaN layer is placed under the gate contact in the GIT structure [259],[260],[261] shifting the threshold voltage and enabling normally-off operation since the channel below the gate is now fully depleted. In case the gate voltage rises above the built-in voltage of the formed gate pn-junction, holes will be injected in the channel characterizing operation in bipolar mode with current modulation.

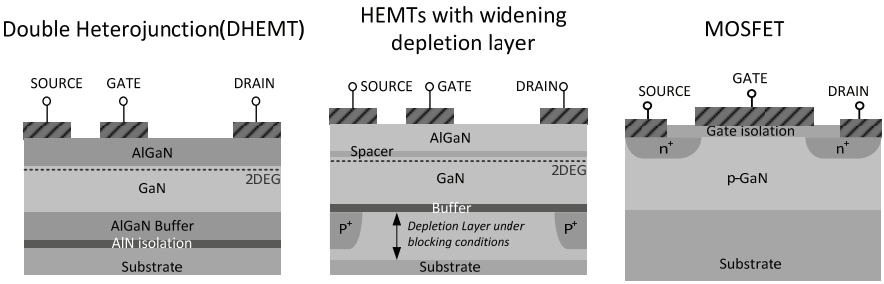


Fig. 35: GaN transistor structures: double heterojunction [253] FET, widening depletion layer HEMT [256], lateral MOSFET [257].

The specific chip resistance value for the investigated GaN devices is depicted below as a function of the breakdown voltage.

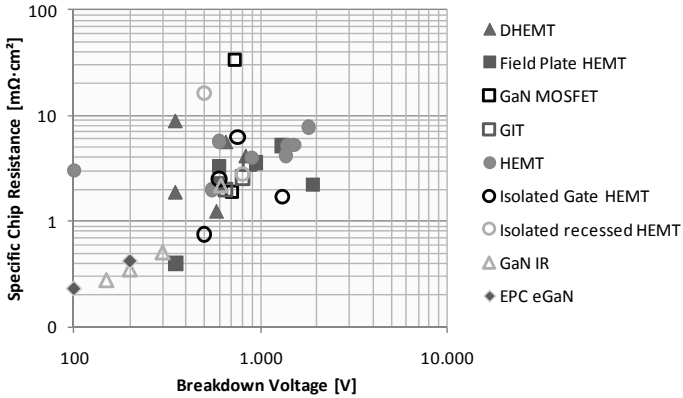


Fig. 36: Specific chip resistance as a function of breakdown voltage from diverse GaN devices [238], [241], [243]-[247], [250], [251], [253], [254], [258]-[260], [262]-[273].

2.4.2. Operation & Driving

In the basic HEMT structure, the gate forms a Schottky contact between the drain and source and in case its potential becomes increasingly negative; the well potential is raised, completely repelling electrons out the channel (or 2DEG) path and effectively deactivating the device. In contrast with their Si-based counterparts, the 2DEG is naturally formed and the device is already capable of conducting with zero gate voltage, thus characterizing a normally-on device. Driving voltages in contrast with SiC-JFETs are more limited, requiring around 10V for proper pinch-off and a slightly positive voltage for conduction with minimum losses [240].

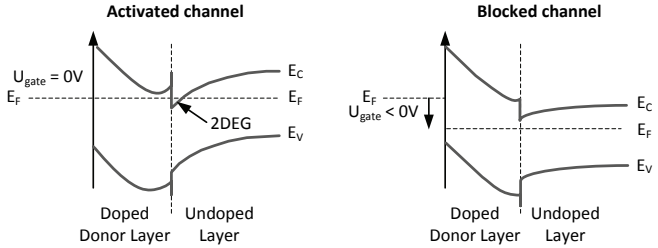


Fig. 37: Energy states at activated and blocked states in the basic HEMT.

Going from the basic normally-on HEMT structure, several cascode configurations are available depending on the targeted device application. By connecting a low

voltage silicon Schottky diode between the gate and source of the HEMT [275] as depicted below, the cascode will operate as a normal freewheeling diode. A very low level of conduction losses can be obtained with such configuration given the low forward voltage drop of the Si-Schottky Diode (around 0.3V) plus the HEMT resistance.

Normally-off switches can on the other hand be attained by classical cascode configuration, either by connecting a low-voltage enhancement-Si-JFET or Si-MOSFET between source and gate of the HEMT, being respectively proposed by the companies International Rectifier [274] and MicroGaN [275]. Such arrangement may nevertheless lead to a higher resistance level of the HEMT because its gate potential will be shifted by the auxiliary Si-device, resulting in a condition where the channel is not totally open.

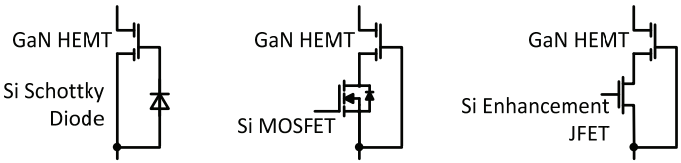


Fig. 38: HEMT configurations for freewheeling diode function and normally-off cascode.

Some modifications on the HEMT structure can nevertheless shift the threshold voltage to a positive value, enabling a normally-off operation as was already explained before. Hence driving the device now is similar to normal Si-MOSFETs.

3 Experimental investigation and benchmarking

Though much data can be obtained from publications and preliminary datasheets (as was already presented); one problem standing in the way of a fair comparison between technologies is that such information is rarely obtained under similar conditions.

This chapter will thus concentrate on the characterization of some samples under controlled conditions in order to allow a benchmarking of these devices in a later chapter. Focus was mainly given to the conduction and switching losses, along with other directly related parameters like driving characteristics and related effort. Below are listed the devices that were investigated.

Table 2 – List of investigated devices.

Manufacturer	Device #	Breakdown voltage (datasheet)	Device Type
CREE	CMF40120D	1200V	SiC MOSFET
	Sample January 2011	1700V	SiC MOSFET
Transic	BitSiC1240AC	1200V	SiC BJT
Infineon/ SiCED	120R10XT1	1200V	SiC N-on JFET
	Sample from March 2011	1700V	SiC N-on JFET
Semisouth	SJDP120R085	1200V	SiC N-on JFET
	SJEP120R063	1200V	SiC N-off JFET
	SJEP170R550	1700V	SiC N-on JFET

3.1. Experimental investigation

A certain sequence of measurements was employed here in order to characterize the selected devices as presented in the picture below, with the measurements in

the highlighted boxes, while the results are in boxes with dashed lines. The first step of the investigation focuses on the driving characteristic, defining limits to safely operate the device along with any especial driver requirements. The voltage class is obtained by means of the breakdown test, followed by the measurement of the parasitic capacitances, giving an indirect overview of the device structure and possible effects during the switching transients.

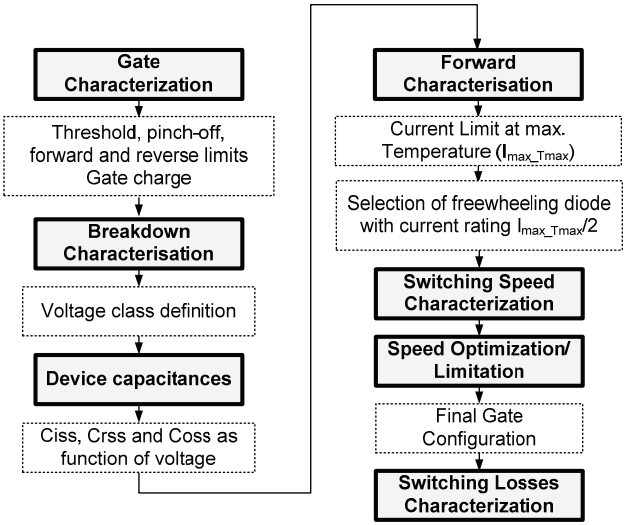


Fig. 39: Process chart for the characterization of power switches.

Static behavior under different levels of current and temperature provide an indication of the device equivalent resistance and current capabilities, enabling in turn the selection of a suitable freewheeling SiC diode. Later, dynamic characterization starts with mapping the values of di/dt and dv/dt as a function of operating parameters like voltage, current and temperature. After designing the driver circuit in order to not exceed established speed values, the switching losses are measured for a multitude of operating points.

Further details on above referred steps will be given in the following items. A final important remark is that most of the tested devices are still in "prototype" stage so that the characteristics may present a significant variance depending on the measured samples.

Most of the investigations were performed on a switching cell with step-down configuration (DUT on low side). Special attention was also given on the design of the air-coil and PCB board, as the respective values of winding capacitance and

stray inductance may affect the slope and result in oscillations during the transients [276], [277]. By means of a special compact construction, a winding capacitance of 55pF was measured for the 0,8mH air coil through the resonant frequency of the same. Meanwhile, the overall commutation path has a stray inductance of 73,5nH, already including the exterior legs of two TO-247 packages with a length of 50mm and coaxial shunt. Considering the values presented in [278] the DC-link parasitic inductance including the coaxial shunt are approximately 21nH.

In the following items are described the conditions under which the measurements took place along with other related information.

3.1.1. Gate characteristics

In order to properly design the driver it is necessary to select suitable voltage levels for activation and blocking taking under consideration characteristics like the threshold voltage limit and the forward/reverse characteristic in case of devices with PN junctions in the gate structure.

3.1.1.1. Threshold/pinch-off voltage

The threshold limit is the voltage applied to the gate terminal under which the device starts to conduct a certain amount of current. Here was assumed a limit of 300μA. Such value is investigated in order to select:

- a minimum activation voltage which is high enough to ensure that the device is properly turned-on. The influence of higher levels on the device resistance is later investigated in the forward characterization.
- a deactivation voltage ensuring that the device remains blocked. In face of the high speed switching transients, a significant amount of noise can be observed in the gate terminals; either due to capacitive coupling or due to field induction. With the objective of increasing the noise immunity, the difference of the applied deactivation voltage and the threshold limit blocking voltage is selected to be at least 4V. As a result for normally-off devices with low threshold value, a negative voltage is normally employed for blocking; while in the case of normally-on devices the negative voltage is extended to a further negative value (saving only a certain margin from the reverse breakdown value).

As a remark, in the case of current driven devices like the BJT the threshold limit does not play a significant role regarding the susceptibility against accidental turn-on. Reason for this is that the base current needs to flow continuously in order to fully activated the device (moving out of saturated region). Such characteristic makes therefore the BJT more rugged against driving transients and oscillations.

The table below summarizes the obtained results.

Table 3 – Measured threshold voltage values.

Manufacturer	Device #	Threshold Voltage @ 25°C	Threshold Voltage @ 150°C
CREE	CMF40120D	1,5…1,7	0,98…1,07
	1700V MOSFETs	2,1…2,2	1,35…1,55
Transic	BT1240AC	2,68	2,48
Infineon/SiCED	IPW90R120C3	2,96	1,80
	IKW40N120H3	5,40	4,7
	120R10XT1	-16,5…-15,25	-14,15…-13,5
	1700V JFETs	-16,2	-16
Semisouth	SJDP120R085	-5,3V…-4,75	-5,05…-4,5
	SJEP120R063	0,65...0,75	0,47…0,52
	SJEP170R550	0,6…1	0,45…0,8

An overview of the extreme values for the two temperature values is given in the picture below. Practically all normally-off devices have a rather low value of threshold voltage in comparison to a standard IGBT, with values lower than 2,5V at high junction temperature. Consequently most of them require either an active clamping technique or preferably deactivation with a negative level.

On the other hand for the normally-on devices more important is how far the threshold (or pinch-off voltage) is from the maximum applicable negative value so that it can be ensured that the device is safely deactivated without danger of gate junction breakdown. This was also depicted in the graph below for the three first normally-on devices.

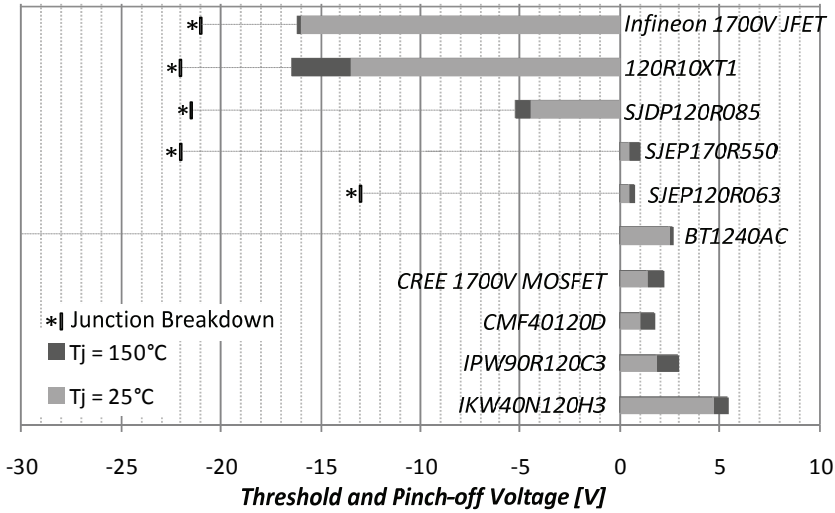


Fig. 40: Overview of threshold voltage graph for investigated devices.

3.1.1.2. Forward/reverse gate characteristic

Focus is here given to devices with PN junctions in the control terminal; namely BJTs (basis to source) and JFETs (gate to source).

Two investigations were performed to fully characterize the referred junction, namely:

- Forward characteristic: Provides the limit for direct polarization and the relationship between the current and voltage at the control terminals. Such characteristic is of major importance for current driven devices like the BT1240AC and for some JFETs.
- Reverse characteristic: Of interest here is to identify the reverse junction breakdown and thus limit the minimum negative voltage that may be applied.

For the two above cited tests, it is also necessary to consider the temperature influence; hence tests were performed at room temperature (approximately 25°C) and at 150°C. In addition to this, several samples from different chip technologies were tested to provide an initial overview of the variation of such parameters.

From the reverse breakdown characteristic, it is possible to assert some conclusions.

- A rather strong variance can be observed in the Semisouth devices, with also significant temperature dependence. The 1200V devices from the referred manufacturer, namely D120R085 and E120R063, have in fact no clear breakdown limit, as reverse currents can be observed already at levels around -10V.
- Meanwhile the devices from Infineon have showed lower temperature dependency and also lower parameter variance. Some of the tested devices still have a rather soft transient into the breakdown region, as discussed above.
- The BT1240AC from Transic has showed not sign of reverse breakdown up to 40V, as the junction is capable of supporting a much higher voltage level when compared with the JFETs; mainly due to differences in the device structure and construction.

Regarding the forward characteristic, the following points could be observed:

- The forward polarization limit of the junction can be found ranging from 1,7 to 2,1V for a junction temperature with 150°C, with an average increase of 1,3V when the temperature drops to 25°C.
- All devices presented only a slight parameter variance, with the 120R10XT1 and E170R550 displaying the most homogenous data among the tested samples.

3.1.1.3. Gate Charge

Besides the already investigated voltage limits and thresholds, the gate charge is another key property to be investigated, as it represents the amount of charge (in Coulombs) required to properly control the device. It is also an indirect indication regarding how fast a device can operate, taking in consideration the level of gate driving current. On one hand, the required driver current capability (I_{gate}) can be asserted from the measured charge (Q_g) and the required switching times ($T_{switching}$), as given in the equation below [279].

$$I_{gate} = \frac{Q_{gate}}{T_{switching}} \tag{11}$$

From this value and the selected driving voltage (U_{supply}), the driver impedance (gate resistor, R_{gate}) can be directly deduced (without considering devices with an intrinsic diode on the driving terminal)

$$R_{gate} = \frac{U_{supply}}{I_{gate}} \tag{12}$$

Another use for the gate charge is to calculate the expected power rating of the driver (P_{driver}), now depending on the selected switching frequency (f_{sw}). More about such topic will be later discussed in the chapter 3.2. Additional power components still need to be considered in the final driver design, like the losses in the gate resistor.

$$P_{driver} = Q_{gate} \cdot f_{sw} \cdot V_{drive} \tag{13}$$

The most common test methodology to investigate the gate charge [280], [281] is providing a constant value of gate current and measuring the behavior of the gate voltage for a given value of drain current and voltage, which are kept fixed. Since the gate current is constant, the time scale can be directly translated into the charge in Coulombs, as depicted below. During the first rise of the gate voltage, the gate-source capacitance is being charged with the correspondent charge being named Q_{gs}. Afterwards, the voltage across the device drops while the gate-drain capacitance is charged; meanwhile the gate voltage remains constant, forming the so-called Miller-Plateau. The charge of such period is named Q_{gd}. Both referred components form then the so-called gate-charge. The gate current nevertheless continues to flow as the gate voltage rises up to the driver supply voltage consuming an additional amount of charge (Q_{final}) that is normally not mentioned in devices datasheets as it directly depends on the final selected gate voltage.

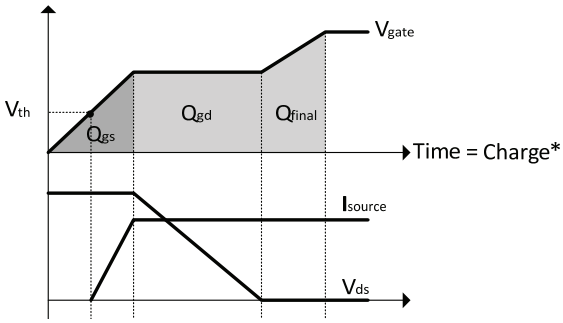


Fig. 41: Simplified turn-on diagram with gate charge components.

The investigation of the gate charge was performed here on a different way that from the above cited references. Firstly, a very high gate resistor (300Ω) was used to reduce the switching speed and consequently the oscillations, enabling the identification of the limits from each transient. In addition to this, another resistor was placed in series to measure the current provided by the gate driver. The charge was then simply obtained by integrating the gate current curve along the time with a digital oscilloscope. The commutation took place here with an inductive load at

the highest current values and different voltage levels in order to assert a realistic value for the expected gate charge.

An overview of the measured values for the three charge components is presented below, along with the testing conditions regarding gate voltage, source current and drain-to-source voltage. All measurements were performed at a junction temperature of approximately 25°C, with results presented in the picture below.

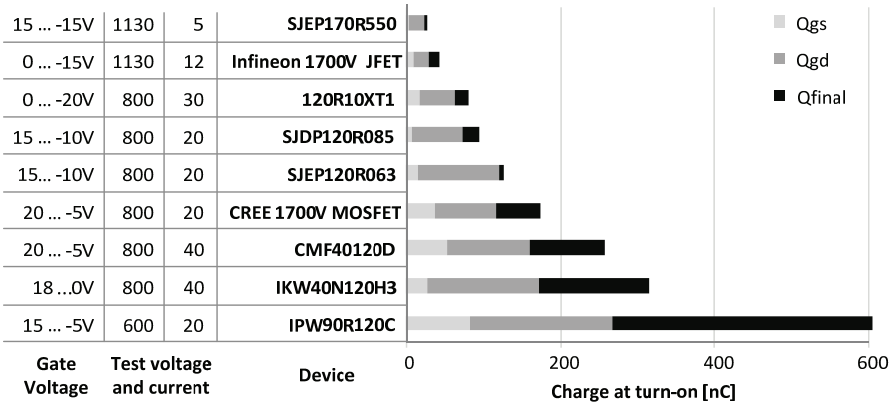


Fig. 42: Gate charge components for investigated devices.

From Fig. 42 it is possible to draw some following conclusions:

- As expected the CoolMOS device presents the highest charge given the high intrinsic capacitance values. The value of Q_{final} is in this case more than half of the total charge.
- The SiC MOSFETs presented similar values as the ones observed for the IGBTs with similar ratings. Despite the much smaller chip area, the device capacitance remains high due to very thin drift region and higher doping concentrations.
- JFETs present on the other hand lower values of charges, especially regarding the value of Q_{final}, as normally either 0V or a very low value of gate voltage under forward polarization is observed.

3.1.2. Device capacitances

The three main device parasitic capacitances are normally lumped together in three components as depicted below: input capacitance (C_{ISS}), output capacitance (C_{OSS}) and reverse capacitance (C_{RSS}).

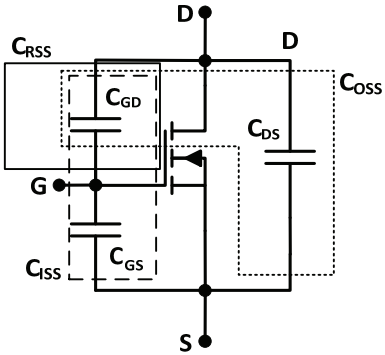


Fig. 43: Representation of parasitic capacitances displaying the lumped components.

The value of these components and their dependency to the voltage across the device is directly related to a series of important points regarding the expected dynamic performance:

- Input capacitances (C_{ISS}) : related to switching delays and values of gate charge
- Reverse capacitance (C_{RSS}): directly affects the duration of the Miller plateau and rate of change of the voltage during commutation
- Output capacitance (C_{OSS}): energy stored there during turn-off is converter in thermal energy during the turn-on, being therefore the smallest theoretical value of for the switching losses

The measurements were performed with a high-precision impedance analyzer Wayne Kerr 3260B and with an especially developed board having an isolation capability of 1000V. Such isolation was obtained by means of high voltage ceramic capacitors that were compensated using the spot calibration feature of the referred impedance analyzer. Tests were always performed at frequency of 1MHz. Two values of AC signal amplitude were employed in order to enable high resolution without influencing the capacitance behavior - $10mV_{AC}$ was employed at voltage levels below 10V and 100mVAC beyond it. Normalized values of the capacitances against the device equivalent resistance will be presented later on the benchmarking.

3.1.3. Forward characterization

The characterization of the conduction behavior was not performed with a curve tracer but rather with the direct measurement of the voltage drop across the device under conduction.

- The device was activated with two short pulses to avoid self-heating.
- Current was kept constant during conduction
- Clamping circuit limited the maximum voltage to enable measuring with very high resolution avoiding overdriving problems of the oscilloscope channels.

The following parameters were investigated in the performed tests:

a) Gate control characteristics: in case of voltage- (MOSFETs, JFETs) or current-controlled devices (BJTs, bipolar BJts) different values of respectively gate voltage and current were tested.
b) Temperature: the measurements were made following three temperature steps (25, 75 and 150°C) in order to assert the temperature dependence.

Obtained results will be presented on the comparison and benchmarking of devices.

3.1.4. Switching behavior characterization

The dynamic performance of the referred SiC devices was investigated in order to assert the level of losses under selected levels of switching speed. A more detailed explanation of the switching transient for unipolar devices will be firstly presented in the next item, followed by an overview of measurement conditions and techniques. The obtained results, likewise happened with the forward characteristic, will be employed in the benchmarking process to be later presented.

3.1.4.1. Switching transient description

The ideal switching waveforms are presented below, under the assumption of no parasitic components at board level and freewheeling diode without any stored charge or energy.

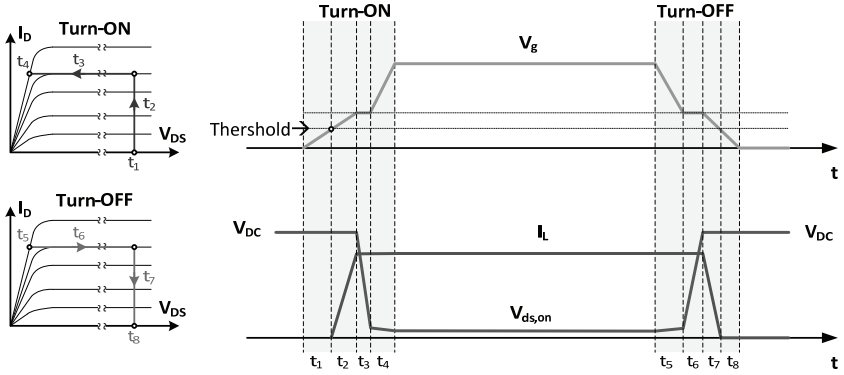


Fig. 44: Ideal switching waveforms for inductive load

A brief description of each stage is given in Table 4.

Likewise in the case of the Si-MOSFET and all other unipolar devices, the switching behavior is mainly governed by the device capacitances, namely C_{GD} and C_{GS}. The main limitation of the switching speed is thus how fast one can charge/discharge these device capacitances, what in turn can be affected by the driving current (resulting from the gate voltage and gate resistance).

As a first remark, the referred plateau on the gate voltage cannot be completely observed in some SiC-devices (especially MOSFETs), because of the unclear limit to the saturation region given the higher channel-length modulation coefficient. In the final interval of the activation, the drain voltage continues to drop entering the ohmic region and reaching the nominal conduction value, as the gate voltage will afterwards rise up to the supply level. On the other hand, an important consequence concerning the low transconductance and threshold voltage of some SiC-devices is that they may be more susceptible to gate ringing effect, i.e. the direct reflection of oscillations in the device voltage to the gate signal and vice-versa.

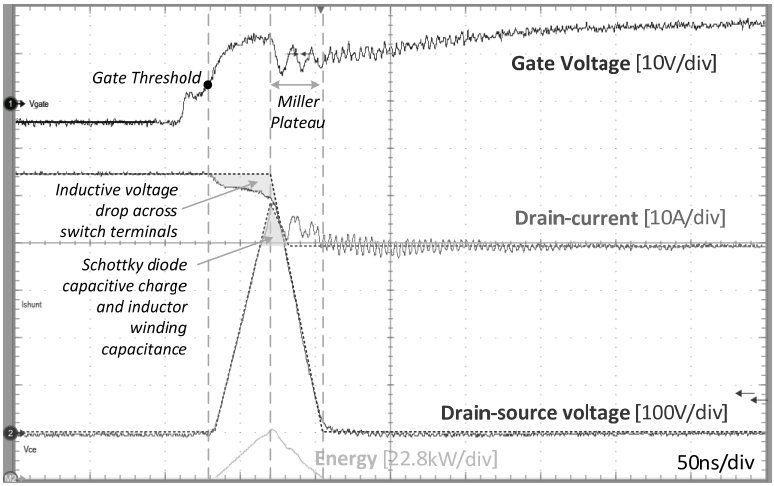
Table 4 – Ideal switching waveforms description, with R_g (gate resistor), V_{GS_ON} (driver on-voltage), $V_{plateau}$ (Miller-Plateau voltage) [292]

Name	Description and equation
t_1 Turn-on delay	Time required to charge the input capacitance to the threshold level. $t_{delay,on} = R_G \cdot C_{ISS} \cdot \ln\left(\frac{V_{GS\_ON}}{V_{GS\_ON} - V_{TH}}\right)$
t_2 Current rise	Transference of the load current from the diode to the switch, as its channel resistance is being reduced. $t_{current,rise} = R_G \cdot C_{ISS} \cdot \ln\left(\frac{V_{GS\_ON} - V_{TH}}{V_{GS\_ON} - V_{PLATEAU}}\right)$
t_3 Voltage fall	Diode stops conducting and starts. V_{gs} practically unchanged due to the discharging of C_{gd} (device operating in saturation region). Stored charged in C_{ds} is discharged as voltage drops. $t_{voltage,fall} = \frac{Q_{GD} \cdot R_G}{V_{GS\_ON} - V_{PLATEAU}}$
t_4 V_{gate} rise	Gate voltage increases to final level, further reducing the channel resistance
t_5 Turn-off delay	Driver voltage drops to zero, V_{gate} starts to reduce towards the plateau level. Voltage drop slightly increases due to higher channel resistance. $t_{delay,off} = R_G \cdot C_{ISS} \cdot \ln\left(\frac{V_{GS\_ON}}{V_{PLATEAU}}\right)$
t_6 Voltage rise	Device enters saturation region, building up voltage Gate voltage constant at plateau level due to C_{gd} charging. $t_{voltage,rise} = \frac{Q_{GD} \cdot R_G}{V_{PLATEAU}}$
t_7 Current fall	Device takes all DC-link voltage, allowing diode to be forward biased. Current transference to the diode. $t_{current,fall} = R_G \cdot C_{ISS} \cdot \ln\left(\frac{V_{PLATEAU}}{V_{TH}}\right)$
t_8 V_{gate} fall	V_{gate} continues to drop towards zero, as C_{ISS} is being totally discharged.

3.1.4.2. Influence of parasitic elements

The switching cell employed in the investigation of the switching energy is in fact a rather complex association of several parasitic elements, which have a significant influence on the measured commutation waveforms. Besides the devices parasitic capacitances and case inductances, the commutation path inductance, ESL from DC-link capacitors and finally inductor winding capacitance also play a key role in explaining some differences between theoretical and measured waveforms.

Regarding the turn-on transient, the initial voltage drop observed during the current rise is an effect of the case inductances from the switch (and not from the whole commutation circuit, as normally assumed). Meanwhile, the current peak is not only justified by the diode capacitive charge but also by the inductor winding capacitance. The Miller Plateau cannot be in this case clearly observed, firstly because of the already referred unclear saturation limit and also due to oscillations triggered by the transient.



Power

Fig. 45: Turn-on transient for the SiC-MOSFET at 550V/40A/25°C.

Concerning the turn-off waveforms as depicted below, the initial current drop before the voltage across the switch reaches the DC-link value (directly polarizing the diode) is cause by the discharge of the capacitances from the diode and inductor windings. The voltage peak shortly after the transient is on the other hand mainly caused by the inductances of the switch case, superimposed by some oscillations.

Tests were also performed with different values of inductance on the commutation path. For all tested configurations, the dv/dt remained as expected the same, as it is rather dependent on the device capacitances and driver configuration, which were not affected. On the other hand, the increased inductance of the third tested configuration resulted in a clear decrease of di/dt for both transients, also followed by smaller oscillations. In this case, the overall losses were increased by approximately 12%.

As a conclusion, it is therefore of significant importance to have an overall low inductance on the commutation path, not only to enable faster speeds (with lower oscillations) but also to avoid high voltage transient with enough energy to trigger an avalanche as was discussed in [3]. Solutions like placing a high voltage ceramic capacitor right near the commutation path inside the module are among the best and most simple ones [30].

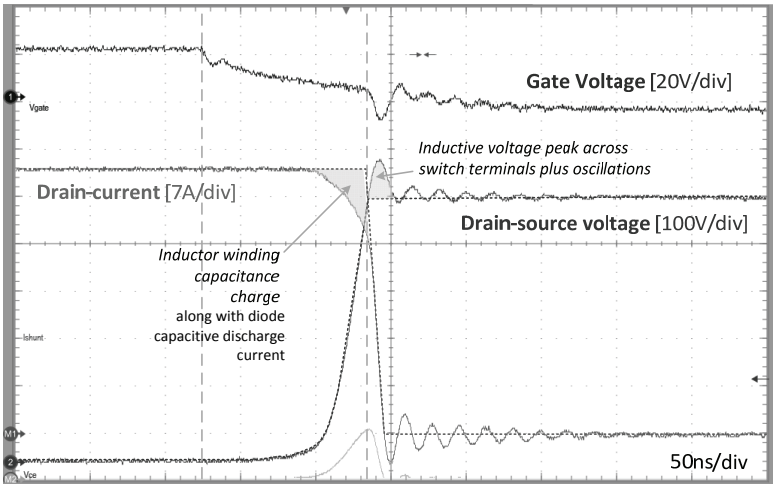


Fig. 46: Turn-off transient for the SiC-MOSFET at 550V/40A/25°C.

3.1.4.3. Measuring procedure

One key aspect of the current investigation is the consideration of the switching speed in the measurement of the switching losses. The classic limits of 90% and 10% used on the measurements of the switching speed were nevertheless not applied here. Of interest here are the maximum values, as they are the ones with the highest impact on the electromagnetic activity and parasitic coupling in the circuit. In the picture below is exemplified the dependence between the selected lower limit and the actual measured slope for an IGBT current waveform. After a

local maximum, the value decreases again when going in the direction of 10% of the reference curve. The maximum slope was therefore always checked for the entire transient during the here performed tests, considering a minimum time resolution of 1ns.

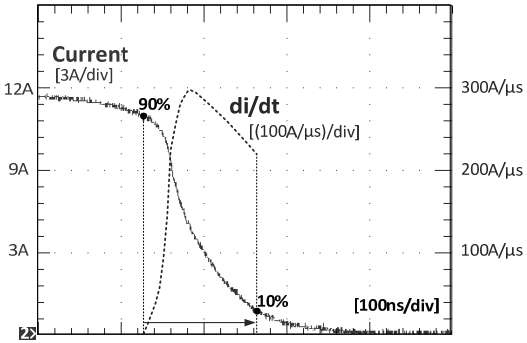
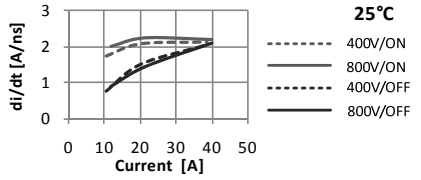
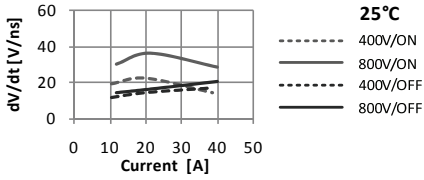
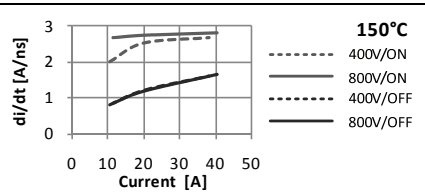
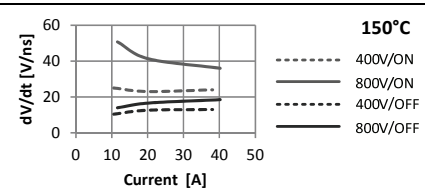


Fig. 47: Example of the variation on the di/dt value depending on the selected limits [66].

As presented in Fig. 39, the first step in the investigation of the switching losses was therefore finding the conditions (voltage, current and temperature) under which the device operated with the highest speed. An example of such "mapping" is presented below for the 1200V SiC-MOSFET from CREE.

Table 5 – Mapping of switching speed behavior for CREE 1200V SiC MOSFET with external 20A 1200V SiC diode with 20V/-5V gate voltage, 15Ω at turn-off, 6Ω (equivalent) at turn-on for different temperature, voltage and current levels

di/dt	dv/dt
	
	

By identifying the conditions where maximum speed is achieved, it was later possible to configure the driving circuit in order to not surpass selected speed limits. Taking in consideration the present technology regarding discrete/module packing and driving circuitry, the maximum di/dt and dv/dt were respectively limited to 2A/ns and 50V/ns. A more detailed discussion about these limits will be presented in the item 4.1.

3.1.5. Operation at higher speeds

Considering that the considered switching speed limits are not absolute, further investigations were performed here in order to present a prospect of possible gains regarding operation at higher speeds.

For such purpose, another new switching cell was designed and constructed with the single purpose of reducing as much as possible the commutation loop inductance. The original value was reduced to approximately 45nH by placing the devices much nearer to each other, cutting the device legs to a minimum and finally adding several high voltage ceramic capacitors near the commutation circuit.

The di/dt can for instance be separately controlled by means of the placing an additional capacitance between the gate and source. An explanation for this is the fact that the current slew rate depends on the device transconductance (g_{FS}) and on the gate voltage slew rate (dV_{GE}/dt), as given in the equation below.

$$dI_D / dt = g_{FS}(I_D) \cdot dV_{GS} / dt \quad (14)$$

The slew rate of the voltage remains on the other hand practically unaffected [33] as the gate voltage remains approximately constant (Miller Plateau) due to the changing value of C_{gd}. Such effect can be observed in the waveforms in Fig. 48 and Fig. 49, with the dv/dt remaining practically unaffected for both transients. Despite significantly reducing the di/dt at turn-on, the amplitude of the oscillations on the current was in fact increased. Meanwhile, the capacitance had as expected a minor effect on the turn-off transient (which is more dependent on the diode).

Because of rather reduced effect on the turn-off transient and also increased oscillations, the speed with different gate capacitances was not further investigated here. Of interest here was also to observe the behavior of the device at speeds higher than the previously established limits. The measured waveforms for turn-off are presented in Fig. 50 with the diverse values of gate resistor values.

At very low speeds, the current presents a small "tail" (not to be confused with carrier recombination effect) while the voltage takes more than 70ns to rise.

Reducing the gate resistor significantly affects the voltage steepness, while the current commutates with less delay. At the minimum measured gate resistor, both waveforms presented significant amount of oscillations, with amplitudes respectively equal to 20A and 200V. As was already discussed, the initial current drop representing the discharge current of the inductor winding capacitances becomes more accentuated, with a value over 20A at maximum speed.

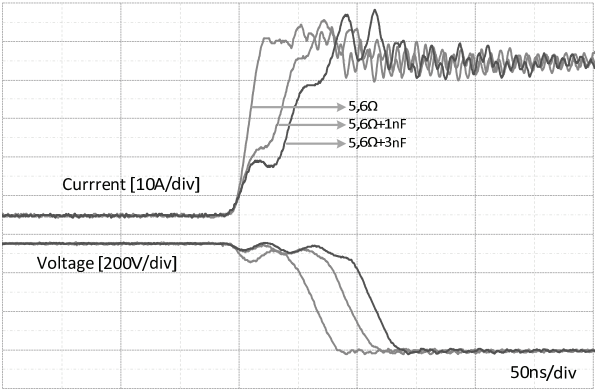


Fig. 48: Turn-on for the SiC-MOSFET at 550V/40A/25°C, R_g=5,6Ω, with different gate-source capacitances.

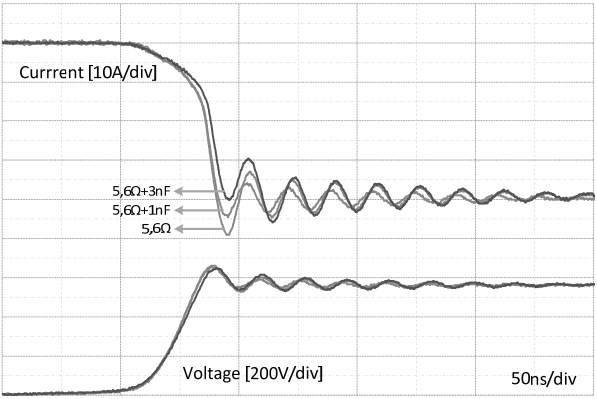


Fig. 49: Turn-off for the SiC-MOSFET at 550V/40A/25°C, R_g=5,6Ω, with different gate-source capacitances.

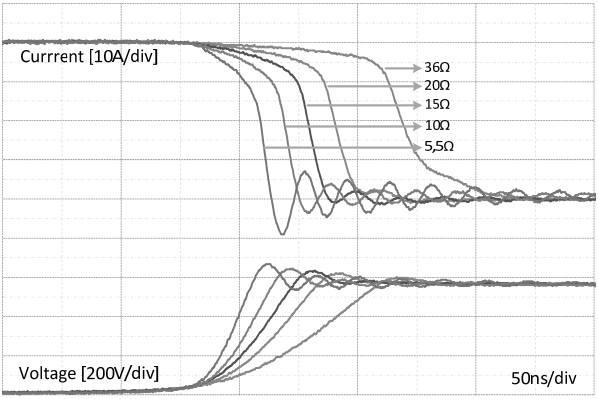


Fig. 50: Experimental turn-off waveforms for the SiC-MOSFET at 550V/40A/25°C with different gate resistor values.

Concerning the turn-on transient with external diode, it is interesting to observe here that despite the increasing current slope; the current peak was not increased (but rather reduced) given the fact that capacitive discharge process of the Schottky diode does not depend on the di/dt. The amount of high frequency oscillations in both waveforms at higher speeds showed practically no increase. With increasing values of di/dt it also becomes possible to notice a very small inductive voltage drop across the voltage, shortly before the commutation, which at higher speeds is superimposed by oscillations.

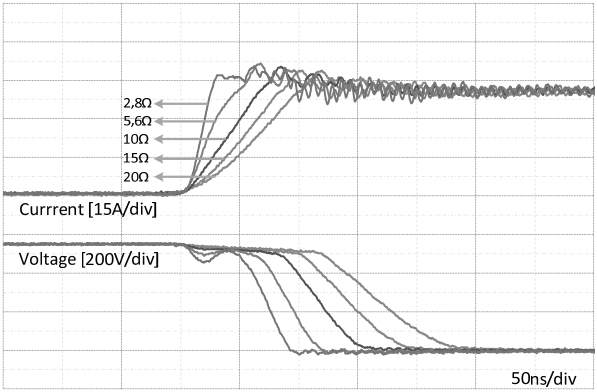


Fig. 51: Experimental turn-on waveforms for the SiC-MOSFET at 550V/40A/25°C with different gate resistor values and with external SiC diode (C2D20120)

When the turn-on takes place with the device intrinsic diode, it is possible to observe two clear differences. Firstly, the current peak at turn-on tends to increase with higher speeds likewise happens with Si PN diodes. The observed levels and discharge times are nevertheless much smaller given the smaller thickness and higher doping concentration of the epilayer, resulting in lower lifetimes.

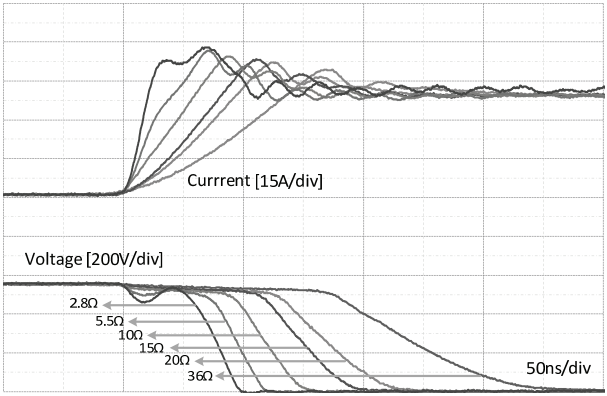


Fig. 52: Experimental turn-on waveforms for the SiC-MOSFET at 550V/40A/25°C with different gate resistor values and with intrinsic diode.

In addition to this as was pointed out in [46] and [47], the recovery charge has very little dependence on the current value and also on the temperature. The second major difference is that the oscillations on the current waveform have lower frequency (approximately 60 MHz in comparison with previous 240 MHz). Meanwhile the voltage waveform behavior remains practically the same.

In Fig. 53 are plotted the speed values as a function of the measured losses for both turn-off and turn-on transients, with the last one being performed with either an external SiC Schottky diode or with the device intrinsic PN diode.

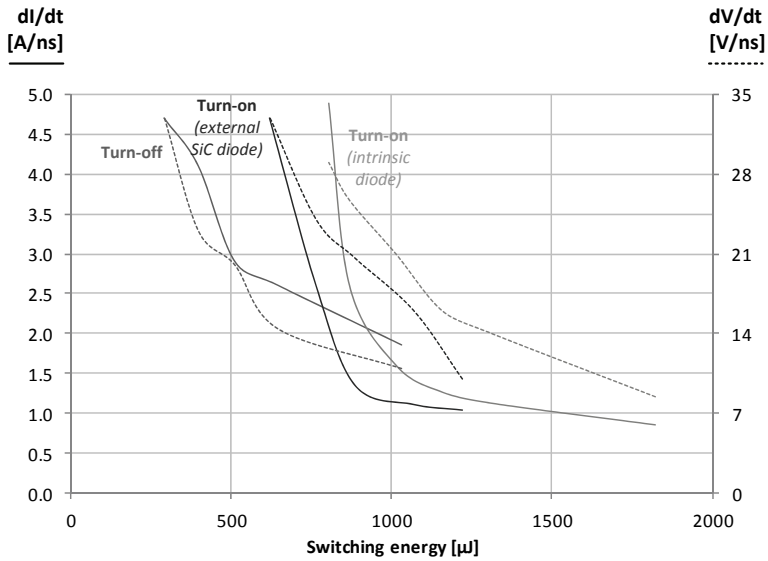


Fig. 53: Trade-off between speed and losses for the SiC MOSFET measured at 550V/40A/25°C.

From these results it is possible to draw some conclusions, as follows.

- In the direction towards higher steepness for both current and voltage, the possible reduction of the losses becomes less significant from a certain point. This is justified by the increasing influence of parasitic elements on the switching transient (overvoltage at turn-off and peak current at turn-on) and also limiting effect of the internal gate resistance.
- The above referred limitation is especially clear when operating with the device intrinsic diode, as above approximately 2A/ns further reduction of the losses is only obtained with a sharp increase on the di/dt value. Reason for this is the significant dependence of the current peak amplitude to the di/dt. Such peak is also responsible for practically shifting the switching losses to higher levels in comparison to operation with an external Schottky diode.
- The presented behavior is in the end strongly affected by the layout parasitic elements and may be shifted to higher levels when considering a power module with very low inductance of the commutation path.

Another conclusion in part coming from the two last points above is that despite switching with practically the same speed; the turn-on losses are still more than

two times larger than the turn-off losses. Such relation is in fact valid not only for the MOSFET but also for practically all investigated SiC switches. In order to better observe such relation, the turn-on waveforms were horizontally inverted and superimposed to the ones from the deactivation, as presented below.

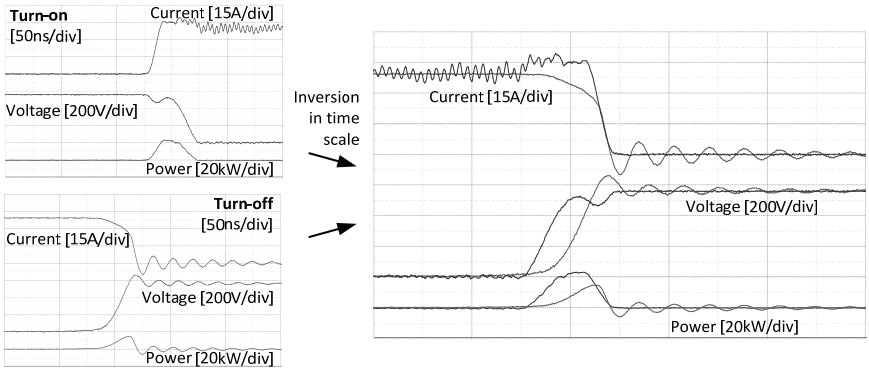


Fig. 54: Superposition of turn-on and turn-off (horizontally inverted) waveforms for the SiC MOSFET operating at 550V/40A, 25°C.

One can firstly observe the higher amount of oscillations at turn-off, mainly because of the strong current transient towards zero that excites resonant tanks in the board elements. In addition to this, with both current waveforms aligned, it is also possible to notice a certain delay on the turn-on voltage in comparison with the turn-off component. Such time difference is introduced by the fact that before blocking, the freewheeling diode needs to fully discharge either the injected minority carriers or the capacitive charge for respectively a bipolar (PiN) or unipolar (Schottky) structure. Another important difference leading to lower losses on the deactivation is the initial reduction of the current while the voltage is rising, due to the inductor winding capacitance and diode capacitance charging. Such significant difference between the turn-on and turn-off losses serves as an indication for a possible interesting operation in order to reduce switching losses, namely the at higher current ripple, as will be later investigated.

3.2. Benchmarking of investigated devices

A multitude of figures of merits (FOM) can be employed in the comparison of different device technologies, taking performance or constructive parameters as main factors in the calculation. A brief overview of then is presented below.

Table 6 – Overview of key-parameters and FOMs used in the comparison of semiconductor devices.

Property/ FOM	**Explanation**	**Observations / Critic**
Specific chip resistance	Most common factor, relates the required chip area in order to attain a certain static performance.	Chip area is not necessarily a precise indicator of device cost, as not only the substrate but also the involved production processes/steps and attained yield (depending on defect density) may significantly affect the final cost. Values are most commonly given at room temperature, what rarely corresponds to application conditions. The temperature dependence is also not considered. Most values found in the literature apply to experimental chips with a very small footprint. In the case of larger chips for real applications, the resultant value may increase due to unequal current distribution on the chip. It is often not clear if either the dye or active area is considered
E_{off}/A x Vsat	Most commonly employed in the comparison of IGBTs, with the normalized switching energy multiplied by the saturation voltage at nominal current.	Turn-on is not frequently considered, as it rather serves an indication of the freewheeling diode performance In the case of the application of reverse-recovery free Schottky diodes, turn-on losses shall also be considered No clear rule of under which values these losses need to be considered and how the normalization (if applicable) shall be performed.
Resistance x Gate	Taking the device absolute resistance and gate charge, an	Commonly employed when comparing low voltage FETs operating at very high switching frequencies. Gate charge may

Charge	indication of static and dynamic performance is attained.	serve as an indication of achievable driving speed.
Current density x voltage drop [85]	Under maximum specific power dissipation limit (300W/cm2) [85], the attainable current density and resultant voltage drop are plotted against each other.	Especially interesting when comparing bipolar and unipolar devices, enabling to trace from which point a certain technology may be more attractive.

The here proposed approach is based on the measured device resistance at high temperature to normalize performance parameters like switching and driving losses. Some points of comparison are firstly presented in the items below.

3.2.1. Static behavior and temperature dependence

As was already discussed before, the device resistance under higher levels of temperature is of more interest when considering practical applications. In addition to this, the highest chip utilization is obtained under the condition of maximum loss density which in turn implies on maximum junction temperature. Therefore the values of the specific resistance at 25°C and 150°C are presented in the graph below for the investigated devices. Here was considered the total chip area instead of only the active area, as the first one serves as a better indicator for the expenditure with SiC substrate.

As expected at the top is the CoolMOS with the highest chip resistance, followed by the Si-IGBT. Right below are all 1700V-rated devices, with the JFET from Semisouth being the one with lowest value among then.

Regarding the 1200V devices, the CREE MOSFET and Infineon JFET displayed similar values of specific chip resistance at high temperature, while the enhancement mode Semisouth JFET has a value roughly 40% smaller. The Transic BJT offered a further reduction of 20%, followed by depletion mode JFET from Semisouth which had the lowest specific resistance among all investigated devices. As already stated in the Table 6, one shall nevertheless not consider the obtained results as an absolute and definitive indication about the technology specific costs,

given other dependencies like involved production processes/steps and attained yield.

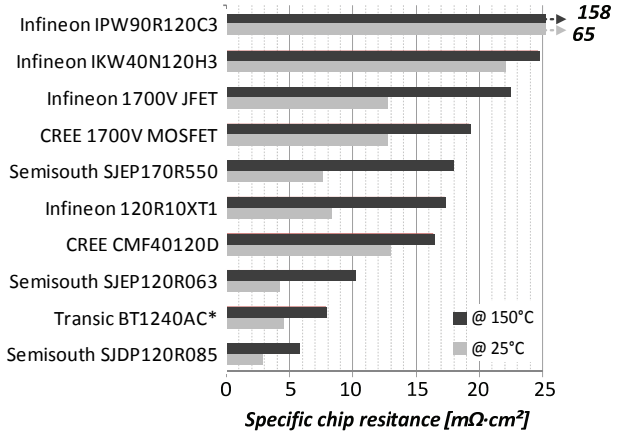


Fig. 55: Specific chip resistance for different junction temperature levels.

Also interesting to consider here is the dependence of the specific resistance to the temperature, as depicted below, for a temperature change of 125K.

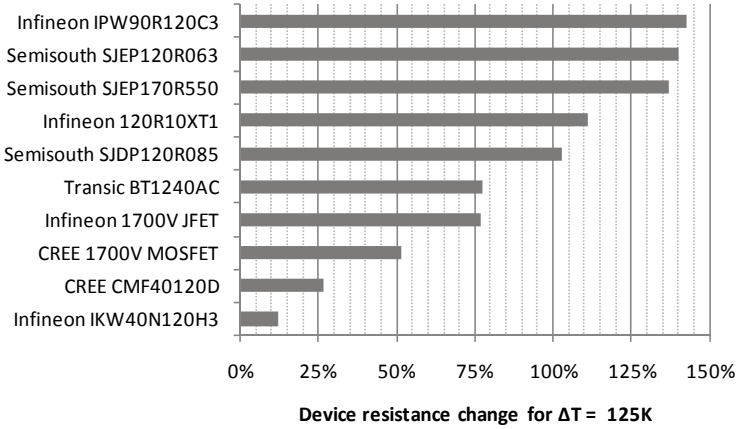


Fig. 56: Temperature dependence of the device resistance.

The well-known high temperature dependence of the RDSON for Si-MOSFETs is also valid for the Superjunction device, placed on the top of the list. The two following devices with very similar coefficients are the enhancement-mode JFETs

from Semisouth. Depletion-mode JFETs from Semisouth and Infineon rated at 1200V had showed slightly lower temperature dependence, but still beyond 100%.

Due to the very low level of conductivity modulation on the Transic BJT, a rather high temperature dependence could be observed, with a similar value also valid for the 1700V JFET from Infineon. The MOSFETs from CREE had the lowest temperature dependence factors among all SiC investigated devices, with the 1200V-rated device having an increase on the device resistance of just 27% for a temperature increase of 125°C. At the bottom of the list is the Si-IGBT that due to the conductivity modulation has a low temperature dependence.

3.2.2. Dynamic behavior

The graphics below present the absolute value of the switching energy for a given voltage level plotted against the current for the tested devices.

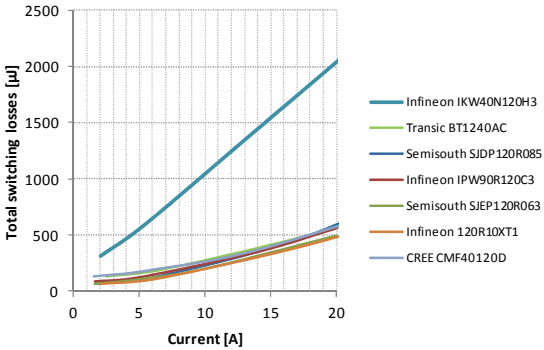


Fig. 57: Switching energy at 150°C and 550V for 900V and 1200V rated devices.

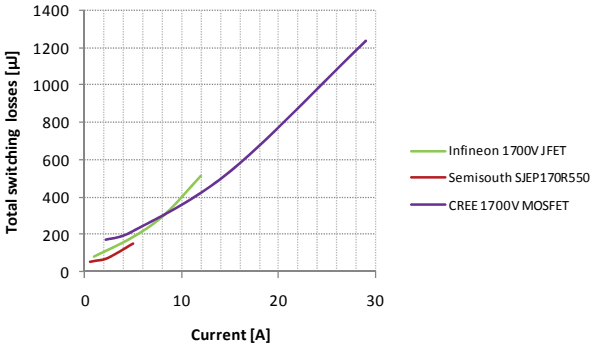


Fig. 58: Switching energy at 150°C and 780V for 1700V rated devices.

From these results it is possible to observe that most of the investigated devices present a rather similar amount of total switching losses, with the SiC MOSFET and BJT having slightly higher losses (approximately 15%) than the JFETs. Such result was in turn expected given the fact that similar limits for di/dt and dv/dt were selected when measuring the losses. From the performed switching speed investigation, practically all devices reached the established di/dt limit of 2A/ns before the dv/dt limit of 50V/ns, with only three exceptions. The first one was the 1700V JFET, which for turn-off reached 51V/ns with 1,51A/ns. Meanwhile the turn-off speed could reach neither of the established limits for the Transic BJT and Si-IGBT IWK40N120H3.

3.2.3. Performance benchmarking

The so far presented comparison of the switching energy is nevertheless not entirely valid given the very diverse values of chip resistance. In order to enable a better assertion of each technology performance, an especial approach is here proposed considering real application conditions.

The first step consists on assuming a total chip area value ($A_{chip\_reference}$) used as reference, either arbitrarily chosen or based on the value of a reference device. The amount of chips in parallel for the analyzed device (n_{chips}) can now be calculated, considering each individual value of chip area (A_{chip_device}).

$$n_{chips} = \frac{A_{chip\_reference}}{A_{chip\_device}} \tag{15}$$

Afterwards the switching losses ($E_{sw\text{-}scale}$) are scaled based on measurement values (E_{sw_single}), considering the amount of chips and switched current level (I_{sw}).

$$E_{sw\_scale}(I_{sw}) = n_{chips} \cdot E_{sw\_single}\left(\frac{I_{sw}}{n_{chips}}\right) \tag{16}$$

Now the maximum attainable switching frequency for a given current stress level is calculated. The value is obtained by calculating the difference between the maximum chip losses and level of conduction losses and then dividing by the switching energy. Here is considered the operation with a certain value of duty cycle (D).

$$f_{sw\_max}(I_{sw}) = \frac{\left(P_{max} \cdot n_{chips} - \frac{R_{dson}}{n_{chips}} \cdot {I_{sw}}^2 \cdot D\right)}{E_{sw\_scale}(I_{sw})} \tag{17}$$

The plot for the 1200V devices taking the chip area of the 900V CoolMOS as reference is presented below, considering a nominal peak current of 35A, duty cycle of 50%, 150°C junction temperature and 100°C case temperature.

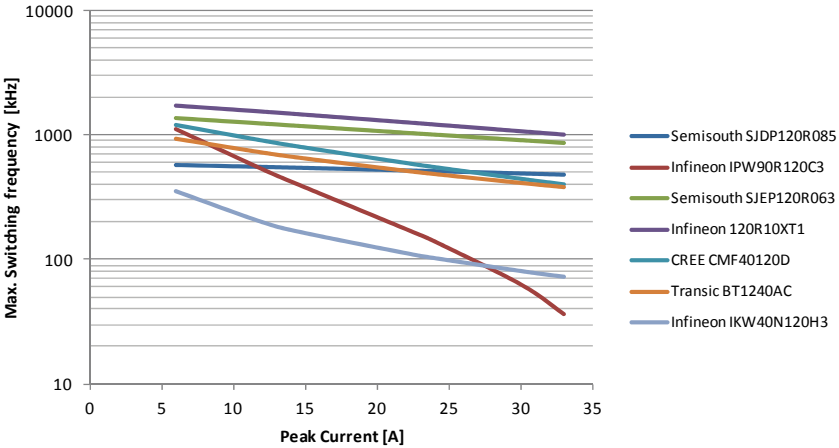


Fig. 59: Maximum attainable switching frequency for different current levels.

Switching frequency levels above 1 MHz are theoretically achievable with the scaled value of chip area. For the reference device (CoolMOs) the dominant conduction losses explain the steep reduction of the achievable switching frequency in comparison with other devices. Owning their high switching losses, the Si-IGBT can in contrast be found in the bottom of the graph.

Concerning the SiC devices, the best performance could be observed for the SJEP120R063 and 120R10XT1. Meanwhile, a clear offset in the direction of lower frequencies can be observed for the SJDP120R085. A reason for this was the very diminutive chip area of the referred device, leading to a high amount of chips in parallel and thus to higher switching losses. The increased steepness for the MOSFET and BJT can in turn be explained by their higher switching losses at higher current levels, as was presented in Fig. 57.

A comparison between the 1700V devices with the above presented methodology is not presented here, mainly due to the very different current ratings that would require a rather extreme scaling of the amount of chips.

3.2.4. Benchmarking considering maximum achievable switching speed

The presented benchmarking of technologies was performed assuming commutation losses measured under switching speeds currently observed at power applications. The attractiveness of increasing the speed levels was nevertheless observed (and demonstrated for the SiC-MOSFET) with the prospect of further reducing losses and hence either increasing the chip utilization or enabling higher switching frequencies.

Benchmarking different devices considering much higher speed levels is nevertheless problematic. Reason for this is the still significant impact of current packaging technology (especially concerning discrete construction) along with board design on the obtained trade-off between speed, overvoltage and losses. As a consequence, the device performance can be in part overshadowed by the periphery characteristics.

New advances in packing might on the other hand enable a significant reduction of parasitic elements that limit the switching speed at device level, as will be discussed in the item 4.1. In order to consider such developments, a benchmarking concerning the driving speed capabilities of the investigated technologies rated at 1200V with focus on intrinsic characteristics is proposed here.

In fact a multitude of "figure of merits" with the above referred objective can be found in the literature. The Baliga Figure of Merit (BFOM) [293] takes in consideration the device specific resistance and input capacitance. Problematic here is that what is considered is not the influence of the input capacitance on the switching losses, but rather on the driving losses. In contrast, the output capacitance is considered in [294] as the main device parameter affecting the switching losses, especially considering higher voltage ratings.

While the device capacitances do affect the switching performance, their strong dependence on voltage level makes a fair comparison among devices a difficult task. In order to deal with such drawback, in [295] was proposed the use of the gate charge values instead. From the overview of switching waveforms in the item 3.1.4.1, it is possible to assert the following relations.

$$t_{rise\_current} = \frac{Q_{GS}^{*}}{i_{gate}} \quad \text{and} \quad t_{fall\_voltage} = \frac{Q_{GD}}{i_{gate}} \tag{18}$$

In other words, the switching times are directly proportional to the charge values and available gate current. Q_{GS}* represents the part of Q_{GS} measured after the gate voltage reaches the threshold voltage, i.e. without considering the delay time

(where no losses take place). Meanwhile, the gate current depends not only on the driver voltage but also on values of the plateau voltage and threshold (as presented in Table 4). Finally, the gate resistance (either extern or intern) serves as a limitation to the resultant gate driving current.

Important to observe at this stage is the opposite relation of the device resistance and charge values with the chip area, i.e. larger chip areas lead to smaller resistance but higher capacitance and vice versa. It is therefore necessary to not only work with specific values but also take in consideration the influence of the chip area on the device performance. For such purpose, the overall device losses (conduction and switching) can be calculated with the following equation. I_{RMS} represents the RMS current across the device, V_D and I_D the switched current values and f_{sw} the switching frequency. To simplify matters, the influence of discharge of the diode capacitance is not being considered here, so that both turn-on and turn-off losses can be directly inferred by the switched voltage and current values multiplied with the switching times.

$$P_{LOSS} = I_{RMS}^{\ 2} \cdot R_{ON} + V_D \cdot I_D \cdot (t_{rise\_current} + t_{fall\_voltage}) \cdot f_{sw} \tag{19}$$

Substituting the rise and fall-times result in the following equation.

$$P_{LOSS} = I_{RMS}^{\ 2} \cdot R_{ON} + V_D \cdot I_D \cdot (\frac{Q_{GS}{}^* + Q_{GD}}{i_{gate}}) \cdot f_{sw} \tag{20}$$

Working with the specific values of chip resistance (R_{ON_sp}) and charge values (Q_{GS_sp}, Q_{GD_sp}) results in the equation below.

$$P_{LOSS} = I_{RMS}^{\ 2} \cdot \frac{R_{ON\_sp}}{A_{chip}} + V_D \cdot I_D \cdot (\frac{Q_{GS\_sp}{}^* + Q_{GD\_sp}}{i_{gate}} \cdot A_{chip}) \cdot f_{sw} \tag{21}$$

The minimum losses can be obtained by considering the derivate dP_{loss}/dA equal to zero. This yields the optimal area with the following equation.

$$A_{opt} = \frac{I_{RMS}}{\sqrt{\frac{V_D \cdot I_D \cdot f_{sw}}{i_{gate}}}} \cdot \sqrt{\frac{R_{on\_sp}}{\left(Q_{GS\_sp}{}^* + Q_{GD\_sp}\right)}} \tag{22}$$

A performance factor can therefore now be defined as follows. The smaller the value, the smaller is the optimal chip area to obtain minimum losses.

$$FOM = \sqrt{\frac{R_{on\_sp}}{\left(Q_{GS\_sp}{}^* + Q_{GD\_sp}\right)}} \tag{23}$$

The FOM is now calculated for the investigated SiC devices, with results presented in the graph below.

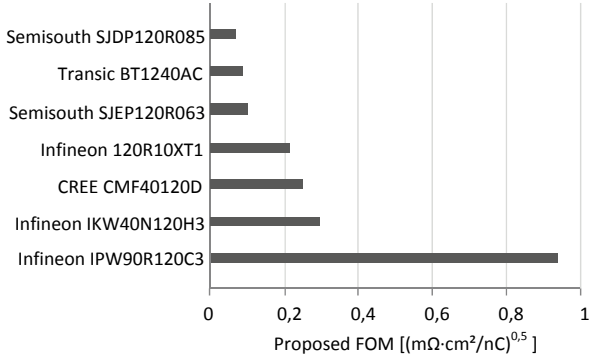


Fig. 60: FOM for tested power devices.

From the obtained results it is possible to assert that the devices having the lowest specific values of chip resistance have in the end also the smaller values of charge (given the smaller chip area), being therefore from the perspective of switching performance also the favorite devices.

Another fact to be considered regarding the dynamic performance is the value of the intrinsic gate resistance, which depends not only on the device technology but also on the chip size. Taking the values measured with open drain/collector at 1 MHz and dividing then by the maximum current loading (assuming junction and case temperature respectively equal to 150°C and 100°C) results in the graph below.

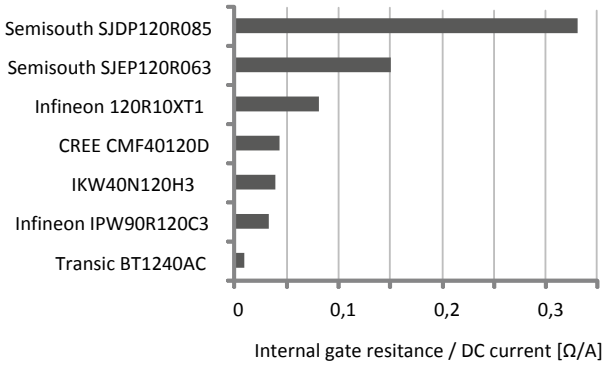


Fig. 61: Internal gate resistance divided by maximum DC current [Ω/A].

The Semisouth devices showed a high value of intrinsic gate resistance in comparison with other SiC devices. Meanwhile, the BJT presented one of the lowest ones, indicating that in the direction towards higher switching speeds, it is possible to perform a faster switching transient with less driving voltage levels.

3.2.5. Driving issues

Practically all the investigated devices require bipolar driving voltage for reliable operation given the low threshold voltage values. An overview of the driving voltage levels applied during this investigation along with others found in the literature is presented below. In case higher switching speed is targeted, then even higher driving voltage levels for some devices (JFETs and BJT) might be applicable.

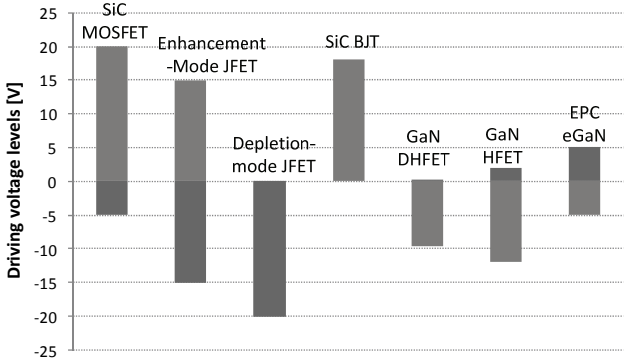


Fig. 62: Driving voltage levels for different device structures [240], [283].

Despite requiring only a single voltage level, depletion-mode JFETs may in the end also require complex driving circuits given the cascode associations required to attain reliable operation.

3.2.6. Freewheeling-related issues

An important issue concerning the application of the devices in bridge circuits is the freewheeling capability, which is in affected by two device characteristics, namely: existence of intrinsic PiN-SiC diode between power terminals (drain-source for unipolar devices) and bidirectional conduction capability.

The existence of the intrinsic PiN diode with the device has been so far focus of much discussion. One disadvantage is that these diodes do display reverse recovery, increasing the switching losses (with an inherent the di/dt coupling),

though the stored charge is much lower than the one observed in Si-bipolar diodes. Below are presented the measured losses at the first pulse for the investigated diodes (external and intrinsic) as a function of the switching voltage and at a temperature of 25°C. From this graph it becomes clear that the intrinsic PN diodes do result in an increase of the switching losses when compared with their Schottky discrete counterparts. In case of very high levels of switching frequency, one simple solution might therefore be simply bypassing the intrinsic diode with an Schottky-SiC diode given the higher voltage drop of the first one (around 2V because of wider band gap).

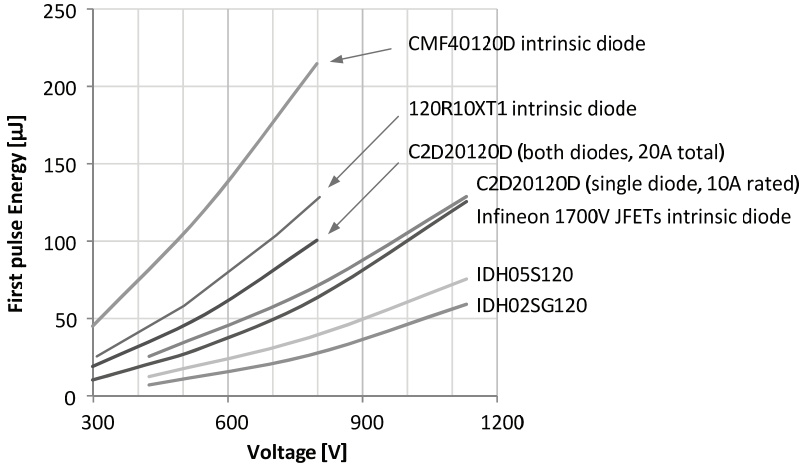


Fig. 63: First pulse energy for different freewheeling diodes as a function of the voltage.

Another interesting capability is the bidirectional current conduction, allowing the device to operate in the so-called synchronous rectification mode. Hence after antiparallel diode (either intrinsic or external) commutates, the device can be activated again and the current will be shared between the channel and diode, significantly reducing the conduction losses. This also opens the possibility of reducing the current-rating of the antiparallel diodes (in case of external) and hence sparing costs.

The two referred capabilities are summarized in the table below.

Table 7 – Overview regarding possible use of intrinsic diode and bidirectional conduction.

Manufacturer	**Device #**	**Intrinsic diode**	**Bidirectional conduction**
CREE	CMF40120D	✓	✓
	1700V MOSFET	✓	✓
Transic	BT1240AC		
Infineon/SiCED	IPW90R120C3	✓	✓
	IKW40N120H3		
	120R10XT1	✓	✓
	1700V JFET	✓	✓
Semisouth	SJDP120R085		✓
	SJEP120R063		✓
	SJEP170R550		✓

4 Application of WBG devices: switching frequency and passive filter elements

The first and perhaps most interesting prospects attained with WBG devices analyzed here is the possible reduction of the switching energy what directly implies on the possibility of operating at higher frequencies without prejudice to the overall efficiency. Such potential is presented in the graph below, where the relative reduction on the switching energy is plotted against the possible increase in the switching frequency, assuming a constant level of losses. At 50% reduction, the frequency can be doubled, while for higher levels of reduction, increasingly higher levels can be attained.

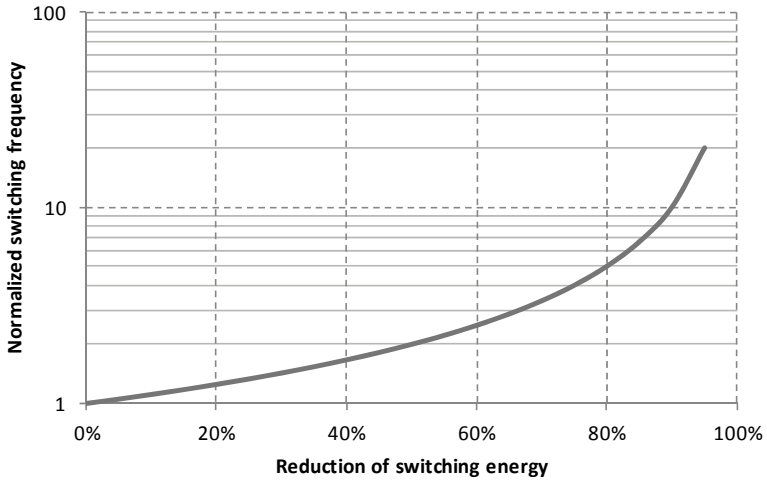


Fig. 64: Reduction of switching energy and attainable increase on the switching frequency.

Such low level of switching energy is mainly achieved by the fact that either no (unipolar structure) or very low level (bipolar structure) of conductivity modulation is employed. The losses are therefore mainly dependent on the switching times, which in turn are influenced by device parasitic capacitances, driver configuration and board parasitic components. Operation at very high speeds also brings several

challenges at board and system levels, as will be discussed in details in the item 4.1.

The primary objective behind the referred increase of switching frequency is the reduction of expenditure with passive filtering elements. For the considered applications in renewable energy systems, main focus is given to output AC filters, inductors for DC-DC converters and finally high frequency transformers for galvanic isolation. Issues related to the design and operation along with technological limits will be identified in the item 4.2. A direct consequence of reducing the size of passive elements is increasing the power density. It becomes therefore possible to either reduce the expenditure with casing (accounting for as much as 20% of overall costs in photovoltaic converters) or increasing the power rating (given proper thermal management of the losses). These issues will be jointly considered in Chapter 7.

4.1.Switching speed and related issues

The level of losses attained with WBG devices is mainly dependent on how fast the switching transient takes place. One first issue to be discussed here are the side effects arising from these fast transients on the circuit and system operation, finally followed by a detailed investigation on possible effects of the operation at higher switching frequency on the conduction losses.

4.1.1. Critical aspects

High switching speeds shall be considered not only as a possibility but rather as a necessity in order to reduce the switching energy and thus enable higher current loading for a given device. Such high speed levels are nevertheless inherently complex to be mastered, especially when considering power applications with several aspects directly and indirectly affected as summarized in the picture below.

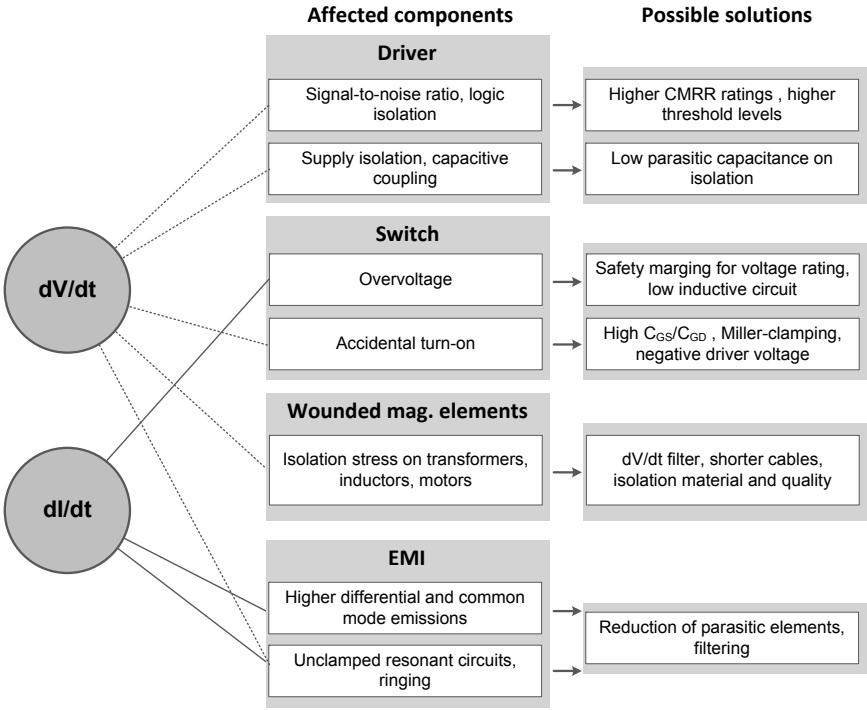


Fig. 65: Overview of affected components by fast switching speed and possible solutions.

4.1.1.1. Driving circuit

The first system component considered here is the driving circuit, especially in the case of high-side switches requiring full isolation of signal and supply. The dv/dt plays in this case the most important role given the generated parasitic currents due to the capacitive coupling with effects like incorrect signal transmission, driver latching (possibly leading to system failure) [34] and overheating/aging. Possible solutions in this case are the use of isolating devices with increased common-mode-rejection ratio and also higher signal-to-noise ratio which can be obtained with higher threshold voltage levels. On the other hand, in case the high-side switch cannot be supplied by a simple boot-strap circuitry, the isolated power supply must be constructed with low winding parasitic capacitance.

4.1.1.2. Switch

The second item is the switch itself as the overvoltage at turn-off is strongly affected by the di/dt. In order to ensure reliable operation, a safety margin to the breakdown voltage needs to be considered in order to cover possible changes on the current steepness under different operating conditions. A general limit is normally hard to be determined and strongly depends on the parasitic inductance of the commutation path. Below are presented as an example the overvoltage values for limits of 2 and 5A/ns as a function of the commutation path inductances.

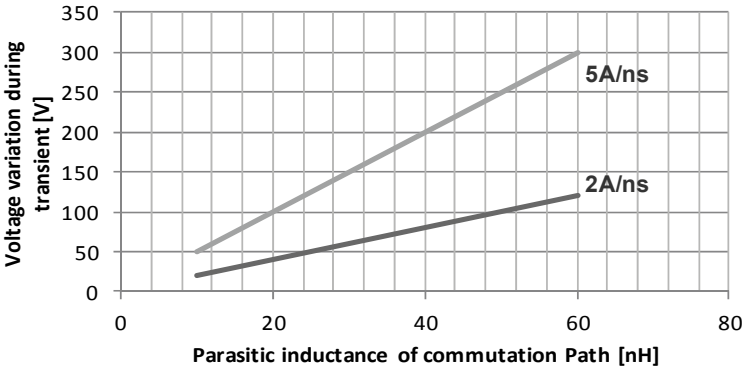


Fig. 66: Overvoltage at commutation for a switching transient at 2A/ns as a function of commutation path stray inductance.

Another case to be considered are bridge-circuits (or similar configurations) operating under high dv/dt values. The sudden voltage change across the capacitances of the high-side device results in a current that may charge the Gate-source capacitance (in case of higher impendence of the driving circuit) resulting in a parasitic drift of the gate voltage. In case of surpassing the threshold limit, the high side devices enters in partial conduction and a peak current is added to the commutation value, increasing the switching losses [31] or under certain conditions even resulting in bridge short-circuit. It is therefore preferable to work with devices with higher values of C_{GS}/C_{GD}, as these will be less susceptible to accidental turn-on [34], [35]. Other measures include adding a miller clamping circuitry to directly short-circuit gate and source while the device remains deactivated. This way, a low impendence path for the charging currents of C_{GD} is provided, avoiding any voltage built-up across C_{GS}. Increasing the difference between the deactivation voltage and device threshold limit will also lead to higher reliability [38]. In the case of normally-off devices, negative gate voltage for deactivation can be employed, while for normally-on such effect can be attained by

further reducing the negative level. Finally, ferrite beads can be employed on the gate path in order to suppress spikes at high dv/dt [36].

4.1.1.3. Wound magnetic elements

The third aspect is related to the isolation stress of windings of magnetic components like inductors, motors and transformers under high dv/dt values. It becomes especially critical in association with long cable lengths possibly leading to voltage reflection phenomenon and thus resulting in even higher overvoltages. In addition to this, the fast voltage transients may cause partial discharge (corona inception), affecting the lifetime of the isolation. Possible solutions are reduction of cable length, placement of a dv/dt filter (with effect depicted below) along with application of suitable classes of isolating materials. As an interesting remark, the CSI (current-source inverter) is more suitable for driving machines at high switching speeds because there are no output voltage transients across the windings [37].

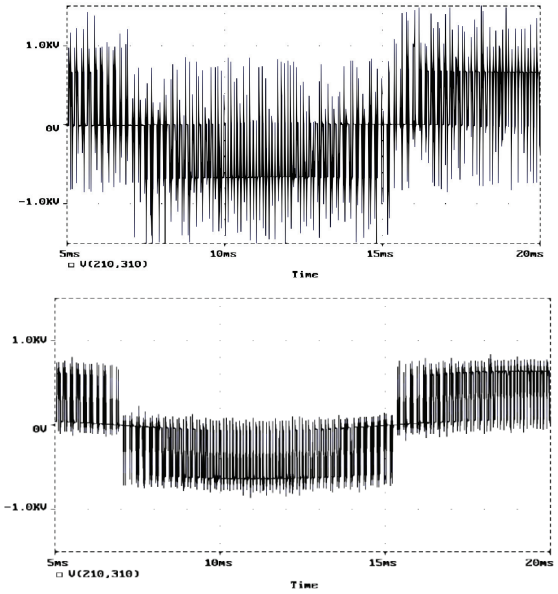


Fig. 67: Voltage across motor windings without (left) and with (right) dv/dt filter [Source: Intec Solutions].

4.1.1.4. EMI

The fourth and perhaps most complex aspect to be considered is the influence of the switching speed on the electromagnetic interference, in form of either conducted or radiated emissions. In this case, it is necessary to observe not only the increased steepness but also the resultant higher levels of oscillations and finally the desired increase of the switching frequency.

On a first step it is necessary to analyze the switch waveforms in details, given the fact they are the main source of disturbances in the circuit. With such objective, the Fourier analysis of the current waveform was performed in order to assert the amplitude and frequency level of aforementioned components.

Assuming a trapezoidal waveform with 50% duty cycle and same values of rise and fall time, the Fourier coefficients normalized to the waveform peak amplitude can be calculated with the following equation [32], where T_{sw} represents the switching period and t_{rise} the rise/fall time. In case of duty cycle values different from 50%, even order components along with others at higher frequency (but with lower amplitude) can also be identified.

$$K_N = \begin{cases} 0, & \text{for n even} \\ \dfrac{2 \cdot T_{sw}}{\pi^2 \cdot n^2 \cdot t_{rise}}, & \text{for n odd} \end{cases} \tag{24}$$

The higher speed has a noticeable effect only for frequency components above 5MHZ, which in turn have relative amplitude smaller than 1%. As was pointed out in [32] such results are also valid for other switching frequencies, given the fact that the coefficients at frequencies above ($1/\pi \cdot t_{rise}$) tend to decrease with a rate of 40db/decade. The same results are also valid for the voltage waveform, given the similar relative values of rise time (considering the here investigated results).

While the above referred analysis procedure provides an overview of expected effects on the frequency spectrum from conducted emissions, it also necessary to remember that current and voltage steepness separately affect the differential and common mode emissions [39], [40]. While the differential mode noise is cause by the magnetic coupling emerging from parasitic loop inductances and the di/dt value, the common-mode noise is generated by the electrical coupling between the parasitic capacitances to ground and the dv/dt value [41], [42]. Consequently, higher steepness leads to a directly proportional increase of both differential and common mode conducted emissions. Meanwhile, higher switching frequencies simply increase the amount of transients per second, also leading to a direct increase of the emissions.

Also critical are unclamped oscillations triggered at the switching transients. The frequency of these oscillations mainly depends on circuit parasitic components like device capacitances and board inductances. In the investigated turn-off waveforms, it was possible to observe high amplitude oscillations at both current and voltage waveforms in range of about 50 MHz. Such frequency approximately matches the switch output capacitance (200pF, at high voltage) and board inductances (approximately 50 nH). Meanwhile, oscillations with much higher frequencies (over 250 MHz) but significantly lower amplitudes were measured in the turn-on.

Finally, it is important to not only consider the frequency but also the amplitude of these oscillations. The dominating factor here is the stored energy on the resonant tank which is in turn influenced by the switching steepness. In the case of turn-on of the switch, the observed current peak due to the capacitive discharge or reverse recovery of the diode stores energy on the commutation path inductances. For a PiN freewheeling diodes (the body diode of a SiC device), higher di/dt values directly result in higher current values so that more energy is stored in the resonant tank what in turn results in higher oscillations. On the other hand if a Schottky-diode is employed, this capacitance discharge is not affected by the current steepness so that the oscillations do not increase with higher di/dt values [32]. Such behavior was also observed on the measurements performed at different speeds.

Regarding the turn-off transient, the steepness of the current through the switch leads to a voltage drop across the parasitic inductances, resulting in a certain voltage across the device capacitances. The higher the value of di/dt, the higher is the voltage drop and thus also the stored energy on the resonant tank. Such tank, which is the same from the activation transient, is excited by the sudden change of di/dt when the device blocks. Consequently it can be concluded that for all configurations, higher values of di/dt lead to higher oscillation amplitudes at turn-off, as was also observed during the experimental investigation.

In order to enable operation with high switching speeds without critically affecting the EMC of the system, it is therefore of major importance to reduce board loop inductances with advanced layout techniques, as discussed in [44]. In addition to this, coupling capacitances not only to ground but also among components need to be observed [43].

4.1.2. Dynamic resistance

In the path towards higher switching frequencies, it is not only necessary to consider the switching losses but also possible dynamic effects of the device conduction behavior. An example is the so-called modulation effect arising in bipolar devices due to the necessary time for the plasma injection in order to

achieve "nominal" conduction characteristic. Such data normally found in datasheets is measured with an increasing current through a continuously activated device using a curve tracer. Under practical operating conditions, the device is nevertheless stressed with high peaks of current following hard commutation, so that shortly after activation it is possible to experience a higher voltage drop than would be normally expected. Such temporary increase on the conduction losses becomes noticeable however only at higher switching frequencies, as the duration of the transient with increased resistance becomes more significant under decreasing duration of switching periods, as will be later investigated.

Measuring such effect is a challenge given the fact that it is necessary to simultaneously have a high dynamic and also amplitude resolution. Using a high voltage probe and just increasing the channel resolution is in this case not a suitable solution as the amplifier will be over-saturated leading to false results (even with negative levels). In order to deal with such problematic a clamping solution was employed to limit the maximum voltage across the probe to approximately 30V.

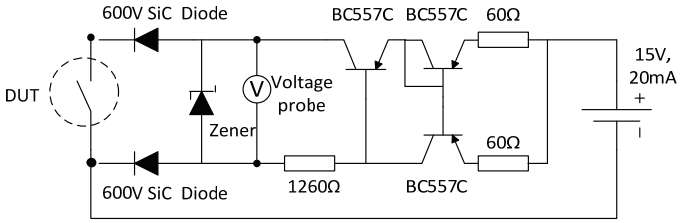


Fig. 68: Clamping circuit employed on the measurements [283].

Such clamping circuit has a very fast dynamic behavior and enables the use of low voltage probes that inherently have lower capacitance (higher bandwidth) and also higher resolution. A comparison between the clamped and unclamped measurement is depicted below.

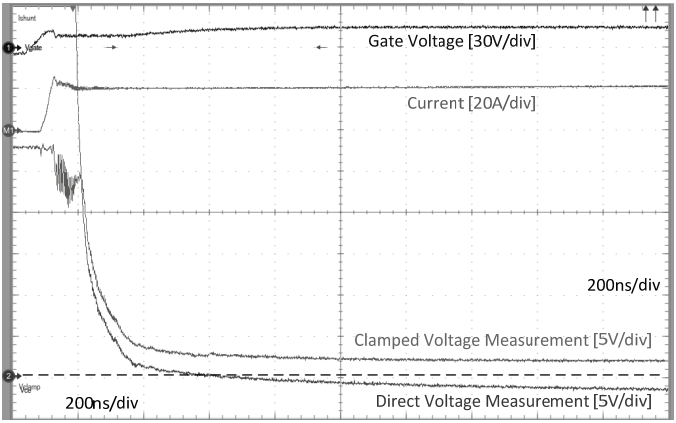


Fig. 69: Comparison between clamped and unclamped voltage measurement.

As was referred above, the modulation effect is mainly observed in bipolar devices that strongly resort on plasma injection for reduction of the drift region resistance. In order to better investigate the influence of such phenomena, some IGBTs were tested under ambient temperature at 550V/20A using an inductive load, enabling fast current transients. From the presented waveforms below it was possible to identify that the duration of the transient towards a lower voltage drop is significantly affected by the chip technology, being smaller for Trench structure and increasing for NPT. As an example, the waveforms for the FGL40N120AND rated at 1200V/40A with NPT technology are depicted below.

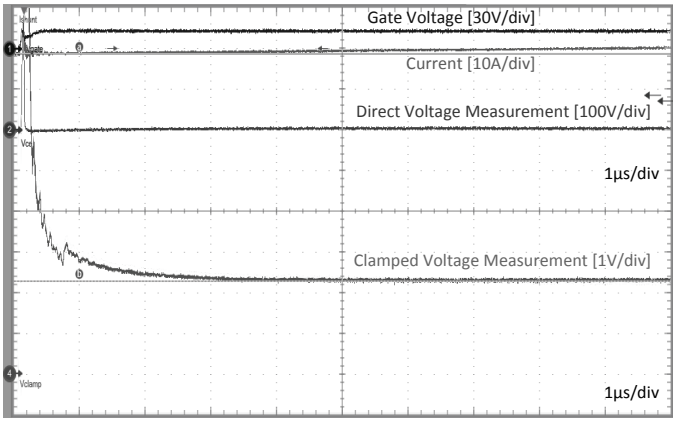


Fig. 70: Clamped voltage measurement of the FLG40N120AND.

The same measurements were afterwards performed for all investigated SiC devices (along with the 900V CoolMOS). Due to sharp transient into the conduction state, strong oscillations on the clamped voltage signal were triggered, especially in the case of the CoolMOS. It was also possible to observe a voltage discontinuity shortly after the commutation. After detailed simulations, it could be observed that the reason behind the observed behavior is an inductive voltage drop caused by the current peak flowing due to the sudden commutation of one of the high voltage diodes in the clamping circuit.

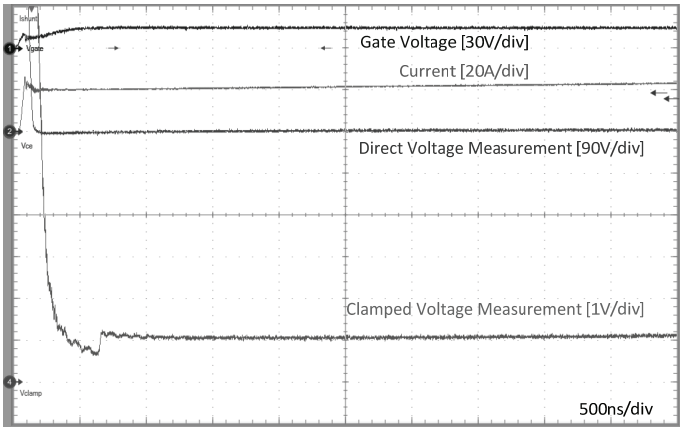


Fig. 71: Clamped voltage measurement of the CREE MOSFET.

As expected, none of the SiC devices presented any kind of modulation effect, as was expected for unipolar devices. Even though the normally-off JFET from Semisouth operates with a certain level of gate current (likewise happens with JFETs in bipolar mode), the behavior was also purely unipolar. This was also the case for the Transic BJT that also operates with practically no conductivity modulation.

In order to better assert the influence of the modulation effect on the conduction losses, the dynamic voltage drop of the FLG40N120AND was mathematically modeled by means of the following exponential function. In order to obtain a good fitting, the voltage variation (V_{drop}) during the transient time (T_{drop}) towards stable voltage drop (V_{nom}) was considered.

$$V_{DS}(t_x) = (V_{drop} \cdot e^{-\frac{tx}{T_{drop}}} + 1) \cdot V_{nom} \tag{25}$$

The conduction losses considering the modulation effect were calculated assuming a certain value of switching frequency (f_{sw}), duty cycle (D_x) and were afterwards

normalized to the losses obtained with fixed voltage drop value, as given in the equation below.

$$\overline{P_{cond}} = \frac{\int_0^{\frac{D_x}{f_{sw}}} V_{ds}(t_x) \cdot dt_x}{\int_0^{\frac{D_x}{f_{sw}}} V_{nom} \cdot dt_x} \tag{26}$$

The graph below presents an overview of the obtained results with the FLG40N120AND taken as reference. As was expected, the effect becomes more critical at higher frequency and smaller values of duty cycle, as the device is more constantly operating under the transient with increased losses. At switching frequency levels above 200 kHz, the modulation effect can increase the conduction losses in more than 10% when compared with the application of unipolar WBG devices.

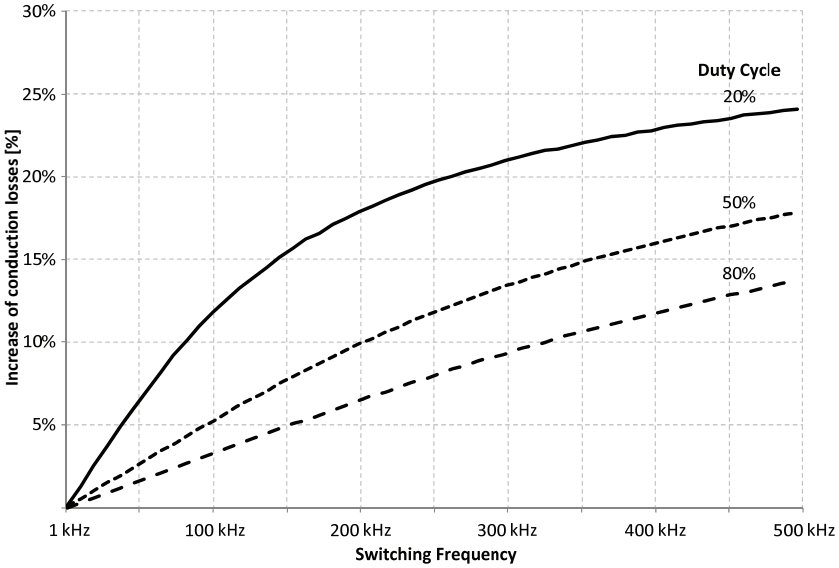


Fig. 72: Theoretical increase on the conduction losses depending on switching frequency and duty cycle value.

4.2. Effects on magnetic components

The main objective behind increasing the switching frequency is the possible reduction of magnetic elements, namely filter inductors and transformers, as these are responsible for a significant fraction of the overall hardware costs (roughly 15%). In order to attain not only a cost- but also a loss-optimized solution it is necessary to consider the different applications and inherent requirements. Such information needs to be afterwards linked to exiting materials properties, as will be presented in the following items.

4.2.1. Overview of magnetic materials and properties

Within the broad spectrum of available choices regarding magnetic materials, some key characteristics can be considered to identify the best candidate for a given application. The saturation flux density (given in T) is directly related to the required core cross-section area and thus to the overall volume. On the other hand, specific loss parameters define the attainable frequency and flux considering a maximum loss density. Meanwhile when considering transformers, high levels of permeability are also of interest, since it enables smaller core size.

A brief overview of materials available in the market is presented below, with their saturation flux plotted against specific losses for a flux swing of 100mT, switching frequency of 20 kHz and a temperature of 100°C.

Three main groups of materials can be identified, as marked on the graph. The first one includes ferrite that can be found having average to low level of specific losses, while the saturation flux is normally limited to a maximum of 0,3T. On the top right it is possible to identify the second group of materials including amorphous and SiFe alloys, now with much higher saturation flux but at the same time with high level of losses. The third and final group includes nanocrystallines alloys that have simultaneously high saturation flux and reduced amount of losses.

The first group (ferrites) is preferably employed in the design of magnetic elements operating with significantly higher flux swing. Examples are inductor for DC-DC converters, which are normally designed for higher ripple values given the possible use of larger capacitances. Another common application is in high frequency transformers with full magnetization swing.

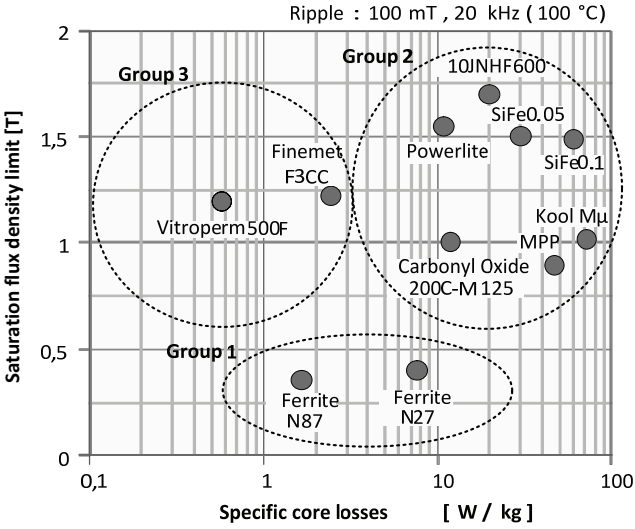


Fig. 73: Overview of core materials and inherent properties for given conditions with focus on differential mode inductors.

In contrast, the second group of materials referred above is widely used in output grid filter inductors, mainly because of the relatively low current ripple that allows moderate levels of core losses. The exact material choice depends directly on the switching frequency and power level: silicon-iron alloys for high power converters operating around 3 kHz and amorphous/silicon-steel alloys for up to approximately 20kW at around 16 kHz.

4.2.2. Prospects regarding higher switching frequencies

Based on the above discussed aspects, it becomes clear that increasing the switching frequency of inverters currently operating at 16 kHz (implying power rating below 50kW) will require materials with simultaneously low specific core losses and high saturation flux. The use of ferrites would not be in this case a good option, given the larger core size due to the inferior flux saturation limits. The best alternative is therefore the referred third group of materials that enable the desired size reduction. Concerning costs, the higher specific prices of such materials may in end be compensated by the smaller required cores along with other advantages like smaller expenditure with casing and transport, as will be later discussed.

In order to assert suitable choices regarding switching frequency and core material, an analysis will be here performed considering some practical application

conditions. The starting point is the consideration that the maximum utilization of the magnetic material (leading to minimum core size) is normally reached when the design fully exploits the maximum saturation flux capability. The flux swing (ΔB), from which the core losses are exponentially related, can thus be directly calculated from the application ripple ($\Delta I_{\%}$) and maximum flux values (B_{max}), as given in the equation below. As a consequence, in case the specific core losses reach a certain critical limit, the maximum flux needs to be decreased what leads to an increase on the core size.

$$\Delta B = B_{max} \cdot \Delta I_{\%} \tag{27}$$

The graph in Fig. 74 presents an overview of the maximum selectable flux density with a peak ripple value of 10%. The calculation was done considering the actual ripple variation of a 3-Level converter under worst case conditions for a whole sinus wave. The ripple variation of a 2-level converter with filter designed for a similar ripple limit reaches slightly lower values. A general limit for the specific core losses was also assumed at 100mW/cm³. Because individual limits are strongly influenced by core geometry/size along with material thermal conductivity and Curie temperature, a more detailed investigation would be necessary in order to assert more precise individual limits.

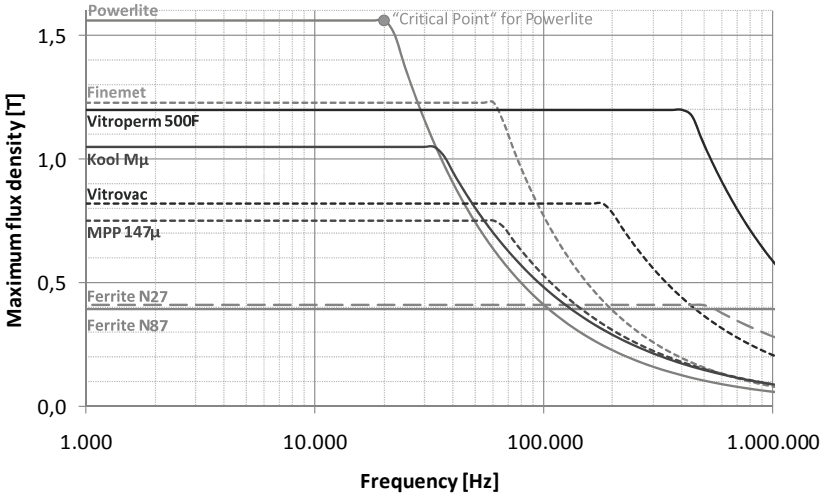


Fig. 74: Benchmarking of core materials for AC inductors in low power systems.

As can be observed in the obtained graphic above, at lower frequencies the design is rather limited to the saturation flux limit. After increasing the frequency further, a critical level is reached, where the specific losses surpasses the maximum limit.

Going beyond such limit requires a reduction of the flux swing and consequently of the selected maximum flux density. Consequently from this point on, no significant reduction of the magnetic element size may be obtained; as for each increase in the frequency the maximum flux needs to be correspondently reduced.

In comparison with ferrites, Powerlite (amorphous material, Group 2) and Finemet (nanocrystalline material, Group 3) from Toshiba are respectively interesting up frequencies respectively around 20 and 60 kHz. Meanwhile, the materials Kool Mμ and MPP 147μ (iron powder, Group 2) from Magnetics have their critical points at 35 and 60 kHz. One the other hand, these limits are significantly extended for the materials from Vacuumschmelze Vitrovac (amorphous material, Group 2) and Vitroperm 500F (nanocrystalline material, Group 3) to 200 and 440 kHz. Despite its outstanding performance, one drawback of Vitroperm 500F is the still very high levels of permeability in the currently available cores (so far ungapped), what may prove to be critical in future designs of AC or DC inductors with air-gap.

Increasing the switching frequency of high power inverters currently operating below 3 kHz will in contrast demand materials will lower specific losses within the group 2. The same graph presented in Fig. 74 is now plotted only for materials of the group 2.

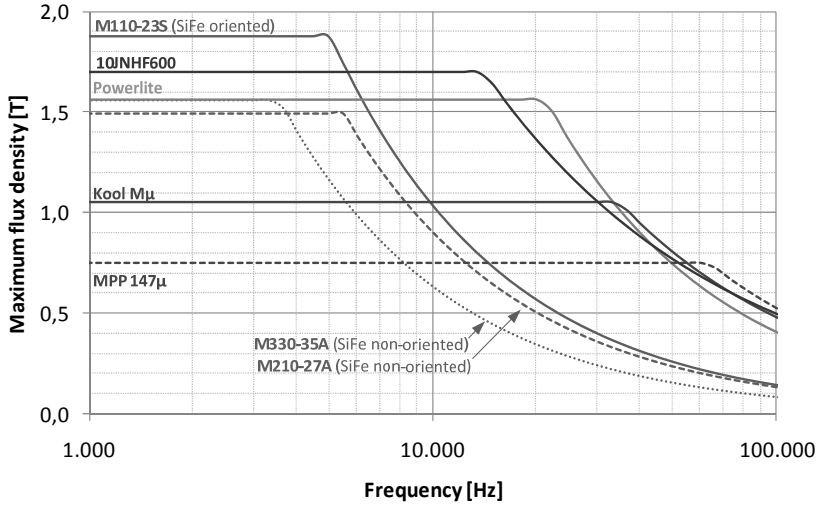


Fig. 75: Benchmarking of core materials for AC inductors in high power systems.

Conventional silicon steel normally used in the referred applications cannot cope with higher frequency levels, being strongly limited in the maximum flux density. The investigated non-oriented and oriented variants reach their limit up to

respectively 3,6 and 5,4 kHz. One first option is the high-grade variant 10JNHF600 that has a higher silicon concentration and at 5 kHz and 0,2 T have almost 50% less specific losses [4], with a critical frequency of over 14 kHz. Moving in the direction of frequencies above 20 kHz, the Powerlite material becomes a better option. On the other hand, both iron powder materials (Kook Mμ and MPP 147μ) have lower saturation flux limits and are attractive up to 66 and 36 kHz.

Another issue to be considered at high power applications is that the converter is in most cases connected to a step-up transformer for connection to the medium-voltage grid. Given the fact that part of the current filtering is performed by the transformer inductance, it is necessary to consider a possible impact on the transformer core losses in case of higher switching frequencies.

The results from the graphics above can also be used to display a direct estimation of the filter size. This is obtained by calculating the inverse of the multiplication between the frequency and flux density values as given below.

$$\text{Inductor Size Factor} \propto \frac{1}{\text{inductance value}} \propto \frac{1}{\text{frequency} \times \text{maximum flux}} \tag{28}$$

The results are presented as follows. Here becomes clear the above referred limitation of the maximum loss density, as going beyond each material "critical point" on the direction of higher frequencies only offers a marginal size reduction.

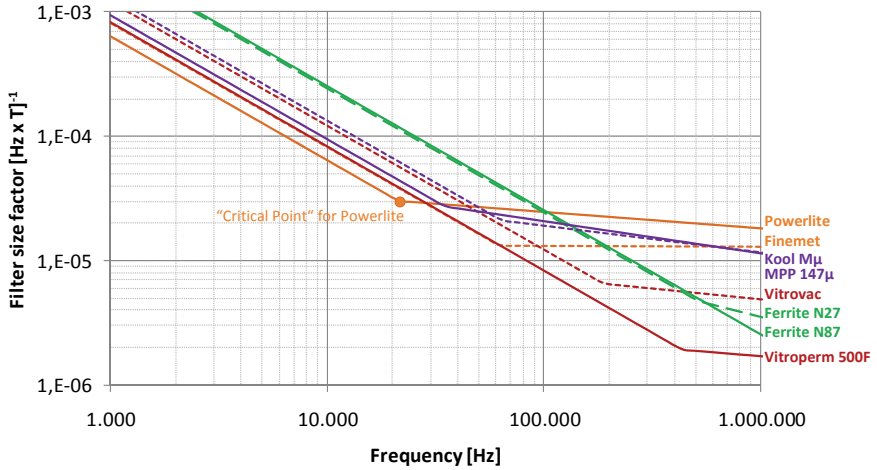


Fig. 76: Filter size factor of core materials for AC inductors in low power systems.

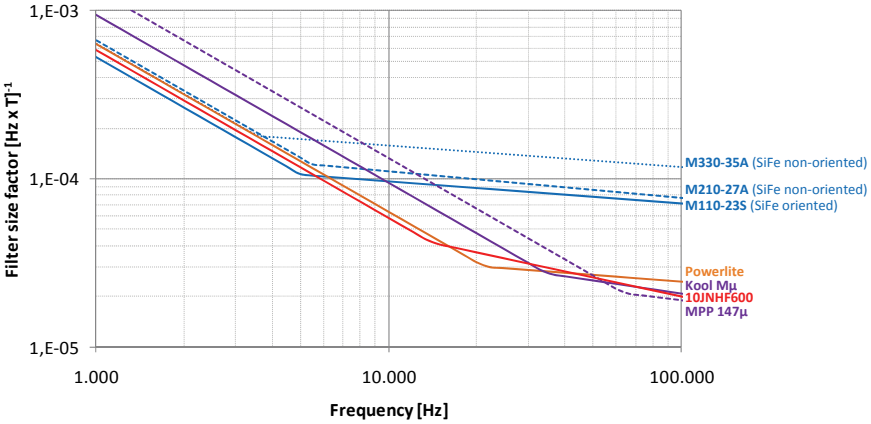


Fig. 77: Filter size factor of core materials for AC inductors in high power systems.

In the case of the application with high frequency transformers, another material property of interest is the relative permeability in order to operate with low levels of magnetizing current, enabling smaller core sizes. An overview of some materials is presented below.

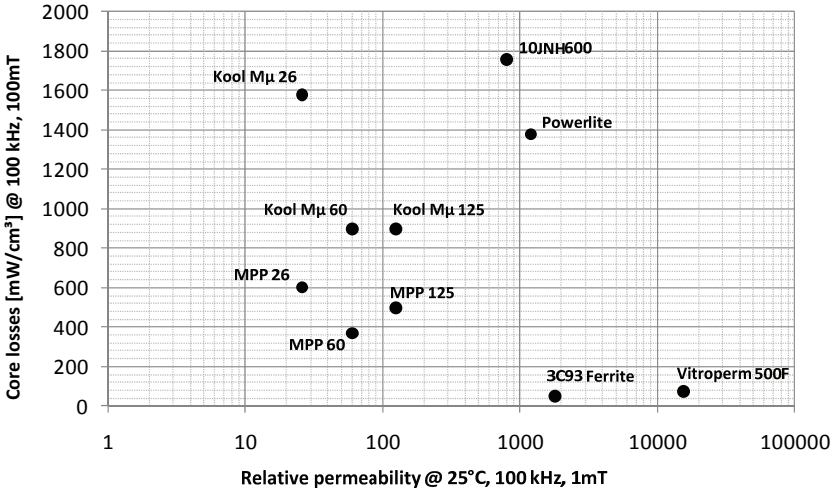


Fig. 78: Benchmarking of core materials for high frequency transformers [6].

It becomes clear that for the given operating conditions, critical level of core losses are obtained with practically all materials, requiring a reduction of the flux swing what in other words means increasing the core size. In contrast, ferrites are as expected the ideal material for high frequency transformers, simultaneously having low core losses and high levels of permeability. And outstanding performance can be observed for the material Vitroperm 500F, with slightly higher losses, but almost ten times higher permeability, being therefore the preferred material for high frequency compact transformers.

4.2.3. Prospects regarding higher ripple amplitudes [48]

Besides increasing the switching frequency, another possibility of reducing the size of filter inductors is the operation at higher ripple values. Considering that requirements concerning the maximum ripple in either input or output remain the same, it therefore necessary to either employ a higher capacitance or operate with more interleaved stages to compensate the smaller inductor size.

The prospect of increasing the ripple value turns out to be especially attractive in conjunction with the use of WBG devices. Reason for this is the fact that in some of the investigated devices, the turn-off losses were significantly smaller than the turn-on. By increasing the turn-off current value while reducing the one at turn-on, the overall switching losses tend to decrease. Such potential is analyzed below, which presents the normalized total switching losses for ripples up to 100% (peak-to-peak). Two values of average current, namely 15 and 35A are considered in the calculations, in order to illustrate the fact that the behavior of some devices is strongly influenced by the operating conditions. In the best case (with JFETs) one can spare up to 20% of the switching losses. In contrast, the SiC MOSFET represents an exception, as at lower current values the total losses tend to increase. Such behavior is on the other hand valid for Si-IGBTs at all current values, given the fact that the turn-off losses are always higher and as a consequence any increase of the ripple leads to higher switching losses. This is in fact one of the reasons why higher ripple operation has so far always resulted in lower efficiency levels.

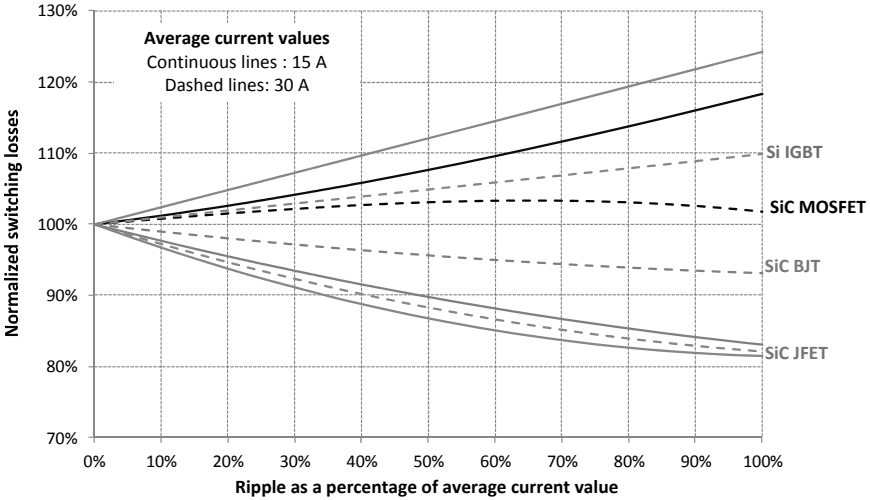


Fig. 79: Variation of total switching losses as a function of ripple value for different semiconductor technologies (at 550V, 150°C).

Important to observe here is that despite a similar reduction is obtained in the required filter inductance value when either increasing the switching frequency or ripple; the resultant change on the inductor volume differs. Reason for this is that higher ripple values directly lead to higher RMS current value (requiring higher winding cross-section) and higher current peak (with higher peak flux and consequently larger core).

In order to evaluate such effects, the required inductance for a step-up and step-down converter is calculated below, with V_o and V_i being respectively the output and input voltage, ΔI_{max} the maximum ripple limit, f_{sw} the switching frequency and M the voltage gain. These final equation equations consider the condition under which the maximum ripple is attained, namely with duty cycle (D) equal to 0,5.

$$\Delta I_{BOOST} = \frac{V_O \cdot (M-1)}{M^2 \cdot L \cdot f_{SW}} \Rightarrow \text{Max for M=2} \Rightarrow L_{BOOST} = \frac{V_O}{4 \cdot \Delta I_{max} \cdot f_{SW}}$$
$$\Delta I_{BUCK} = \frac{V_O \cdot (1-D)_s}{L \cdot f_{SW}} \Rightarrow \text{Max for M=1/2} \Rightarrow L_{BUCK} = \frac{V_I}{4 \cdot \Delta I_{max} \cdot f_{SW}} \quad (29)$$

The influence of the current ripple on the expected inductor volume is calculated following the procedure presented in [48]-[49] by considering the multiplication of three parameters: inductance, RMS current and peak current as presented below, with I_{avg} equal to the average value of the current across the inductor.

$$V_L \propto \frac{1}{\underbrace{\Delta I}_{L}} \cdot \underbrace{\sqrt{\left({I_{avg}}^2 + \left(\sqrt{\frac{1}{3}} \frac{\Delta I}{2} \right)^2 \right)}}_{I_{RMS}} \cdot \underbrace{\left(I_{avg} + \frac{\Delta I}{2} \right)}_{I_{peak}} \tag{30}$$

This equation is rewritten using the ripple factor r, as defined below.

$$r = \frac{\Delta I}{I_{avg}} \tag{31}$$

$$V_L \propto \frac{1}{r} \cdot \sqrt{\left(1 + \left(\sqrt{\frac{1}{3}} \frac{r}{2} \right)^2 \right)} \cdot \left(1 + \frac{r}{2} \right) \tag{32}$$

The equation is simplified assuming that the ripple factor r is much smaller than 10.

$$V_L \propto = \frac{1}{r} + 0{,}5 \tag{33}$$

In the figure below is plotted the inductor volume as a function of the relative ripple value, normalized to the value obtained with a ripple of 20%. One can clearly observe that it is possible to obtain significant size reduction up to about 80% ripple, afterwards, any additional increase brings only marginal gains.

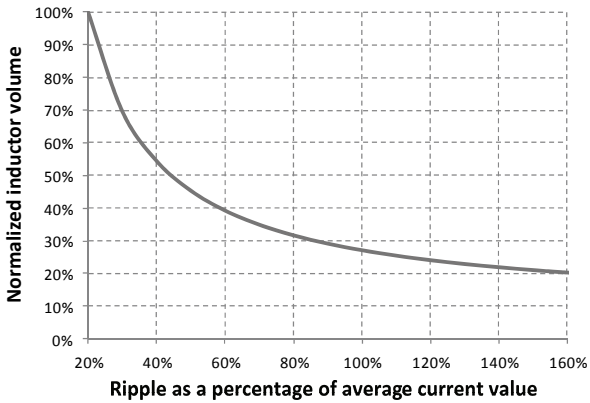


Fig. 80: Normalized inductor volume as a function of current ripple.

With the objective of more precisely asserting the influence of operation at higher ripple values, it is necessary to individually consider the inductor loss components. In the case of the core, losses are normally modeled after the Steinmetz equation, with exponents related to the frequency and flux swing values. From a brief

overview of these exponents presented below, one can observe an increase on the ripple and consequently of the flux swing will have a higher impact than higher frequencies on the core losses of ferrites. For other materials, especially the nanocrystalline ones, there is only little difference.

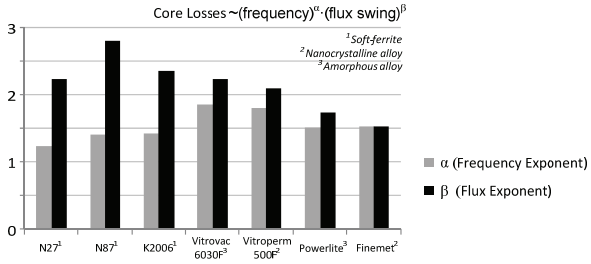


Fig. 81: Overview of Steinmetz core loss factors for different materials.

With the graph above it is possible to assert only the relative impact on the core losses. In the end, the absolute value strongly depends on the operating conditions. The methodology already presented in Fig. 74 is employed again with the aim to investigate the trade-off between higher frequencies and ripple values. The maximum flux density for 20 and 40 kHz is therefore plotted as a function of the ripple value for different materials. The influence of the ripple value on the peak magnetic flux is in this analysis assumed to be compensated by a higher number of turns.

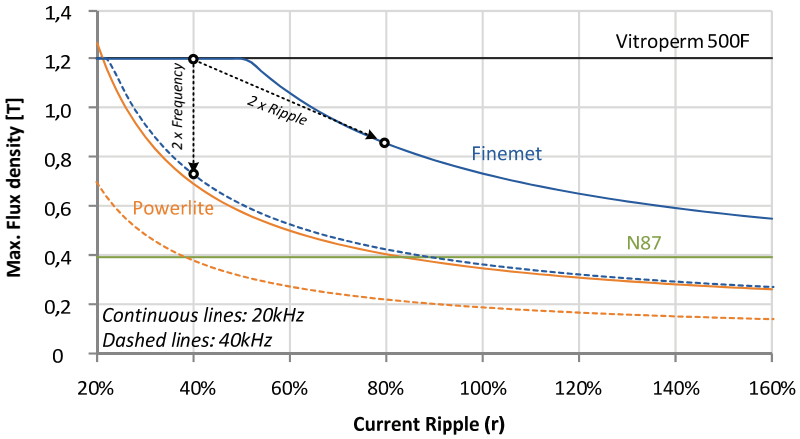


Fig. 82: Maximum flux density for operation at 20 and 40 kHz considering different ripple values.

From the picture above it is possible to draw some conclusions. Firstly, materials with very low amount of core losses, namely Vitroperm 500F and N87 Ferrite show no loss limitation at the investigated conditions. Meanwhile, for both Finemet and Powerlite it becomes clear that for the given conditions, doubling the ripple had a smaller impact on the losses and therefore on the required peak flux reduction when compared with doubling the switching frequency.

Another aspect to be considered here are the winding losses, namely the AC component caused by the skin and proximity effects. In order to deal with such effects in the case of operation at high frequency values, the wire diameter is normally reduced with the squared root value of the frequency along with especial winding techniques. Related drawbacks are higher costs and less effective winding cooper area. In the case of higher current ripple, the high frequency AC component increases in amplitude, directly affecting the AC winding losses. Such prospect can become especially critical if the winding AC resistance is several times larger than DC one, what is normally the case of inductors constructed with multiple layers. An estimation of such problematic is depicted below (continuous lines), considering different ratios between the AC and DC winding resistances.

As previously stated, higher ripple also leads to an increase on the maximum peak current and consequently higher flux density. In order to cope with such fact, one can either increase the core size or the number of turns. The last alternative is more commonly applied but is also directly responsible for a reduction on the effective cooper cross-section, resulting in higher winding losses. Such aspect is represented with dashed lines in Fig. 83.

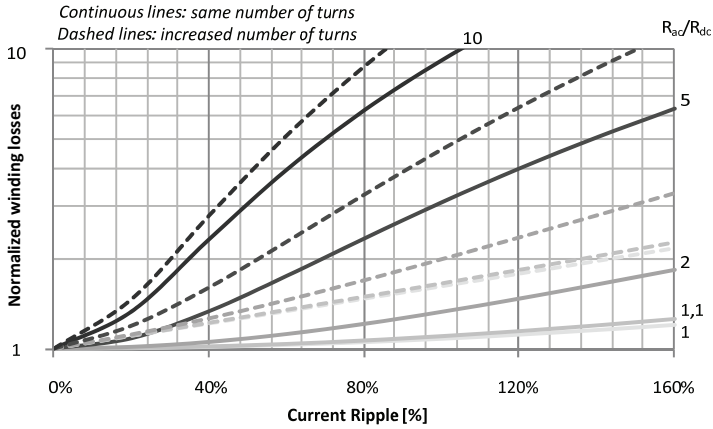


Fig. 83: Normalized winding losses as a function of current ripple for different rations between winding AC and DC resistances.

From the analysis presented above one can observe some points regarding the operation at higher current ripple.

- Inductor size reduction is limited by some side effects, with ripple values beyond approximately 80% having only reduced effect.
- For most of the investigated WBG devices, higher ripple may result in up to 20% reduction on the switching losses.
- Higher core losses are expected with ferrites, while other materials may in fact enable a more significant size reduction instead of higher frequencies.
- Winding losses may become the bottleneck, especially in the case of high AC winding resistance. It is thus necessary to employ especial wires and winding techniques to cope with such problems.

5 Application of WBG devices: cooling effort and other thermal aspects

The expenditure with cooling ranges from the required heatsink size to the auxiliary cooling circuits like fans and water pumps. The use of WBG devices can affect the referred aspects by enabling operation at lower level of losses and/or at higher junction temperature (either continuously or during transients). At the same time, the reduced chip size offers a significant challenge regarding loss concentration and heat spreading. Each of these aspects will be briefly discussed in the following items, followed by an assertion of possible gains regarding the cooling effort on renewable energy power conversion systems.

5.1. Thermal related issues

The maximum junction temperature for normal Si power devices is widely considered to be around 200°C; with some commercial products being currently rated at 175°C. Going beyond such level leads to critical reverse leakage current (among other issues, as presented in [14]) that compromise the correct device operation. An alternative is the use of SOI technology that enables operation up to 300°C but with limits regarding applicable power and voltage levels. Reasons for this are the lateral structure and the difficult manufacturing process of high quality isolated silicon on top of an isolator.

WBG-based devices can on the other hand withstand much higher temperature levels due to the much lower intrinsic carrier concentration level, with 400°C being widely demonstrated in several publications and up to 600°C theoretically expected [12], [14], [17]. When considering the current field of application it is nevertheless possible to identify several limiting issues in the path of such high temperatures not only at device but also on circuit periphery level.

5.1.1. Maximum temperature and thermal runaway

The possibility of operating at much higher junction temperatures (what directly implies higher loss density) is especially attractive in WBG devices as it enables not only the prospect of reducing the cooling expenditure but also allows higher current loading and therefore better chip utilization.

Regarding such possibility, it is important to consider the influence of the temperature on the device performance and the possibility of running into thermal

runaway. In the case of all investigated 1200V-rated JFETs, an increase of the junction temperature of 125K led to an increase of more than 100% on the equivalent resistance. For the BJT it was possible to identify a factor of 75% and for the MOSFETs approximately 25%. Meanwhile the switching losses are practically independent of the temperature for all devices, as between 25 and 150°C was observed a reduction of approximately 5%. An explanation for this lies on the fact that these devices do not rely on conductivity modulation so that the highly temperature dependent recombination times are absent. Such effect on the other hand is observed on the IGBT, with switching losses increasing by more than 110% for a temperature increase of 125K. An important remark here is that in case the intrinsic diode of the SiC devices is employed for freewheeling, stronger temperature dependence for the losses is observed (from 18 to more than 35%) given the dependence on the small amount of stored charges in the respective PN-junctions.

With such information regarding the losses in mind, it is possible to evaluate the relation between the maximum current loading and maximum junction temperature in order to avoid thermal runaway [13]. Such analysis was performed here by calculating the device junction temperature given a certain current stress and switching frequency. For the conduction losses, the temperature dependency of the device equivalent resistance was extended to higher levels taking into account the here performed measurements and information found in the literature. Meanwhile, the switching losses were considered at 550V and at 25°C as a worst-case approximation, as with rising temperature they tend to present a slight decrease. The junction temperature was then calculated for an ambient temperature of 40°C, considering each individual device value of junction-to-case thermal resistance (Rth_{JC}) summed with a thermal resistance of case-to-ambient of 1,3K/W.

The value of the current at thermal runaway was identified at the point where the derivation of the curve from the current as a function of the junction temperature reaches zero. In order to ensure safe operation, the maximum current stress was calculated as 90% from the referred value. Going in the direction of a higher switching losses (i.e. higher switching frequency), the maximum current loading is reduced, while the maximum junction temperature increases, given the lower temperature dependency of the switching losses. On the other hand, changes in the junction-to-ambient thermal resistance have a significant effect only at higher levels of switching losses.

The results obtained with the CREE 1200V SiC MOSFET are presented below for three different values of switching frequencies. The transition into thermal runaway is rather smooth here, given the lower temperature dependency. It becomes clear that junction temperatures above 250°C are under the considered

conditions not of interest, as for operation at 100 kHz the device can be stressed with approximately 25A at 230°C.

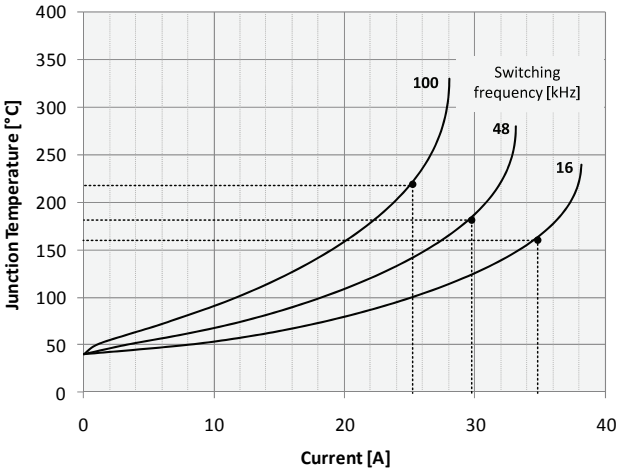


Fig. 84: Thermal runaway characteristic of CREE 1200V SiC-MOSFET assuming Rth_{js} of 1,55K/W.

The same analysis is presented below for the normally-on 1200V JFET from Infineon. The much harsher transition in thermal runaway can be in this case justified by higher temperature dependency. From the de-rating it is possible to identify that the maximum device utilization is reached at 265 and 185°C for operation at respectively 100 and 16 kHz.

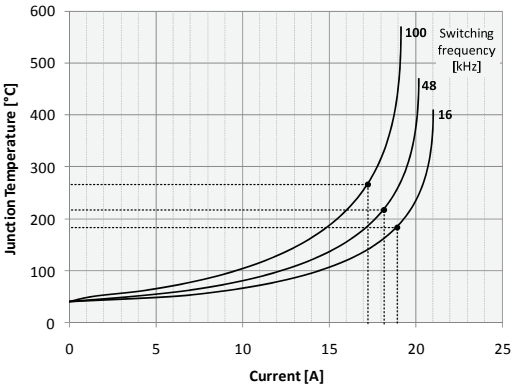


Fig. 85: Thermal runaway characteristic of Infineon 1200V SiC-JFET assuming Rth_{js} of 1,85K/W.

In case of the SiC BJT, the investigation was performed considering two levels of switching energy, considering measurements with different driving configurations. Here it becomes clear the effect of operation with higher switching energy, namely the strong reduction of the device current capability, especially under higher switching frequencies. For the measurements without optimization of switching energy, the maximum temperature was shifted to higher levels, as can be observed below. The maximum device utilization in this case is reached at 365 and 175°C for operation at respectively 100 and 16 kHz.

In contrast to this, when the switching energy is reduced, it is possible to observe a significant increase on the current loading capability, with simultaneous reduction of maximum levels of operating temperature. Maximum device utilization is now reached at about 260°C and 160°C under respectively 100 and 16 kHz.

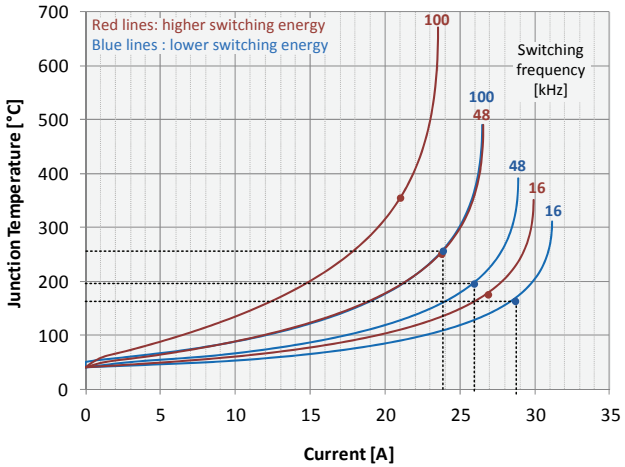


Fig. 86: Thermal runaway characteristic of Transic 1200V BJT assuming Rth_{js} of 1,8K/W.

As a reference, the same analysis was also performed for the IGBT IKW40N120H3, with results presented below. Here the switching losses are the component most strongly affected by the temperature, with more harsh transition into thermal runaway at higher switching frequencies. The value of the switching energy itself, being several times higher than the ones from the SiC devices, leads to a significant limitation observed for operation at higher switching frequencies. At 16 kHz was determined a maximum current stress of 25A at a junction temperature of 165°C, slightly below the maximum specified limit.

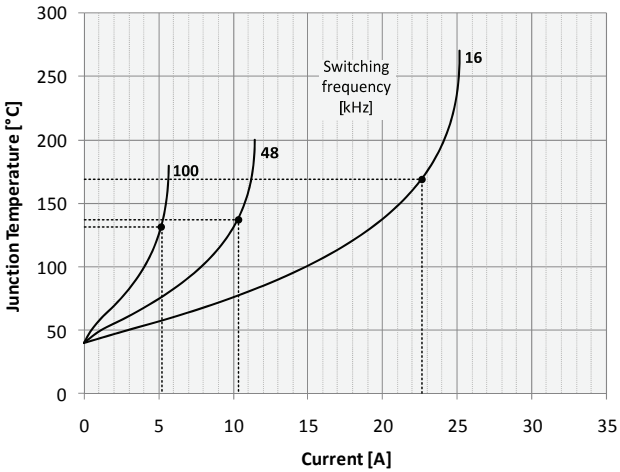


Fig. 87: Thermal runaway characteristic of Infineon IKW40N120H3 assuming Rth_{js} of 1,6K/W.

From the presented results it is possible to assert that in order to achieve maximum device utilization without thermal runaway, maximum temperature levels around 250°C for devices with low switching losses (JFETs and MOSFETs) can be expected. Higher temperatures are theoretically possible by de-rating the current levels and enabling operating with lower current-density. This nevertheless reduces the chip utilization and is of interest only when the application definitively requires such high levels of temperature, either due to limitation of the cooling capability or because of very high ambient temperatures. These both conditions are nevertheless valid for aerospace and automobile applications and not found in renewable energy power converters.

5.1.2. Other limitations

Not only the losses but also other device properties are affected by higher junction temperatures. This is the case for the threshold voltage that shifts towards zero in the case of normally-off devices, while the behavior and stability at levels beyond 200°C still remains not completely investigated. Other individual device issues are presented in the table below.

The most critical aspects are nevertheless not inherent to the SiC devices alone but rather to the construction of suitable and reliable power modules capable of withstanding the referred conditions. Several critical factors towards operation with junction temperatures around 250°C are summarized in Fig. 88. Summing up, the

proposed conditions not only require materials with higher temperature capability (soldering, contacts) but also better CTE matching (coefficient of thermal expansion) to reduce mechanical stress under temperature cycling with increased amplitude.

Table 8 –Device specific thermal issues.

Device	**Issues**	**Temperature dependency of resistance**
SiC MOSFET	Gate insulator long time stability, with effects like threshold voltage shift and even failure being strongly temperature dependant.	Low
SiC BJT	Higher driving losses with increasing temperature due to gain reduction (35% for 125K change)	Moderate
N-on SiC JFET	Low-voltage Si-MOSFET in cascode association needs to be thermally isolated from JFET given inherent limitations	High
N-off SiC JFET	Possible increase of junction leakage	Very high

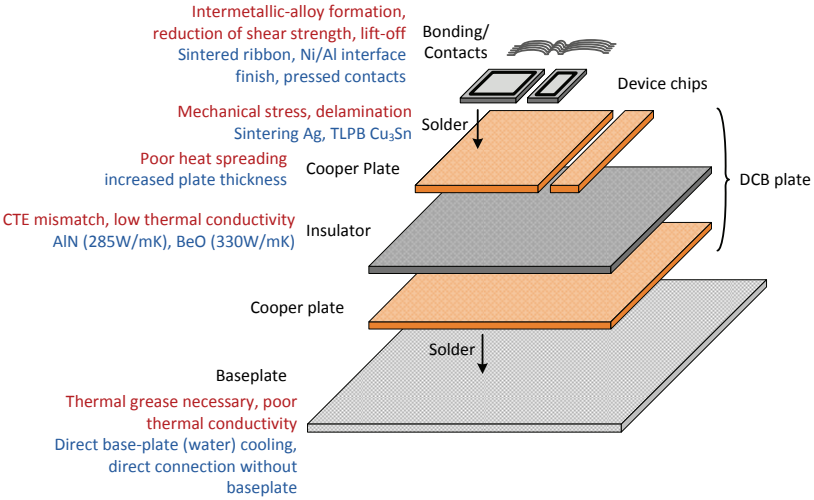


Fig. 88: Issues related to module construction (in red) with possible solutions (in blue) [14][19]-[27].

On the other hand, the temperature limitation of other components at system level like capacitors and control/driver circuitry [15] becomes critical only when considering operation under very high ambient temperatures when the whole system is under thermal stress. This is not the case for the applications under investigation, as only the power devices and heatsink are affected. Proper distance and thermal isolation between board and heatsink are nevertheless necessary in order to avoid placing all board components and sensors under stress, as can be seen below for a board with 1cm distance from the heatsink [21]. The gate driver circuits are for instance the components with highest stress due to their proximity to the power module. It is consequently not advisable to employ optocouplers, given their significant temperature susceptibility and aging issues.

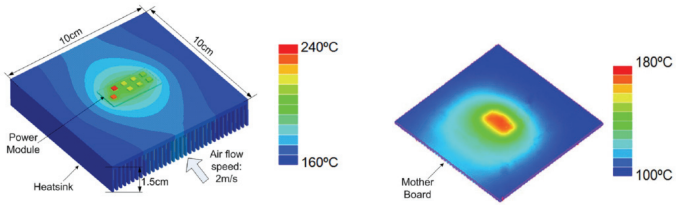


Fig. 89: Temperature profile of SiC Module with heatsink and PCB board directly placed over it [21].

In addition to this, the heatsink, which now may have temperature beyond 100°C, needs to be protected from external access and thermally isolated from the rest of the enclosure. While this is already valid for high power systems rated at several hundred kW, it may be necessary to perform significant design changes in lower power systems. Reason for this is the tendency to integrate the heatsink in the enclosure, as can be observed below for a three-phase photovoltaic inverter from the company SMA.

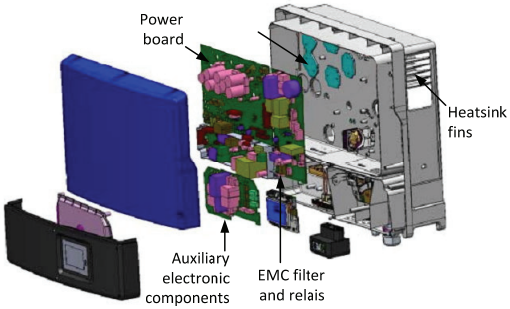


Fig. 90: Exploded view of three-phase inverter rated at 17kW [16].

5.1.3. Overload capability

The capability of operating at higher junction temperatures can also be used to extend the overload capability under circumstances where the loss profile has a time constant smaller than the one from the power module thermal impedance. This is most frequently found in generator systems when operating below 5 Hz [28], with concentration of the losses on a few devices. The effect of the waveform fundamental frequency on the junction temperature increase is depicted below.

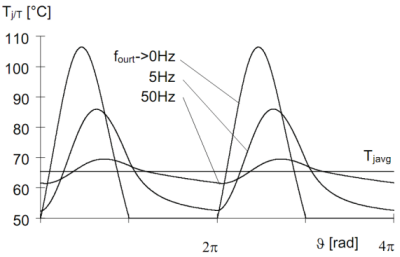


Fig. 91: Simulated junction temperature for different values of load fundamental frequency [29].

In the case of wind power systems, such conditions are most commonly found with double-fed asynchronous and gearless synchronous generators where the power converter needs to be over dimensioned in order to cope with the referred stress conditions.

Another consequence of the higher temperature limit before breakdown is the increased avalanche energy, of interest regarding either short-circuit conditions or during hard commutations (enabling an extension of SOA).

5.1.4. Loss density and dissipation

As was already discussed before, operation under a higher level of specific losses is of considerable interest when employing WBG devices in order to increase the current loading and thus enable further reduction of the chip area.

Such possibility can be attained by reducing the thermal resistance to cooling medium (air or water), enhancing heat spreading or by increasing the maximum junction temperature.

The high thermal conductivity of SiC is for instance normally described as a key property (not only against Si but also GaN) enabling higher loss density due to superior dissipation capability. When considering the whole chain of thermal

interfaces up to the ambient, the overall gain due to using SiC chips is nevertheless practically insignificant. Reason for this is the fact that the chip itself is responsible for less than 3% of the overall thermal resistance, as can be observed in the graph below.

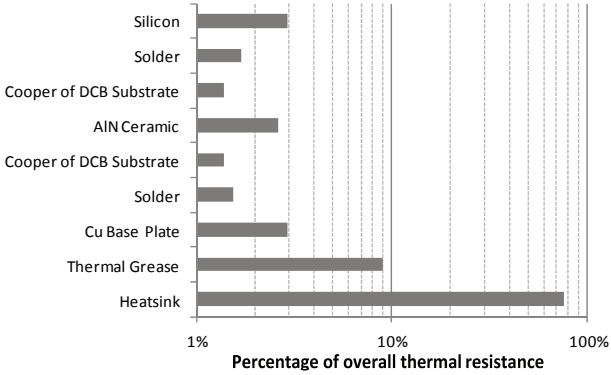


Fig. 92: Distribution of thermal resistances for a power module attached to air-cooled heatsink [45].

More effective is therefore the use of ceramic materials with high thermal conductivity like AlN and BeO or direct base-plate cooling, as already presented in Fig. 88 or even heat pipes. Larger distance between the chips and thicker cooper layer on the DCB may also enable higher heat dissipation but with the drawback of increasing the distance between chip connections and consequently leading to higher commutation path parasitic elements.

5.2. Cooling effort

5.2.1. Savings with operation at high junction temperature

Here will be quantified the possible savings regarding operation at higher junction temperature along with related limitations. Under such conditions, the required thermal resistance between junction and ambient is calculated as a function of the maximum junction temperature. At the same time the expected increase in the losses is considered, with an assumed fixed division factor (k) between conduction (P_{cond}) and switching losses (P_{sw}). The obtained values are then normalized to the ones for a reference value of junction temperature (T_{ref}) in order to obtain a

normalized value for the thermal resistance between junction and ambient ($R_{th\_ja\_norm}$). The equation below provides an overview of such calculation.

$$R_{th\_ja\_norm} = \frac{\left(\frac{T_j - T_a}{k \cdot P_{cond}(T_j) + (1-k) \cdot P_{sw}(T_j)} \right)}{\left(\frac{T_{ref} - T_a}{k \cdot P_{cond}(T_{ref}) + (1-k) \cdot P_{sw}(T_{ref})} \right)} \tag{34}$$

A reference junction and ambient temperature of respectively 150 and 40°C are assumed in the calculations. The results for two loss division factors (k) of 0,8 and 0,5 are presented below. It is clearly possible to observe the effect of the positive feedback of the temperature over the losses, as for higher values of temperature the increasing amount of losses tend to limit the savings, especially when the conduction losses are dominant (for k equal to 0,8).

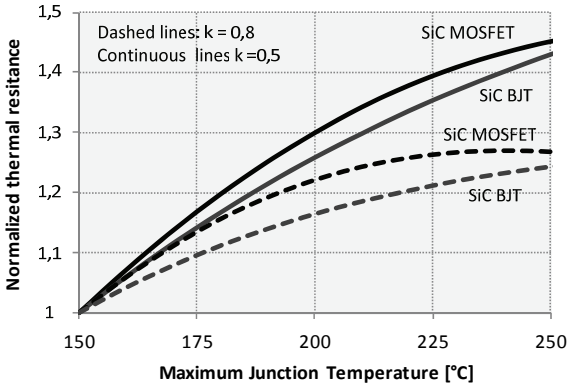


Fig. 93: Normalized thermal resistance as a function of junction temperature.

The MOSFET showed for instance a slightly better performance at lower temperature levels but the curve reached a saturation level much earlier than the BJT. One reason for this is the fact that a low temperature dependency is observed only up to approximately 200°C; above such level a steady increasing tendency dominates. Meanwhile, the BJT enables similar savings but only at much higher temperature.

5.2.2. Savings with reduction of losses

From the discussion presented in the previous topics, one can conclude that increasing the maximum junction temperature of the device may not be an

interesting alternative in order to reduce the cooling expenditure given the higher thermal stress across module components and also lower levels of efficiency.

An alternative goes in the opposite direction, namely towards the reduction of the losses what in turn directly allows higher values of thermal resistance to ambient. Interesting to observe here is that even an apparently insignificant increase of the already high levels of efficiency has a strong effect on the losses. This is demonstrated in the graph below, where the normalized thermal resistance of the cooling system (y-axis) is plotted against the increase of the efficiency at nominal load (x-axis), considering six different values of original efficiency.

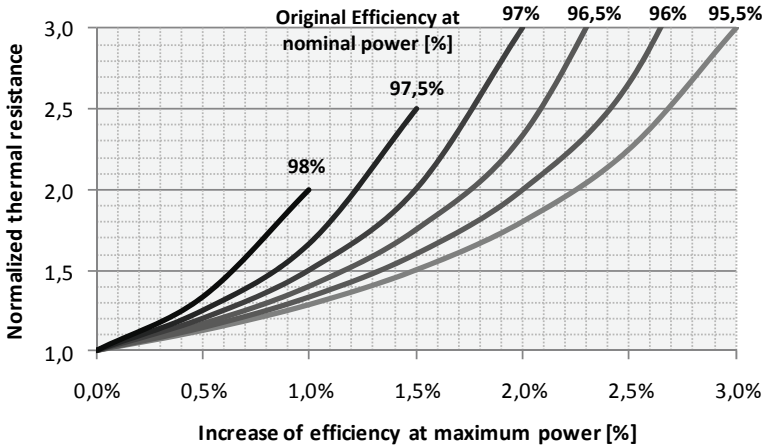


Fig. 94: Possible increase of the thermal resistance given a certain increase of the efficiency.

As expected, the higher the efficiency level is the higher will also be the impact of a given percental increase of the efficiency. Taking as example an inverter with 97,5% efficiency at nominal load, an increase of 1% allows a more than 50% larger thermal resistance of the heatsink in relation to the original one. In order to better assert the referred potentials, a market research of passive air-cooled heatsinks was performed, with relation between the thermal resistance to price and volume presented in Fig. 95.

From this research it is possible to observe that both price and volume depend exponentially on the thermal resistance with exponents respectively equal to respectively 1,15 and 1,54. Taking this in consideration, the expected economy in € is plotted as a function of the possible increase of the thermal resistance, Diverse

levels of losses are considered, along with junction and ambient temperatures respectively equal to 125 and 40°C.

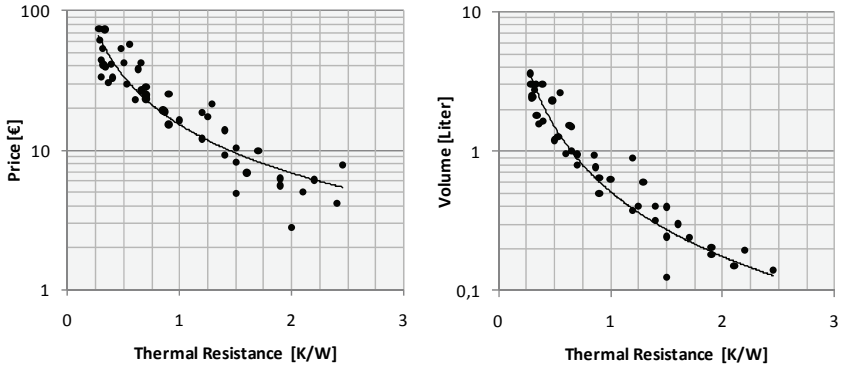


Fig. 95: Market research of heatsinks regarding price and volume.

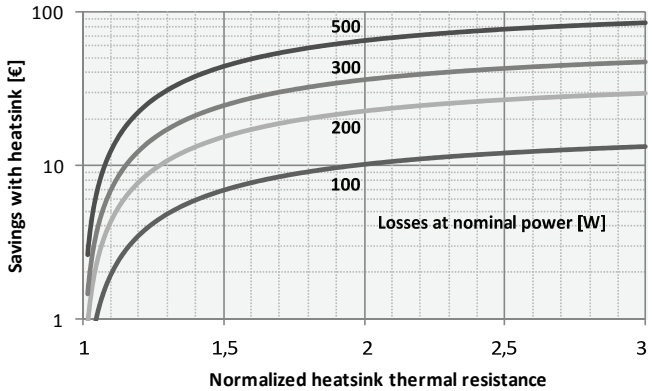


Fig. 96: Potential economy due to increase of thermal resistance for different levels of losses.

From the graph it is possible to conclude that the impact of possible increase of the thermal resistance in systems with low levels of losses (i.e. with lower power rating) is limited to a maximum of 10 €. On the other hand, when a level of 500W losses is considered, more than 60 € can be expected. Another conclusion is that increasing the thermal resistance beyond a factor of approximately 1,5 starts to have a reduced economical gain, simultaneously demanding extended expenditure in order to provide the necessary massive reduction of the losses.

When considering higher power levels employing forced-ventilation or water-cooling, one of the most significant aspect turns out to be the necessary auxiliary power to drive the fans and pumps. An overview of values for both referred cooling methods is presented below, taking as base the SKiiP IPM from the manufacturer Semikron.

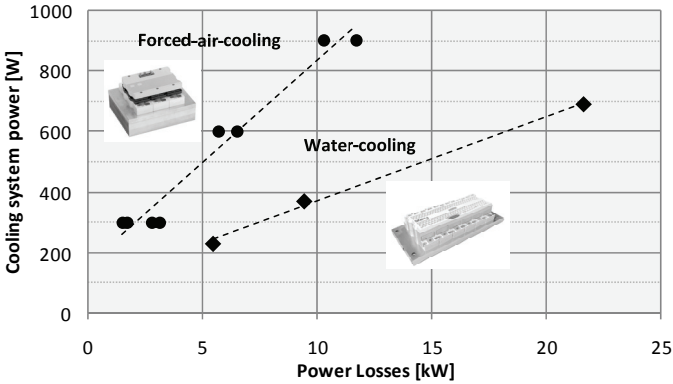


Fig. 97: Cooling system power level as a function of power losses.

In order to assert possible gains related to reducing losses in the referred high power systems, the graph below is plotted. It links the effect of increasing the efficiency from certain reference values (market with a dot) with the result reduction of the losses.

As an example, an increase from 98,5 to 99% would reduce the losses by more than 1/3. In a 2,5MW wind turbine, this would represent reduction of the cooling power by 1kW and 420W in case of respectively forced-ventilation and water cooling.

Taking in consideration current feed-in-tariffs in Germany and assuming a capacity factor of 15% for the power converter, yearly energy savings of respectively 544kWh and 1.3MWh can be expected. Going further and making the calculations for a lifetime of 15 years and 50 €/MWh feed-in-tariff would result in overall savings of 408 and 972€. Such reduction comes together with less expenditure with cooling hardware, bringing additional savings.

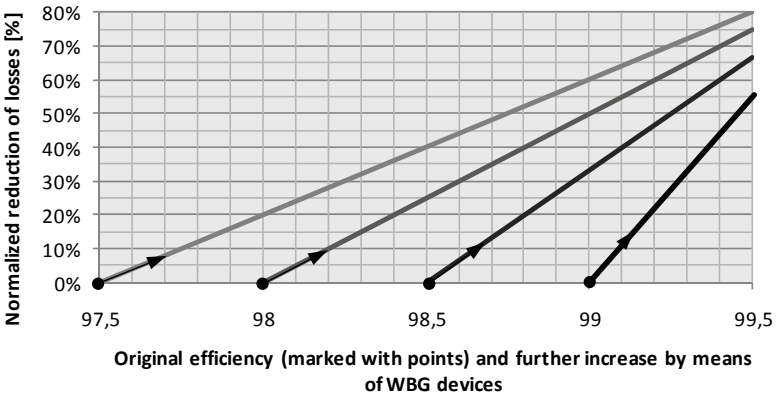


Fig. 98: Reduction of losses considering different levels of efficiency increase.

6 Application of WBG devices: chip area expenditure

The last application issue analyzed here is the possibility of reducing the expenditure with chip area, which is especially important to be considered with the application of WBG devices given their higher cost per chip area. This might be attained by making use of some of the properties of WBG devices, like the lower specific losses (static and dynamic), besides the high junction temperature capability. Each these possibilities is intrinsically linked with heat dissipation limits, as will be briefly discussed in this chapter. As a final remark, the analysis will be performed observing the properties of 1200V-rated Si and SiC devices, given the availability of data.

6.1. Analysis considering only conduction losses

When considering an application requiring a certain nominal current loading capability (I_{nom}), the required chip area (A_{chip}) can be calculated by considering the device specific chip resistance (R_{spec}) along with maximum chip specific power dissipation (P_{spec}). For the sake of simplicity, only conduction losses are for the time being considered.

$$A_{chip} = \sqrt{\frac{R_{spec}}{P_{spec}}} \cdot I_{nom} \tag{35}$$

It is now necessary to define ratio factors concerning the specific chip resistance and maximum loss dissipation from Si and SiC, as follows.

$$R_{spec\_Ratio} = \frac{R_{spec\_SiC}}{R_{spec\_Si}} \tag{36}$$

$$P_{spec\_Ratio} = \frac{P_{spec\_SiC}}{P_{spec\_Si}} \tag{37}$$

With these ratios, the possible reduction of the chip area using SiC (or other WBG material) for the same nominal current rating can now be calculated.

$$A_{chip\_reduction} = 1 - \sqrt{\frac{R_{spec\_Ratio}}{P_{spec\_Ratio}}} \tag{38}$$

Meanwhile, the attainable level of conduction losses with SiC normalized with the value for Si devices and considering the same conditions valid for equation above is given as follows.

$$P_{cond\_ratio} = \frac{R_{spec\_Ratio}}{\sqrt{\frac{R_{spec\_Ratio}}{P_{spec\_Ratio}}}} \tag{39}$$

Below are plotted both chip area economy and reduction of the conduction losses as a function of the ratio between the specific chip resistances, considering different ratios between the specific loss density. It is possible conclude that under assumption of same current rating and also same limit of specific losses, operation with SiC devices offers lower amount of conduction losses. Such reduction may in some cases be attractive in order to reduce the cooling expenditure as was already discussed, besides increasing the efficiency.

If this is nevertheless not of significant interest in a certain application, a better alternative would be increasing the level of specific losses, as this would enable higher economy with chip area, compensating the higher SiC material costs. Such possibility is also plotted in Fig. 99, as one can observe that the gain regarding higher specific loss density becomes less significant as the specific chip resistance ratio decreases. In this analysis, it was assumed that that operation at higher loss density was not achieved by higher chip temperature, as this may result in higher specific chip resistance leading to smaller level of chip economy.

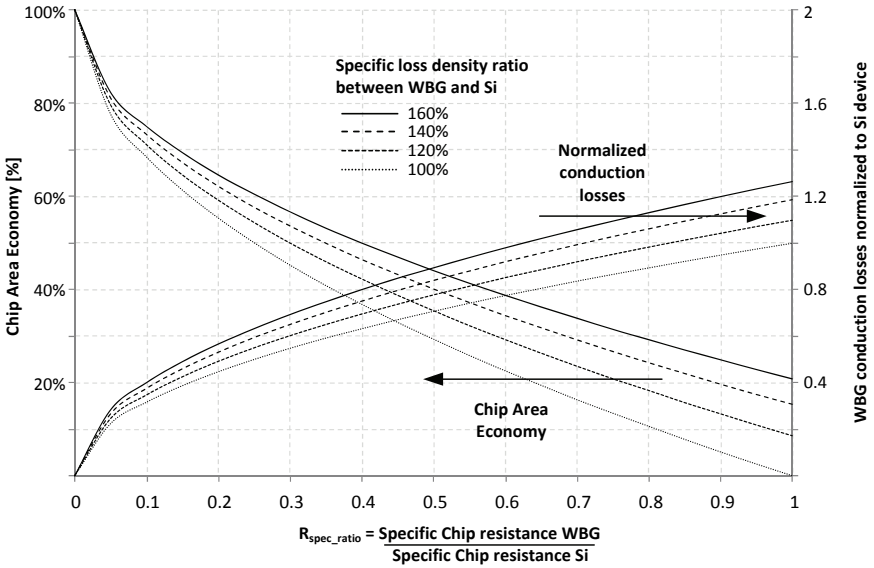


Fig. 99: Chip area economy and normalized conduction losses as a function of the ratio between the specific chip resistance values only considering conduction losses.

6.2. Analysis considering conduction and switching losses at same switching frequency

While the analysis presented above considered only conduction losses, in real applications the switching losses may take an important amount of the total semiconductor losses. In order to take such aspect in consideration, two new factors need to be defined. The amount of specific loss limit reserved to the switching losses (P_{spec_Psw}) from the total available value ($P_{spec\_material}$) is calculated with the factor $k_{Psw\_material}$.

$$k_{Psw\_materal} = \frac{P_{spec\_Psw}}{P_{spec\_material}} \tag{40}$$

In addition to this, it is also necessary to calculate the ratio (y_{Esw}) between the switching energy of SiC (E_{sw_SiC}) and Si devices (E_{sw_Si}).

$$y_{Esw} = \frac{E_{sw\_SiC}}{E_{sw\_Si}} \tag{41}$$

An important assumption taken in the analysis here is that for a given current rating, the switching energy is not affect by the device chip area. This was experimentally verified, as all 1200V SiC devices achieved for the same conditions practically the same switching energy levels, despite the different chip areas.

One first possibility considered here is that both technologies operate at the same switching frequency. Under such condition it is possible to calculate the amount of specific losses that need to be reserved for the switching losses in the SiC device.

$$k_{Psw\_SiC} = \left\{ \frac{k_{Psw\_Si} \cdot y_{Esw}}{2 \cdot P_{spec\_ratio} \cdot R_{spec\_ratio} \cdot (k_{Psw\_Si} - 1)} \cdot \left(k_{Psw\_Si} \cdot y_{Esw} - \sqrt{k_{Psw\_Si}^{\ 2} \cdot y_{Esw}^{\ 2} - 4 \cdot P_{spec\_ratio} \cdot R_{spec\_ratio} \cdot k_{Psw\_Si} + 4 \cdot P_{spec\_ratio} \cdot R_{spec\_ratio}} \right) \right\} \tag{42}$$

Plotting the factor above assuming different values of k_{Psw_Si} leads to the conclusion that the smaller the specific chip resistance is, the higher is the amount of specific losses that can be allocated to the switching losses (because the switching energy remains constant).

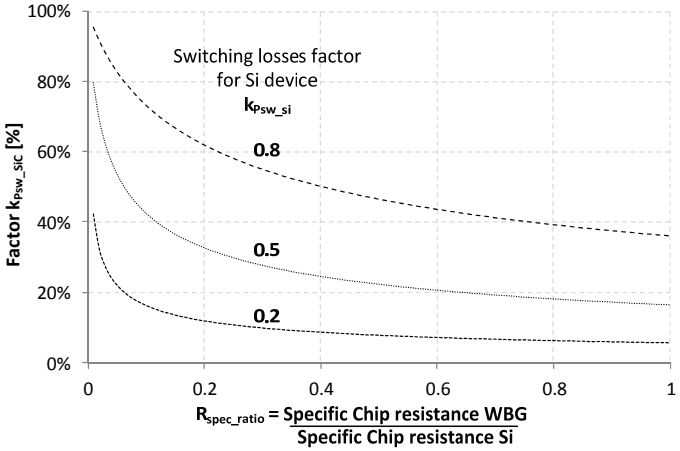


Fig. 100: Ratio of specific switching losses for the SiC device.

The ratio between the required SiC and Si chip areas can now be calculated with the following equation.

$$\frac{A_{chip\_SiC}}{A_{chip\_Si}} = \left\{ \frac{2 \cdot R_{spec\_ratio} \cdot (k_{Psw\_Si} - 1)}{k_{Psw\_Si} \cdot y_{Esw}} \cdot \frac{1}{\left(k_{Psw\_Si} \cdot y_{Esw} - \sqrt{k_{Psw\_Si}^{\ 2} \cdot y_{Esw}^{\ 2} - 4 \cdot P_{spec\_ratio} \cdot R_{spec\_ratio} \cdot k_{Psw\_Si} + 4 \cdot P_{spec\_ratio} \cdot R_{spec\_ratio}} \right)} \right\} \quad (43)$$

In the graph below are plotted the possible chip area economy along with total SiC device losses normalized to Si as a function of the specific chip resistance ratio. In addition to this, several ratios between the total specific loss limits are considered. In these calculations, is assumed that the overall losses in the Si device are equally divided between conduction and switching losses (k_{Psw_Si} equal to 0,5).

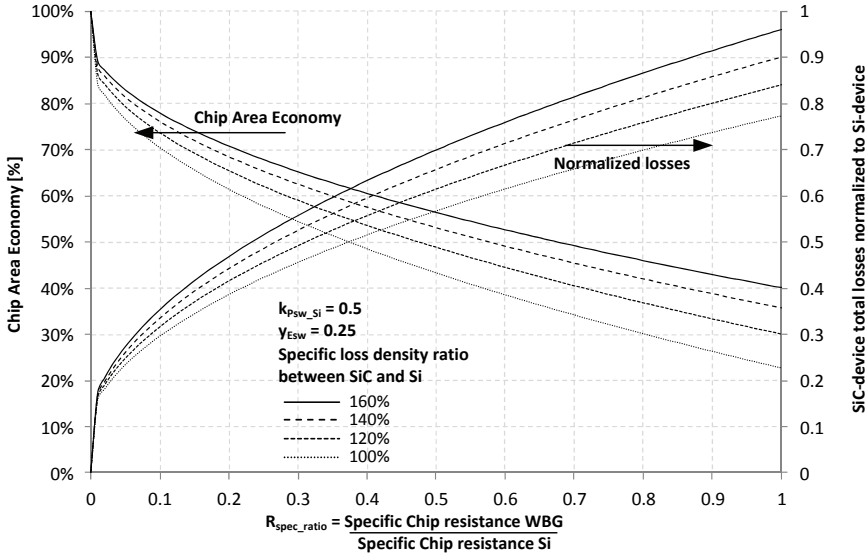


Fig. 101: Chip area economy and normalized losses as a function of the ratio between the specific chip resistance values considering operation at same switching frequency.

For operation at same switching frequency, the much lower level of switching energy from SiC devices enables not only a significant reduction on the required chip area, but also on the overall losses. Increasing the specific loss density for the SiC also results in certain gains regarding chip area savings, but also in higher losses likewise observed before. The obtained reduction on chip area becomes also

less significant with smaller ratios of specific chip resistance, placing in question the validity of operating at higher loss density in face of the related additional expenditure and complexity. Some additional curves are plotted in the picture below assuming a single maximum loss limit ratio, in order to also evaluate the impact of the ratio of the switching losses in the Si device (k_{Psw_Si}) and relative switching energy of SiC device (Y_{Esw}) on the results.

Comparing the red and blue curves, it is possible to observe that the advantages of employing SiC devices become even more evident when the switching losses are dominant for the Si device. Some additional gains may also be obtained by further reducing the switching energy of the SiC devices (continuous versus dashed lines).

From the results presented in this item, it possible to affirm that the operation at same switching frequency represents the scenario resulting in the maximum chip area savings.

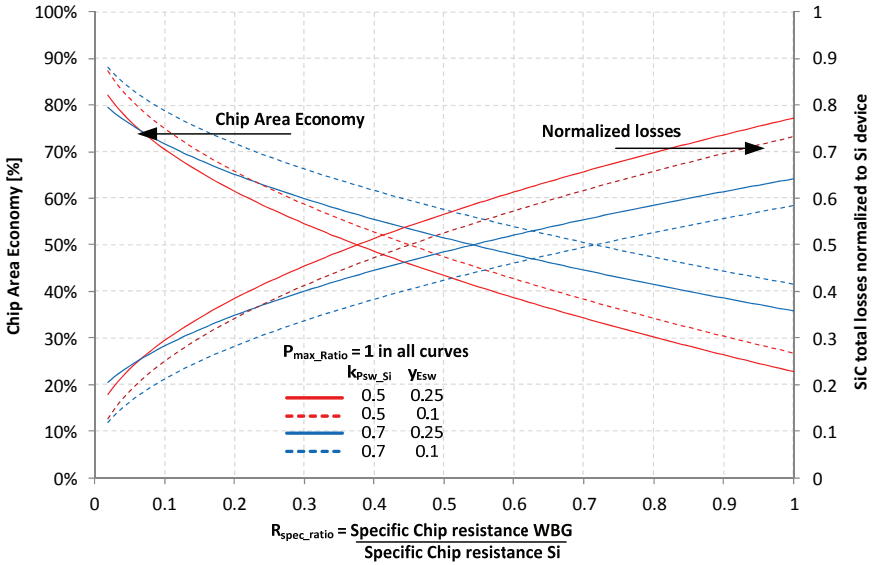


Fig. 102: Chip area economy and normalized losses as a function of the ratio between the specific chip resistance values considering operation at same switching frequency.

6.3. Analysis considering conduction and switching losses for different values of switching frequency

In order to allow savings with magnetics by high frequency operation, another analysis will be performed here considering that a certain ratio between the switching frequencies is desired.

$$f_{sw\_ratio} = \frac{f_{sw\_SiC}}{f_{sw\_Si}} \tag{44}$$

The new factor representing the amount of specific losses that need to be reserved for the switching losses in the SiC device is now calculated as follows.

$$k_{Psw\_SiC\_fsw} = \left[\frac{k_{Psw\_Si} \cdot y_{Esw} \cdot f_{sw\_ratio}}{2 \cdot P_{spec\_ratio} \cdot R_{spec\_ratio} \cdot (k_{Psw\_Si} - 1)} \cdot \left(\begin{array}{l} \sqrt{k_{Psw\_Si}^{\ 2} \cdot f_{sw\_ratio}^{\ 2} \cdot y_{Esw}^{\ 2} - 4 \cdot P_{spec\_ratio} \cdot R_{spec\_ratio} \cdot k_{Psw\_Si} + 4 \cdot P_{spec\_ratio} \cdot R_{spec\_ratio}} \\ -k_{Psw\_Si} \cdot f_{sw\_ratio} \cdot y_{Esw} \end{array} \right) \right] \tag{45}$$

The ratio between the required SiC and Si chip areas can be obtained with the following equation.

$$\frac{A_{chip\_SiC\_fsw}}{A_{chip\_Si}} = \left[\frac{1}{2 \cdot P_{spec\_ratio}} \cdot \left(\begin{array}{l} \sqrt{k_{Psw\_Si}^{\ 2} \cdot y_{Esw}^{\ 2} \cdot f_{sw\_ratio}^{\ 2} - } \\ \sqrt{-4 \cdot P_{spec\_ratio} \cdot R_{spec\_ratio} \cdot k_{Psw\_Si} + 4 \cdot P_{spec\_ratio} \cdot R_{spec\_ratio}} \\ +k_{Psw\_Si} \cdot y_{Esw} \cdot f_{sw\_ratio} \end{array} \right) \right] \tag{46}$$

The chip area economy is presented below, assuming different values of switching frequency and energy ratios. As was expected, one can clearly observe here that in order to operate at higher switching frequencies, less chip area economy is expected. In case of a switching frequency 6 times higher and a specific resistance ratio higher than 0.5, a larger chip area than the original one with Si will be

necessary. Going in the direction of higher frequencies might therefore be attractive only in the case the switching energy of the SiC devices is further reduced, as observed in the same graph with red lines.

The overall normalized device losses considering operation at higher switching frequency are also correspondently increased, as demonstrated in the graph below. Depending on the value of specific resistance, one may even need to cope with a higher amount of overall losses, increasing the cooling expenditure. The impact regarding a possible reduction of the switching energy (red lines) can now be clearly observed, especially at higher frequencies.

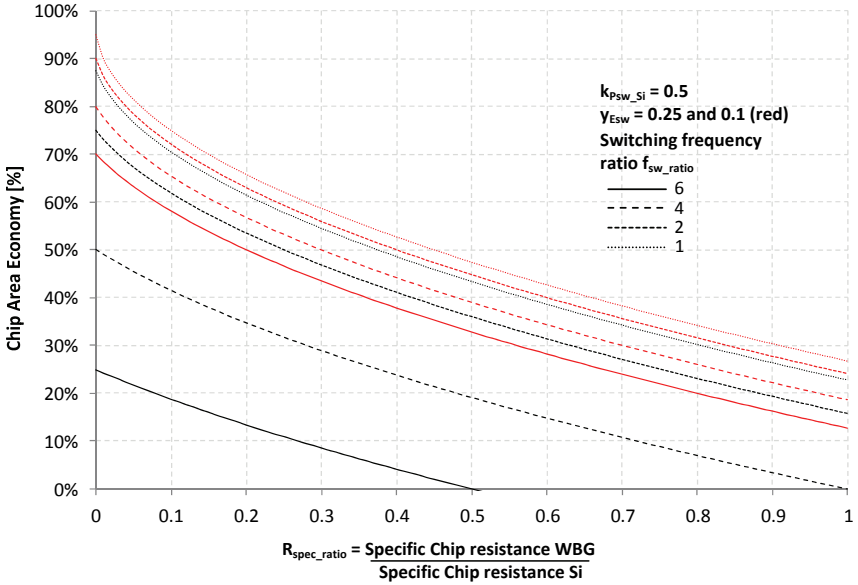


Fig. 103: Chip area economy as a function of the ratio between the specific chip resistance values considering operation at different switching frequencies.

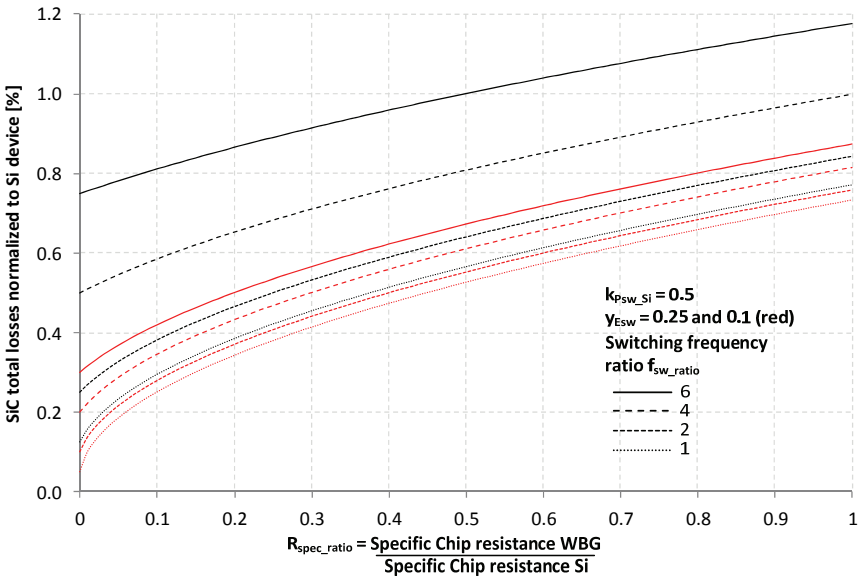


Fig. 104: Normalized losses as a function of the ratio between the specific chip resistance values considering operation at different switching frequencies.

7 Analysis on potential savings

From the so far presented analysis, it becomes clear that the different investigated properties of WBG devices clearly enable higher levels of power density given the possibility of reducing the volume expended with cooling (due to lower losses) and filter elements (given the higher switching frequency. This characteristic is normally required in highly-compact or mobile applications but has been so far not critical on the design of converters for renewable power systems. An overview of the values from commercial PV inverters is presented in Fig. 105 as a function of weight and exterior volume, with the distinction between the employed kinds of galvanic isolation.

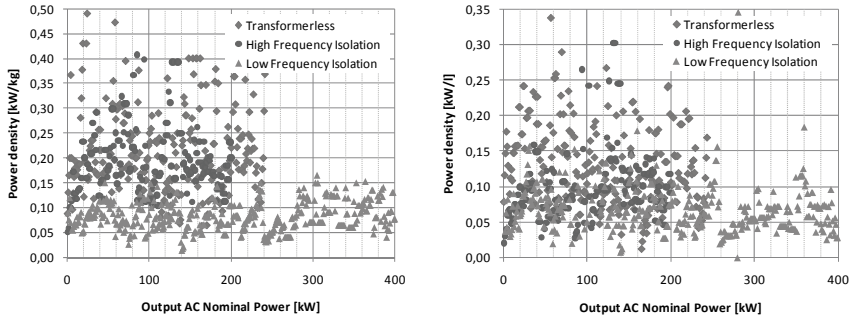


Fig. 105: Power density values regarding weight and volume of commercial PV inverters [8].

In average, levels around 0,22kW/kg and 0,15kW/l are achieved with systems employing high frequency transformer or no transformer, with slightly higher values for the last one. The use of low frequency transformers reduces such levels to on average 0,1kW/kg and 0,075kW/l. Wind power converter systems (without transformer, air-cooled) can on the other hand achieve values similar to the ones from high power drives, around 0,5kW/kg and 0,31kW/l [9], [10]. The significant difference observed from photovoltaic systems can be mainly explained by:

- lower voltage levels,
- higher pressure towards efficiency (what commonly leads to oversizing),
- integration of several safety and operational features in the same case,

In contrast, levels as high as 1kW/l and 3kW/l can be identified for respectively air conditioners and HEV inverters, while scientific publications are well above 20kW/l (considering only the volume with cooling and passive elements) [11] .

Rather than focusing on compactness alone, of interest here are two main possibilities enabled by higher power density as presented below. Both cases lead to a decrease of specific costs (€/kW) because of reduced material expenditure:

- size reduction with same power rating,
- power rating increase with same size.

The last prospect is more suitable for renewable energy systems which are by nature modular. This is the case of photovoltaic facilities, where the increase of power rating from the converter can be easily transmitted to the field by just adding more modules. In contrast, all other investigated sources are much less flexible concerning modification of power rating since this in practice requires a whole new system design.

Another key-issue to be considered regarding the application of WBG devices is the fact that their specific cost (regarding chip area) is and will remain higher than standard Si devices. It this therefore necessary to not only assert possible savings regarding higher power density as referred above, but also observe the trade-off regarding higher expenditure with semiconductors. The objective here is thus to identify the possible break-even point including different scenarios and device properties. Such analysis will be presented in the items 7.1 and 7.2 respectively focusing on photovoltaic inverters and back-to-back converters for wind systems. Later in the item 7.3, additional possibilities concerning savings at system level will be discussed.

7.1. Photovoltaic inverters operating at 16 kHz with IGBTs

Here both proposed approaches (size reduction or power rating increase) are investigated in order to identify which one might enable higher savings, along with inherent limitations or drawbacks.

7.1.1. Size reduction with same power rating

Because the power rating remains the same, it is necessary to only consider the overall specific cost normalized to the original design, which is here referred as P_{norm}.

For such purpose, the percental expenditure with magnetics, enclosure (cooling), semiconductors and the other elements is respectively represented by the factors K_{mag}, K_{enc}, K_{sem} and K_{rest}. Values are based on cost distributions found in the literature, as depicted below.

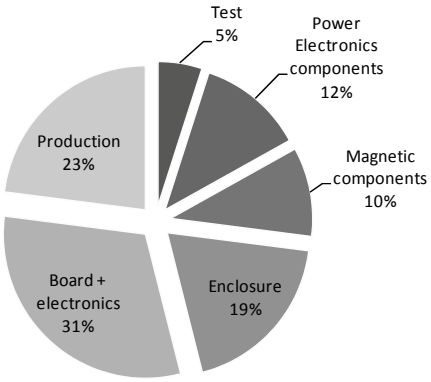


Fig. 106: Possible cost distribution of a transformerless photovoltaic inverter [284].

Meanwhile, possible changes in each of these factors (with the exception of K_{rest}) enabled by the application of SiC Technology are asserted by the factors X_{mag}, X_{enc} and X_{sem}.

The final cost of the system can be thus calculated with the following equation. This value is already normalized to original ones, given the calculation considering the percental cost distribution as previously explained.

$$P_{norm} = K_{mag} \cdot X_{mag} + K_{enc} \cdot X_{enc} + K_{sem} \cdot X_{sem} + K_{rest} \quad (47)$$

7.1.1.1. Cost reduction factors explanation

- Expenditure with magnetics (X_{mag})

The volume of magnetic filters (either DC or AC) can be approximated by the stored energy as previously discussed in the item 4.2.3. Under the assumption here that the power level (and consequently current) remains constant, the resultant volume change is directly dictated by the required inductance values and thus influenced by changes in switching frequency (as represented by the factor f_{sw_ratio}). Assuming that expenditure with magnetics is directly proportional to volume, it is possible to define the factor X_{mag} in the equation below. As an important remark, it

is here assumed that the material is still operating under non-critical levels of specific losses, thus enabling higher levels of switching frequency.

$$X_{mag} = \frac{1}{f_{sw\_ratio}} \cdot I_{ratio}^{\ 2} \ \rightarrow \ X_{mag} = \frac{1}{f_{sw\_ratio}} \ \text{assuming} \ I_{ratio} = 1 \tag{48}$$

- Expenditure with semiconductors (X_{sem})

The expenditure with semiconductors (power devices) is influenced by several factors like device technology, chip area expenditure, substrate costs and casing. In order to assert the cost impact of the adoption of WBG devices, it is necessary to make some considerations.

Firstly, the introduction of WBG technology does not affect all installed semiconductors. One first reason for this is that some devices switching at grid frequency in some circuits may well continue employing Si technology. In addition to this, several converters commercially available already employ SiC-diodes. Besides theses aspects at device level, wiring/bonding and casing are also responsible for a significant percentage of the overall expenditure. Under these considerations, the factor $\underline{n_{SiC}}$ defining how much of the overall original expenditure with semiconductors is being affected by the adoption of WBG devices is assumed as 60%.

The required chip area normalized to the value from the system with Si technology is here defined with the factor $\underline{A_{chip\_ratio}}$. The value takes in consideration the relations obtained in Section 3.2.1, assuming different values of specific chip resistance ratio R_{spec_ratio}.

Even if less chip area is required, higher material costs may in the end hinder gains with SiC-based devices. In order to take such fact in consideration, $Cost_{ratio}$ is defined as the ratio between the specific costs (€/cm²) of SiC and Si devices, considering not only substrate but also fabrication costs (epitaxy, casing). An initial value of 20 considering only the actual ratio between the specific substrate costs of SiC and Si [50] is considered, followed by 10 and 5.

Following the aspects discussed above, it is now possible to define the factor representing the expected expenditure with semiconductors as follows.

$$X_{sem} = 1 + n_{SiC} \cdot \left(A_{chip\_ratio} \cdot Cost_{ratio} - 1 \right) \tag{49}$$

- Expenditure with enclosure (X_{enc})

The last factor to be observed in the calculation is $\mathbf{X_{enc}}$, concerning the expenditure with enclosure. Given the fact that the cooling function is also integrated in the enclosure, it is important to consider not only the impact of the size reduction of

magnetic filters but also the loss reduction and consequent less cooling expenditure.

The proportion of the overall enclosure size taken by the magnetic components (represented by V_{ratio_mag}) strongly depends on the converter power rating, topology and finally on some specific design aspects. From the exploded views of some converters from the company SMA [7] as depicted below, it is possible to roughly estimate that the magnetics are responsible for at least 50% of the case volume.

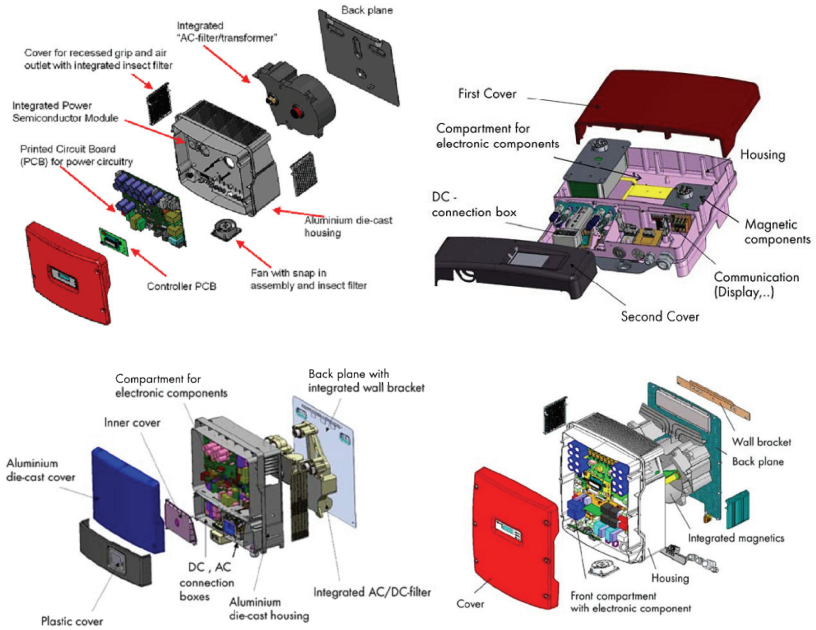


Fig. 107: Exploded view of photovoltaic converters from the company SMA [7].

Also from these pictures it is possible to make an estimation of the factor $V_{ratio\_heatsink}$ (proportion of enclosure volume taken by the heatsink) at about 15%. Given the fact that forced air cooling is in most cases employed, the assumed heat sink volume change is directly proportional to the obtained loss reduction. In order to assert such value, it is firstly necessary to assume a factor representing the amount of the overall losses being affected by the semiconductors, here given by the factor P_{loss_ratio}. The value of semiconductor losses from the system using SiC-devices normalized to the one from the Si-system is then represented by the factor $P_{loss\_SiC/Si}$, as was already calculated in the Chapter 6.

With all the previous consideration it is possible to calculate the factor representing the possible change on the expenditure with enclosure with the following equation.

$$X_{enc} = 1 + V_{ratio\_mag} \cdot \left[X_{mag} - 1 \right] + V_{ratio\_heat\,sink} \cdot \left[P_{loss\_SiC/Si} \cdot P_{loss\_ratio} - 1 \right] \tag{50}$$

The final overall normalized cost is calculated by the following equation:

$$P_{norm} = \left[\begin{array}{l} K_{rest} + K_{mag} \cdot \left(\dfrac{1}{f_{sw\_ratio}} \right) + \\ \quad + K_{enc} \cdot \left[\begin{array}{l} 1 + V_{ratio\_mag} \cdot \left(\dfrac{1}{f_{sw\_ratio}} - 1 \right) + \\ + V_{ratio\_heat\,sink} \cdot \left(A_{chip\_ratio} \cdot P_{spec\_ratio} \cdot P_{loss\_ratio} - 1 \right) \end{array} \right] + \\ \quad + K_{sem} \cdot \left[1 + n_{SiC} \cdot \left(A_{chip\_ratio} \cdot Cost_{ratio} - 1 \right) \right] \end{array} \right] \tag{51}$$

with $A_{chip\_ratio} =$

$$= \left[\frac{1}{2 \cdot P_{spec\_ratio}} \cdot \left(\begin{array}{l} \sqrt{k_{Psw\_Si}^{\,2} \cdot y_{Esw}^{\,2} \cdot f_{sw\_ratio}^{\,2} - } \\ \sqrt{-4 \cdot P_{spec\_ratio} \cdot R_{spec\_ratio} \cdot k_{Psw\_Si} + 4 \cdot P_{spec\_ratio} \cdot R_{spec\_ratio}} \\ + k_{Psw\_Si} \cdot y_{Esw} \cdot f_{sw\_ratio} \end{array} \right) \right]$$

7.1.1.2. Analysis results for reference Si-system with equal share of conduction and switching losses

The converter cost of the system employing SiC devices normalized to the one with Si devices is presented in Fig. 108, taking in consideration the factors in the table below. In a first step different values of specific cost ratios ($Cost_{ratio}$) and values of loss density (P_{spec_ratio}) are investigated, considering same switching frequency and higher level of specific losses due to better heat spreading (and not higher junction temperature).

Table 9 – Factors employed in the calculation (otherwise specified on the graphic).

Factor	Value	Explanation
K_{mag}	0,15	Proportion of overall costs affected by magnetics
K_{enc}	0,2	Proportion of overall costs affected by enclosure
K_{sem}	0,12	Proportion of overall costs affected by semiconductors
K_{rest}	0,53	Rest of overall costs
y_{Esw}	0,25	Switching losses of SiC device normalized to Si
V_{ratio_mag}	0,5	Proportion of enclosure volume affected by magnetics
$V_{ratio\_heatsink}$	0,15	Proportion of enclosure volume affected by heatsink/cooling
n_{SIC}	0,6	Proportion of expenditure with semiconductors affected by adoption of SiC devices
P_{loss_ratio}	0,7	Proportion of the overall losses being affected by the semiconductors
P_{spec_ratio}	1	Ratio between specific chip losses (W/cm²) between SiC and Si devices
k_{Psw_Si}	0,5	Distribution between switching and conduction losses of system using Si devices

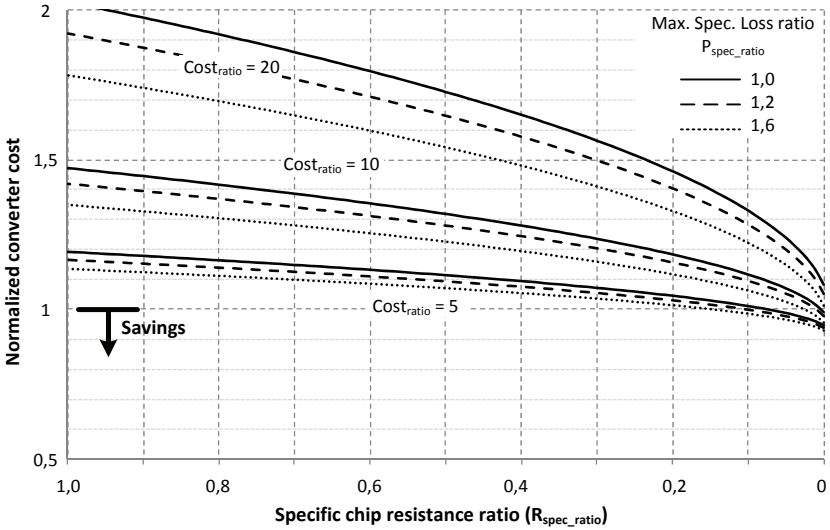


Fig. 108: Normalized cost as a function of the specific chip resistance ratio, for different values for semiconductor material costs ratio ($Cost_{ratio}$) and specific loss ratios, but same switching frequency.

One first interesting result is that for the assumed conditions above, only marginal savings are obtained, even for reduced device specific costs and very low values of specific chip resistance. Operating with higher loss density on the other hand brings some gains but tends to lose importance with reducing device costs. In order to better understand the influence of each factor on the overall cost, the individual distribution is presented below with two different values of switching frequency ratio and two values of material cost ratio factor ($Cost_{ratio}$).

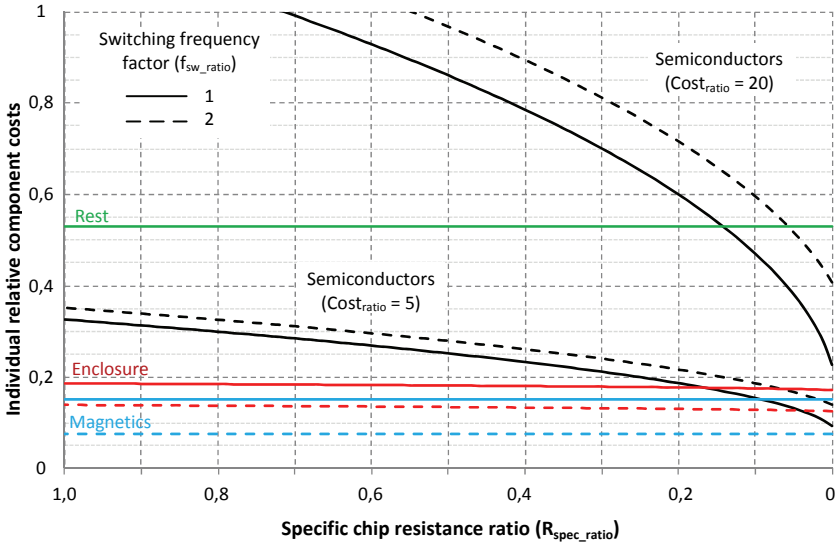


Fig. 109: Individual costs distribution as a function of the specific chip resistance ratio, assuming two different values for semiconductor material costs ratio ($Cost_{ratio}$) along with three different values of switching frequency ratio.

From these results it is possible to draw some preliminary results:

- The expenditure with semiconductors dominates the overall system costs employing SiC devices, mainly due to the much higher material costs. Only with much lower costs ($Cost_{ratio}$ = 5) is the share of semiconductors similar to enclosure and magnetics.
- Operation at higher switching frequency brings significant gains for both enclosure and magnetics, but these gains are in part superseded by the larger amount of chip area required to cope with the additional losses.
- The influence of the specific chip resistance on the enclosure reduction (through reduction of the losses) is marginal, when compared with the gain due to higher switching frequencies.

From some of the above presented points it becomes clear that the overall cost reduction potential due to higher switching frequencies may be rather limited in case either the power devices have a high specific cost or magnetics have a marginal participation on the overall costs. Such fact is depicted below, with plots for three different values of switching frequency, assuming now same value of specific losses.

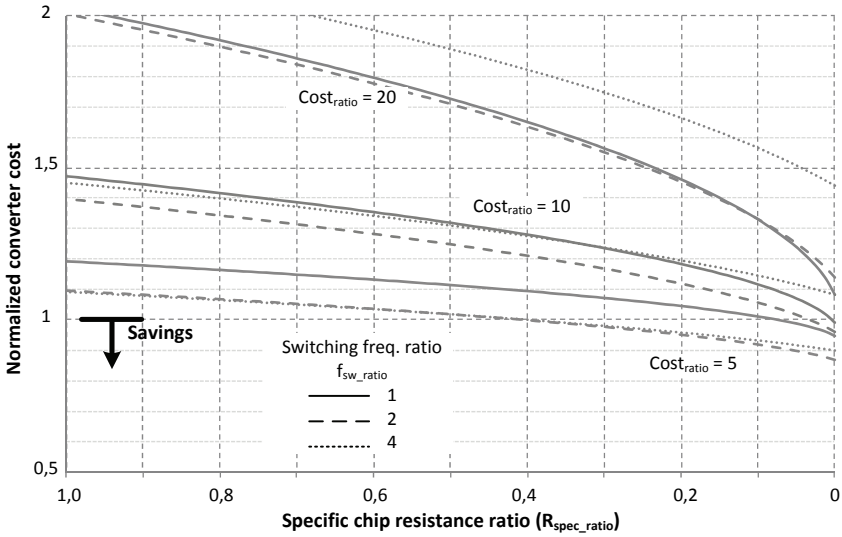


Fig. 110: Normalized cost calculation as a function of the specific chip resistance ratio, assuming three different values of switching frequency.

From these results, one can clearly observe that the higher the device material costs are, the less attractive is the operation at higher switching frequency. Of interest here is therefore to try to identify the optimal switching frequency value in order to attain minimal overall cost. Such aspect is investigated in the next graph, as the costs are plotted as function of the switching frequency ratio, considering different values of cost ratios (line color) and specific chip resistance values (line style).

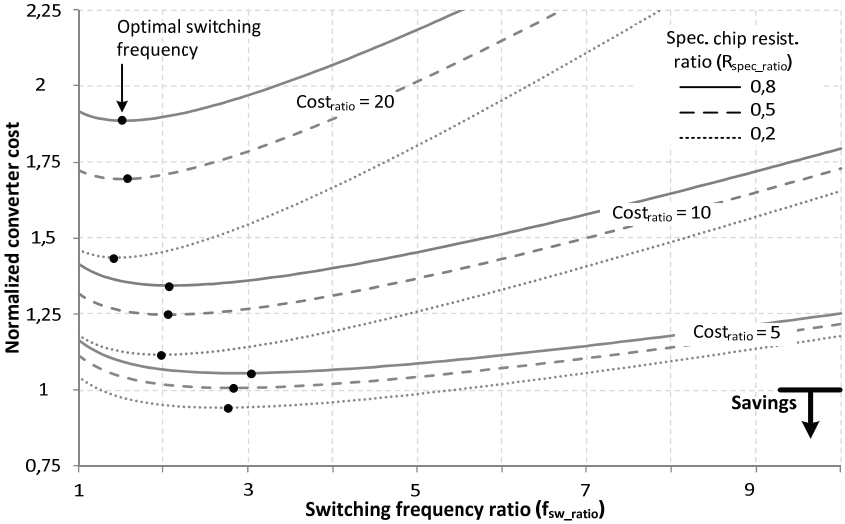


Fig. 111: Normalized cost calculation as a function of the specific chip resistance ratio, assuming three different values of switching frequency.

The range of the optimal frequency tends to increase with falling material cost ratios, while the specific chip resistance has only a rather minor effect on it. From the so far presented results it becomes clear that for the assumed conditions the application of SiC hardly brings any benefits regarding cost savings.

7.1.1.3. Analysis results for reference Si-system with dominant switching losses

Another scenario to be analyzed here considers a reference system employing Si devices where the switching losses are dominant. In this case, the k_{Psw_Si} is assumed to be 0,8 (with curves for 0,5 also depicted for comparison). Due to higher weight of the switching losses on the original design with Si, the lower switching energy of SiC devices can now be directly translated in less chip expenditure and thus higher savings. In case of material device costs ratio equal to 5, increased gains can also be obtained when doubling the switching frequency. One final possibility now is to consider a further reduction of the switching energy of the SiC devices, mainly feasible when operation at higher values of di/dt and dv/dt is considered.

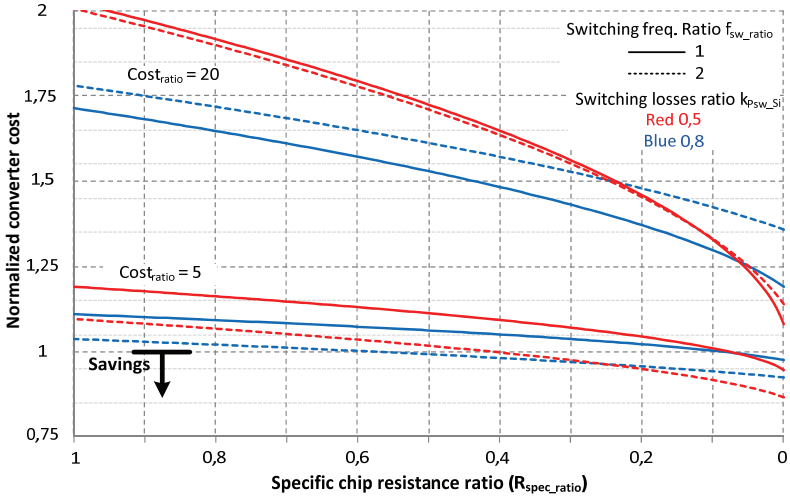


Fig. 112: Normalized cost as a function of the specific chip resistance ratio, assuming two different values of switching frequency and device material costs.

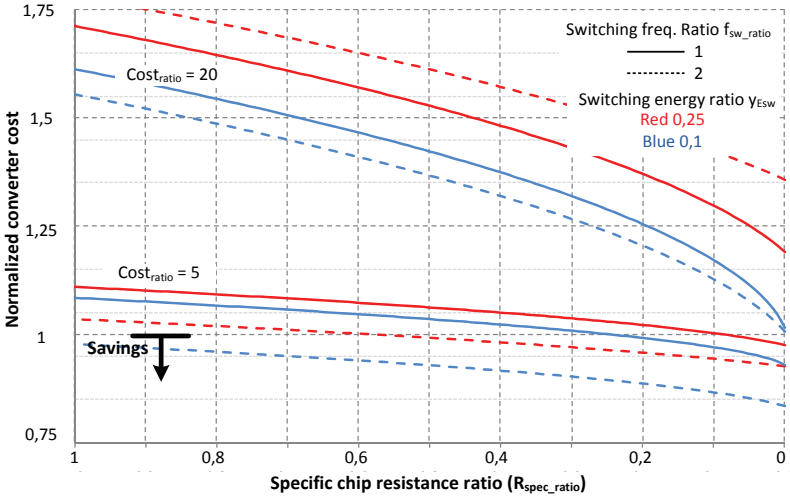


Fig. 113: Normalized cost as a function of the specific chip resistance ratio, with two different values of switching frequency, two relative device material costs and two different switching energy ratios.

From these results it is possible to identify three main aspects. Firstly, the lower amount of switching energy (red and blue lines compared) and consequently lower overall losses allows lower chip expenditure, being especially attractive in the case of higher material cost ratings. The increase of the switching frequency (continuous and dashed lines) becomes in the case of lower switching energy attractive, even at higher material costs.

7.1.2. Power rating increase with same size

Of interest now is to investigate the alternative of maintaining the equipment size and increasing the power rating by making use of properties from SiC devices. Considering a constant output voltage, the higher power rating can be directly translated in an increase of the output current, here assumed as the factor I_{ratio}, which is obtained by the division between the output currents of the converter employing SiC (I_{out_sic}) and Si devices (I_{out_si}).

$$I_{ratio} = \frac{I_{out\_SiC}}{I_{out\_Si}} \tag{52}$$

Meanwhile, the enclosure size needs to remain constant. One first possibility consists on the individual size of the heatsink and magnetics remaining unchanged. A second approach considers that only the sum rather than the individual values needs to remain constant. Making use of the previously defined factor X_{enc}, it is thus necessary to maintain the relation below. An advantage here is the additional degree of freedom regarding possible changes on either heatsink or magnetics, enabling further savings depending on the cost distribution.

$$X_{enc} = 1 \quad \rightarrow \quad V_{ratio\_mag} \cdot \left[X_{mag} - 1 \right] = V_{ratio\_heat\,sink} \cdot \left[1 - P_{loss\_SiC/Si} \cdot P_{loss\_ratio} \right] \tag{53}$$

Because of the increasing expenditure with semiconductors (due to higher material costs), it is necessary not only to observe the possible increase of the nominal power, but rather the resultant change on the specific cost (cost/power), as happened in the previous analysis.

Here the investigation is focused on the assumption that the individual sizes of the heatsink and magnetics remain the same. In the case of the magnetics, similar assumptions as made in the item 7.1.1.1 are also taken here, namely considering that the core is not operating near the limit of the specific losses and that no limitation of the flux swing is necessary. The change in the size of the output filter can thus be directly accessed by the factor X_{mag}, defined now in order to take in account the targeted change in the current level. In case such factor remains constant, each increase on the current rating can be taken as the square root of the frequency change.

$$X_{mag} = \frac{1}{f_{sw\_ratio}} \cdot I_{ratio}^{\ 2} \ \rightarrow \ I_{ratio} = \sqrt{f_{sw\_ratio}} \ \ assuming \ X_{mag} = 1 \tag{54}$$

On the other hand, for the semiconductors it is necessary to calculate the possible increase of the factor I_{ratio} under consideration that the overall level of losses remains the same. For the same value of specific chip losses limit, it is possible to directly infer that both systems with Si and SiC devices will thus require the same chip area.

$$A_{chip\_Sic} \cdot P_{spec\_SiC} = A_{chip\_Si} \cdot P_{spec\_Si} \tag{55}$$

This enables obtaining the current ratio factor as given in the equation below. Here it is assumed that the switching losses increase directly proportional to the current level.

$$I_{ratio} = \frac{\sqrt{k_{Psw\_Si}^{\ 2} \cdot f_{sw\_ratio}^{\ 2} \cdot y_{Esw}^{\ 2} + P_{spec\_ratio} \cdot R_{spec\_ratio} \cdot (4 - k_{Psw\_Si})} - k_{Psw\_Si} \cdot f_{sw\_ratio} \cdot y_{Esw}}{2 \cdot P_{spec\_ratio} \cdot R_{spec\_ratio} \cdot (1 - k_{Psw\_Si})} \tag{56}$$

The possible increase on the power rating considering only the semiconductor losses is presented in Fig. 114 as a function of the specific chip resistance ratio for different values of switching frequency and maximum specific losses factors. Devices with lower specific chip resistance will enable higher output current given the lower amount of losses, while increasing the switching frequency, as expected, limits possible gains.

In addition to this it is interesting to observe here that increasing the loss density leads in fact to lower current rating. Reason for this is that the higher loss density directly results in smaller chip area in order to keep the overall losses constant, what in turn leads to the referred reduction of the current ratio. Such fact can also be observed from the relation between the nominal chip current ($I_{nominal}$) with the chip area and loss density as given below.

$$I_{nominal} \propto \frac{A_{chip\_material}}{\sqrt{P_{spec\_material}}} \tag{57}$$

When the achievable current ratting levels regarding semiconductor and magnetics are simultaneously considered, some of the curves presented in Fig. 114 are limited as presented in Fig. 115.

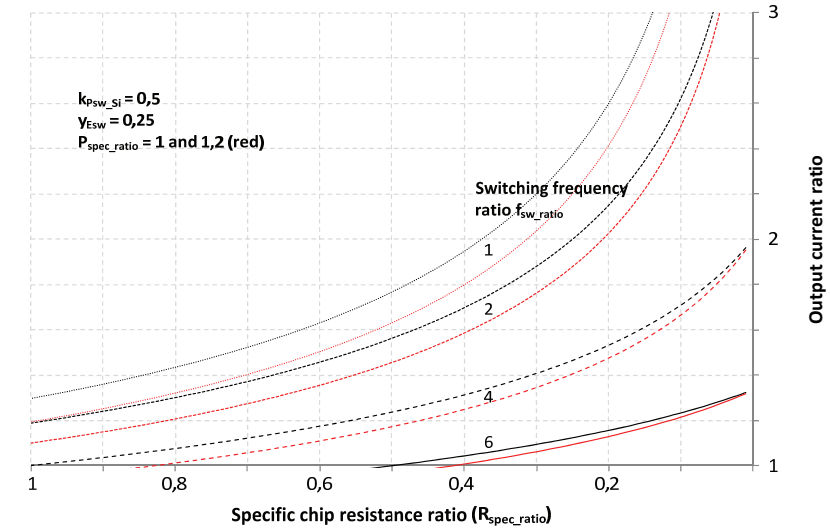


*Fig. 114: Output current ratio **only** considering constant semiconductor losses.*

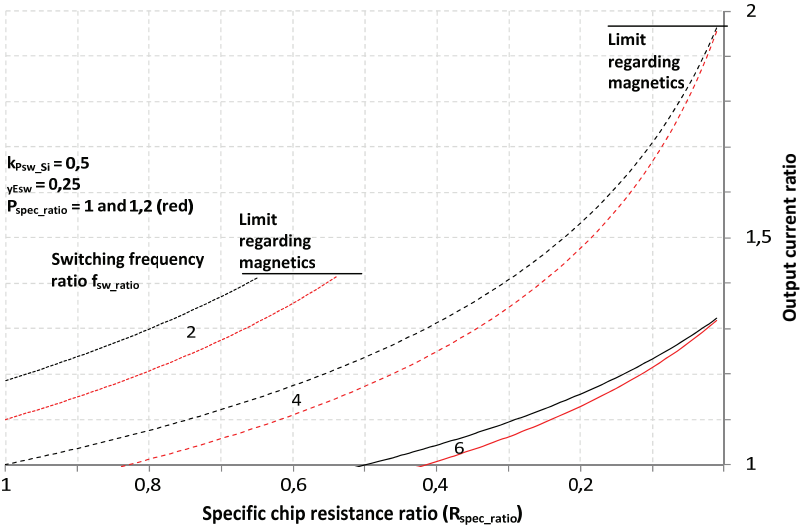


Fig. 115: Output current ratio considering constant semiconductor losses and size of magnetics.

Of interest is now to plot the normalized cost obtained by the division between the increased expenditure (due to the semiconductors) along with possible increase of power rating. From the curves presented below, similar conclusions as the ones already obtained with the first approach (with size reduction) are attained. In the case of lower semiconductor material costs, savings might be attainable already with operation at double the switching frequency. Increasing the switching frequency further might be interesting only in case of much lower specific chip resistances, in order to extend the possible current rating of the magnetics.

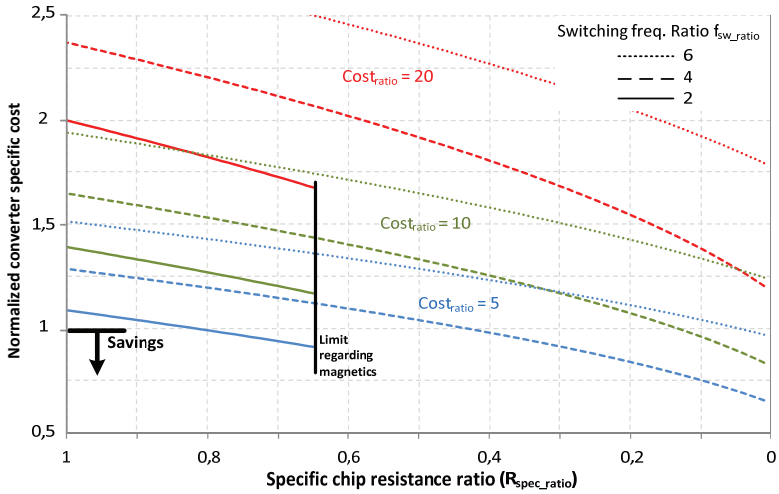


Fig. 116: Specific cost as a function of specific chip resistance for different values of switching frequency and material cost, assuming k_{Psw_Si} =0,5 and Y_{Esw} = 0,25.

7.1.3. Comparison between approaches

In the graph below are presented the normalized converter costs considering the two previously proposed approaches. The switching frequency factor is kept at 4 and three different material cost ratios are considered.

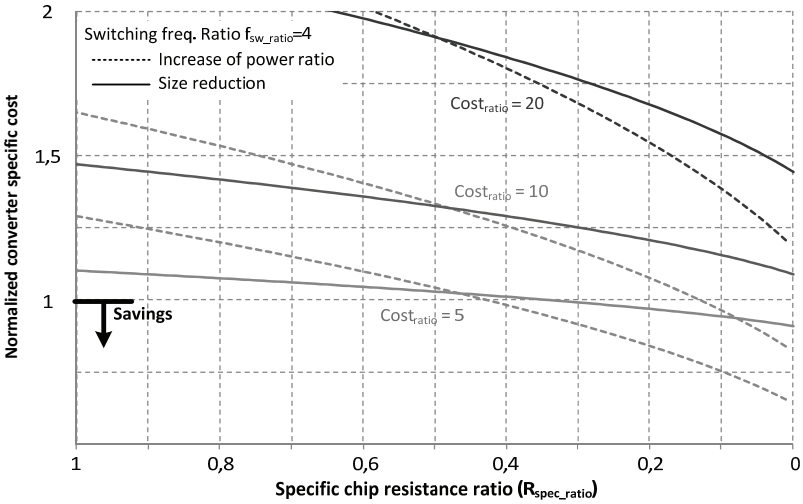


Fig. 117: Comparison between analyzed approaches assuming k_{PSw_Si} =0,5 , y_{Esw} = 0,25 and f_{sw_ratio} = 4.

From these results it is possible to assert that in the direction of lower values of specific chip resistance, it is more attractive to invest on possible increase of power rating under the same overall size. The main reason for this is the fact that for such approach, only the semiconductor expenditure is being modified in order to cope with the higher power rating. Any reduction on the semiconductor expenditure, either by lower material costs or smaller chip resistances, will thus lead to more attractive results.

7.2. High power back to back converter

The same analysis presented in the item 7.1.1 will now be performed considering a back-to-back converter employed in wind power systems. Given the fact that the application of SiC devices is more attractive in systems where the switching losses are dominant, the reference Si-based system will employ 1700V-rated devices. In addition to this, only the approach regarding size reduction with same power rating will be considered.

One assumption taken here is that the DC-link capacitor sizing is not directly affected by the switching frequency of the bridges, as its size is mainly dictated by other factors like system dynamic characteristics (including generator and grid) along with control strategy [51],[52],[53].

The percental expenditure with output sinus filter, cooling, semiconductors and the other elements is respectively represented by the factors K_{mag}, K_{heat}, K_{sem} and K_{rest}, being taken from the cost distribution presented below.

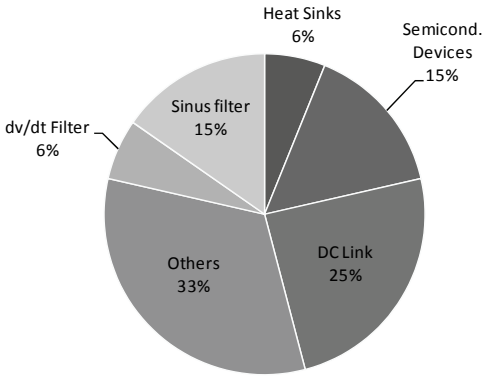


Fig. 118: Cost distribution for a back-to-back converter (active rectifier and inverter) [285].

Meanwhile, possible changes in each of these factors are asserted by the factors X_{mag}, X_{heat} and X_{sem}. The overall normalized cost, is calculated with the following equation.

$$P_{norm} = K_{mag} \cdot X_{mag} + K_{heat} \cdot X_{heat} + K_{sem} \cdot X_{sem} + K_{rest} \tag{58}$$

7.2.1.1. Factors explanation

The output filter will be affected here in a similar way as it was presented in the item 7.1.1, i.e. directly proportional to the inverse of the frequency modification.

$$X_{mag} = \left(\frac{1}{f_{sw\_ratio}} \right) \tag{59}$$

Meanwhile, the analysis of the expenditure with semiconductors is more complex here due to the existence of two converters. Despite different stress conditions of diodes and switches in the rectifier and inverter stages, the same model of IGBT module is normally employed for both stages. In addition to this, both switch and diode also have similar maximum current ratings, with the specific chip resistance of the diodes being roughly the half of the ones from IGBTs (following research of SPT+ chips from ABB). The factor n_{sic} representing the fraction of overall

semiconductor costs affected by the application of SiC switches is therefore selected as 0,6.

$$X_{sem} = 1 + n_{SiC} \cdot \left(\frac{A_{chip\_SiC\_fsw}}{A_{chip\_Si}} \cdot Cost_{ratio} - 1 \right) \quad (60)$$

Finally, the factor representing the expenditure with the cooling takes in account the reduction of the losses due to the use of the SiC devices. From the research presented in the item 5.2.2, it is possible to affirm that the required expenditure with cooling can be approximately considered to be directly proportional to the level of power losses to be dissipated. Following some calculations considering the operation of both active rectifier and inverter stages with 1700V-rated devices, it is possible to affirm that approximately 55% of the overall losses can be allocated to the switches, being represented by the factor V_{heat_SiC}.

$$X_{heat} = 1 + V_{heat\_SiC} \cdot \left[P_{loss\_SiC/Si} - 1 \right] \quad (61)$$

7.2.1.2. Analysis results

The factors employed in the calculations here are summarized in the table below. Considering the application of 1700V rated devices, the amount of switching losses calculated for a Si converter operating at 3 kHz is in average 66%. In addition to this, the switching energy factor y_{Esw} is in this case roughly 0,15 considering experimental data obtained with 1600V-rated IGBTs.

Table 10 –Cost analysis calculation factors (otherwise specified on the graphic)

Factor	Value	Factor	Value
K_{mag}	0,15	y_{Esw}	0,25
K_{heat}	0,06	V_{heat_SiC}	0,55
K_{sem}	0,15	n_{SIC}	0,6
K_{rest}	0,64	k_{Psw_Si}	0,66

In comparison with the results obtained with the photovoltaic inverters, the cost levels here are slightly lower due to the better dynamic performance of the SiC devices and the higher weight of the switching losses. It can nevertheless be observed that savings can be attained only in the case of lower material costs. Another possibility investigated here is the potential gains obtained with operation at higher switching frequency, as depicted below. Compared with the previously

obtained results it is possible to affirm that higher switching frequencies bring some gain only under lower semiconductor material costs. A further limitation regarding the possible influence of higher switching frequencies is that its impact on the enclosure through the magnetics is not considered here.

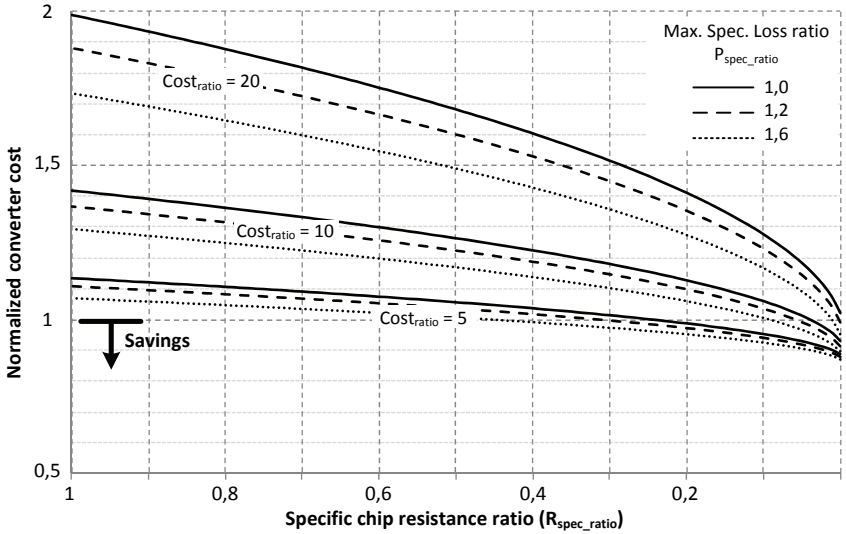


Fig. 119: Normalized cost as a function of the specific chip resistance ratio, with different values for semiconductor material costs ratio ($Cost_{ratio}$) and for specific loss ratio, with same switching frequency.

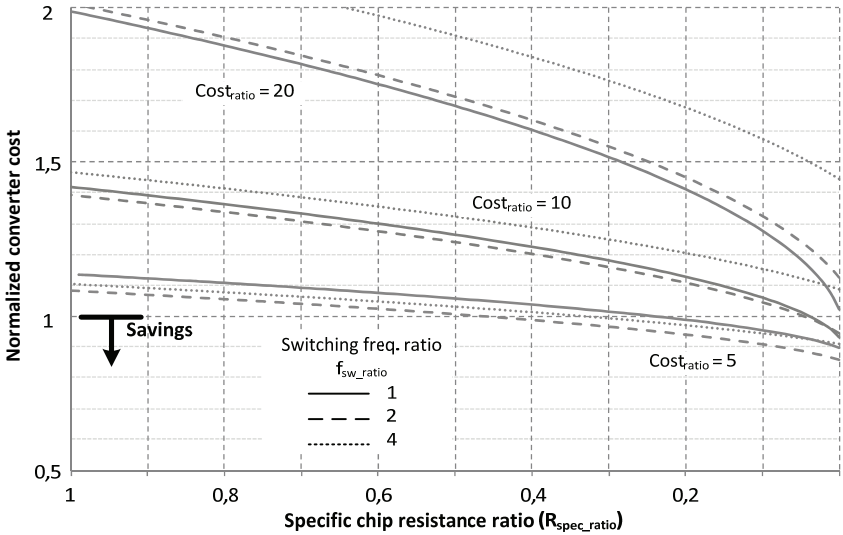


Fig. 120: Normalized cost calculation as a function of the specific chip resistance ratio, assuming three different values of switching frequency.

7.3. Additional savings

7.3.1. Photovoltaic systems

Besides the referred potential savings at converter level, it is also possible to identify some interesting possibilities at system level. One of them is increasing the voltage levels when operating at higher power ratings. For the case of photovoltaic systems connected to the medium voltage grid with transformer, raising the system voltage from 1000 to 1500V enables up to 40% saving of cooper cross-section area for the same power level and expected cabling losses. In transformerless converters, additional savings may be attained by sparing a whole power stage, as will be later discussed in details in the item 8.3.

7.3.2. Wind-power systems

In the path towards ever increasing power ratings, systems operating medium-voltage generators are gaining importance in the market. Multibrid and 6M focus on offshore applications and the chosen voltage levels come as a consequence of the higher power rating. In the particular case of the Multibrid, the higher voltage

enables the placement of the turbine transformer in a lower part of the tower, allowing reduction on the nacelle size and weight. On the other hand, the turbines from Acciona aim for the elimination of the individual turbine transformers, enabling direct connection to the local farm grid with lower losses and expenditure. In the referred systems rated at medium voltage, multilevel circuits and high voltage blocking devices like 4,5kV IGCTs and more rarely IGBTs are employed.

In these systems, the use of SiC devices rated at several kVs could not only enable significant savings in chip area but also reduce the size of filter elements, given the very low switching frequency of the referred high voltage Si devices. This would in turn enable additional gains regarding mechanical stress of the nacelle and installation complexity, being especially of interest in the case of offshore turbines.

Regarding the possible use of SiC switches, some constraints still need to be considered. Firstly, the power levels of wind energy conversion stages are normally more than 6 times higher than the ones found in central PV inverters. This consequently leads to different mounting and construction techniques characterized by higher stray inductances resulting in overvoltages in case of increased values of di/dt. On the other hand, high dv/dt will place the isolation of the generator, output filter and transformer under increasing stress due to possible impact ionization [286], [287]. This last problematic becomes increasingly important for systems operating with long connection cables due to the possible voltage reflection effect [288], [289]. The presented potential for reduction of switching losses may thus be lower than the one estimated before and can only be truly evaluated when investigating in details possible module constructions and system specific limitations.

Another requirement in wind power systems is the increased overload capability in face of wind gusts and other mechanical transients. As a consequence, a larger chip area than the one required for nominal conditions is normally installed, as this not only enables a better distribution of losses but also increases the system thermal capacitance. An alternative to larger chip areas is to enable higher junction temperatures.

At first glance, the above referred overload requirement comes in opposition to the desired chip area reduction for SiC in order to compensate the higher specific material costs. While such diminution will definitely decrease the overall thermal capacitance, the possibility of operating under very high junction temperature levels not only compensates such problematic but also may extend the overload capabilities. While 200°C is regarded as the limit for Si devices, SiC can go up to 600°C without affecting the device correct operation. Making use of such capability still nevertheless requires intense research in module and bonding construction due to the increased thermal and mechanical stresses. An analysis

regarding the overload capability under consideration of the referred material properties along with practical values of specific resistance for the investigated devices is presented in the graphic below. With a chip area approximately 50% smaller than the one from the Si IGBT, the SiC device could still enable an overload of more than two times the nominal value for a temperature gradient between junction and heatsink of 300K. The slow saturation of the curve is caused by the increase on the device resistance at higher temperatures.

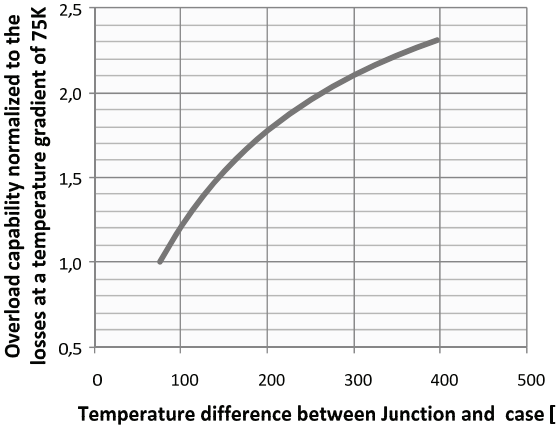


Fig. 121: Possible overload capability as a function of maximum temperature gradient between heat junction and case.

8 Experimental investigations

This final chapter will present some application examples employing SiC devices that were experimentally investigated, followed by some conclusions.

8.1. Effect of different semiconductor configurations on a single stage photovoltaic inverter [59]

In a first step, a preliminary investigation of the influence of different semiconductor technologies will be performed taking a novel single-phase inverter for photovoltaic systems.

8.1.1. Selected topology

The basic principle of operation of the selected topology depicted below relies on two paralleled step-down converters that modulate a rectified sinusoidal current, with the output connected to the load using opposite polarities. The circuit was obtained by modifying the power flow direction on one of the circuits proposed in [60] and discussed in details in [61]. The components of each step-down converter responsible for the positive and negative half waves can be respectively identified as T_1-L_1-D_1-T_4 and T_2-L_2-D_2-T_3. V_{in} represents a photovoltaic array as the input source and V_{out} the utility grid in the output. D_3 and D_4 are clamp-diodes to protect the switches located on the grid side against possible transients.

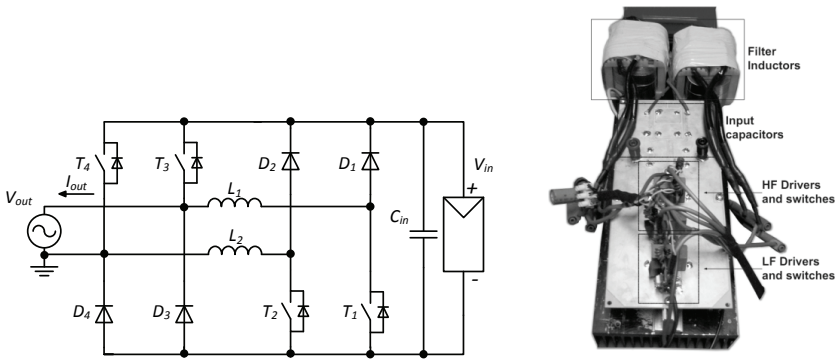


Fig. 122: Single phase inverter topology employed in the tests and prototype photo.

A first advantage of the proposed circuit is the possibility of operating with a single high frequency switch (T_1 or T_2) at a time what significantly reduces the switching losses. The other switches (T_3 and T_4) are under a voltage stress equal to the grid voltage and operate only at grid frequency, so that they can be further optimized for reduced conduction losses. Since the positive terminal of the PV-array is either directly connected to the phase output during the positive half-wave and to the neutral during the negative half-wave; not only are high frequency oscillations and consequently leakage currents avoided, but also the negative voltage across the cell is well suited for application with back-side contact cells [17]. A laboratory prototype of the circuit presented above was constructed with a nominal power of 4,5kW, input voltage range of 375-600V, output 230V± 10%, switching frequency at 16 kHz and output filter equal to 3mH.

8.1.2. Tested semiconductor configurations

Tests were performed with different semiconductor configurations in order to evaluate the potential of the different technologies under equal operating conditions. For such purpose, all measurements were done with resistive load rather than directly feeding the grid, so that the influence of the changing grid voltage would not affect the results [62]. In addition, the measured efficiency considers only the power stage, without any external power supply. The power required by the gate drivers may change depending on the chosen semiconductor (gate charge value), switching frequency and speed; though increases well below 0.15W were observed and hence considered as non-significant on the rated power level.

For each configuration, the efficiency measurement was performed with a wide-band precision power analyzer LEM Norma D-6000, at three-different voltage levels. The first one was the minimum specified MPP voltage, in this case 375V, as with this value the highest level of efficiency is attained. More significant are nevertheless the levels at 435V and 500V, where most of the produced energy from the PV-array is obtained. On the table below are summarized the tested configurations.

Table 11 – Tested semiconductor configurations

	T1 – T2	T3 – T4	D1 – D2
1	Trench IGBT 1stG 25A/1200V	Trench IGBT 1st G 30A/600V	Stealth Diode 30A/ 1200V
2	Trench IGBT 1stG 25A/1200V	2nd G CoolMOS 38A/650V	Stealth Diode 30A/ 1200V
3	Trench IGBT 1stG 25A/1200V	2nd G CoolMOS 38A/650V	SiC Diode 20A/1200V
4	Trench IGBT 2ndG 25A/1200V	2nd G CoolMOS 38A/650V	SiC Diode 20A/1200V
5	SiC D-MOSFET 20A/1200V	2nd G CoolMOS 38A/650V	SiC Diode 20A/1200V

The absolute values of the European Efficiency along with gains in relation to the previously tested configuration are presented in the two pictures below.

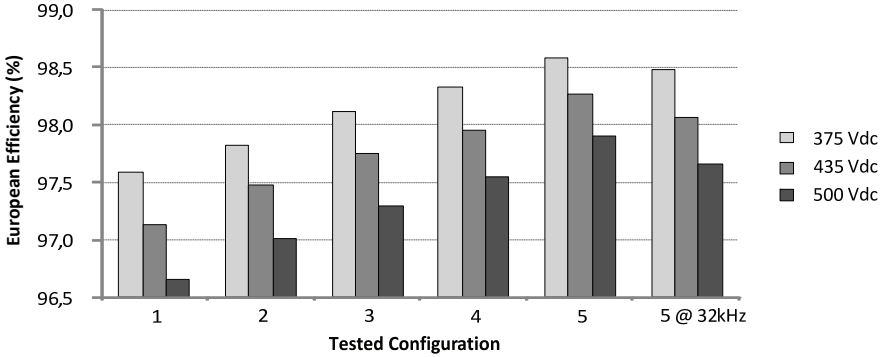


Fig. 123: Measured European efficiency values for the different configurations.

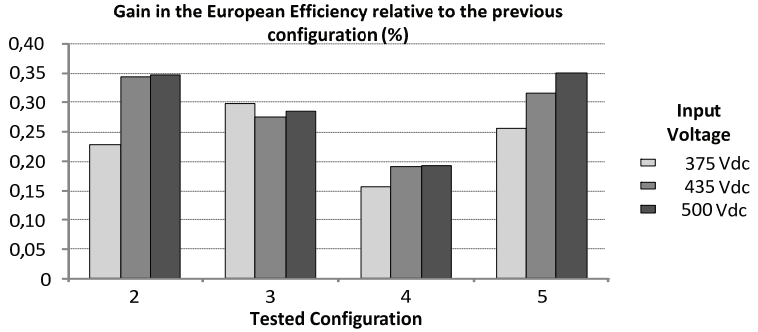


Fig. 124: Gain in the European Efficiency relative to the previous configuration for different input voltage levels.

The configuration **1** was taken as a reference measurement.

With the configuration **2** was evaluated the possible optimization of the switches T_3-T_4. For the rated current values, the lowest possible conduction losses were achieved with the CoolMOS, mainly due to the absence of the saturation voltage, as an increase of approximately 0,35% was obtained for the most significant voltage levels. A less expensive alternative would be employing low-frequency IGBTs that are optimized for low voltage drop or even thyristors. The lower increase of the efficiency for 365VDC can be justified by the lower ripple content on the current through the switch.

The adoption of SiC diodes in the **3**rd configuration provided a gain of approximately 0,275%, mainly justified by the absence of reverse recovery and consequently reduced switching losses. The lower increase for higher input voltages can be justified by the higher conduction losses of the SiC diodes in relation to the Si ones; what is especially critical in higher input voltages, when freewheeling is more frequent.

The implementation of a trench-field-stop IGBT of the 2nd generation having an improved dynamic behavior in comparison with the 1st generation resulted in an increase of approximately 0,19% in the configuration **4**.

The adoption of the SiC D-MOSFET in the configuration **5** allowed a further increase of approximately 0,32% over the already highly efficient 2nd generation Trench IGBT and 0,5% if compared with the 1st Trench generation. The higher gain for the most superior voltage levels is another interesting feature for the application of the device, mainly justified by the fast dynamic behavior. Still regarding the very low switching losses of the device, the potential of operating with the double of the switching frequency (32 kHz) and using only half of the

previous output filters was also investigated. From the presented values of efficiency, it becomes evident the potential of applying SiC devices at higher frequencies for reducing the size and cost of the output filter of an inverter and still maintaining a high level of efficiency.

To further illustrate the results, the obtained efficiency curves are presented below as a function of the input power.

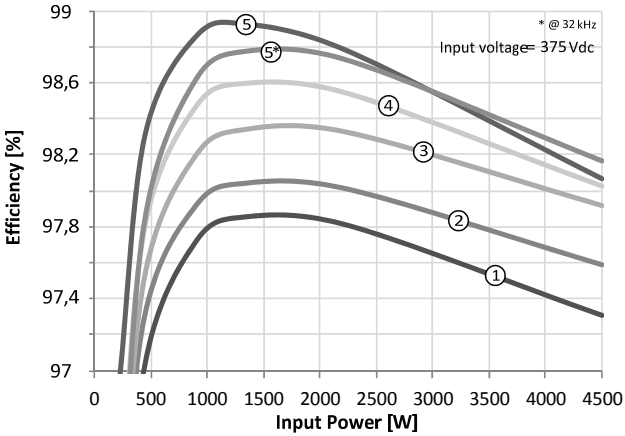


Fig. 125: Measured efficiency as a function of the input power for the tested configurations.

8.1.3. Conclusions

From the obtained results it is possible to assert that systems operating with the state-of-the-art Si switches along with freewheeling SiC diodes are already capable of achieving high levels of efficiency. For instance, in the market is possible to find commercial circuits having peak efficiency levels above 98,6%.

Taking such value as reference, it was still possible to improve the peak efficiency by more than 0.3%, while at nominal power the improvement was only around 0.15%. An increase of more than 1% on the efficiency is therefore not attainable within real application conditions. It also becomes evident here that the limited gain on efficiency alone cannot justify the higher cost of the SiC devices. Operation at higher switching frequency enabled for tested conditions reduction on the size of the output filter, without sacrificing the system performance.

8.2. Circuits suitable for normally-on SiC JFETs [55], [56]

The normally-on characteristic of depletion-mode JFETs has been so far considered as one of the main obstacles towards its wide application. As presented in item 2.2.2, several cascode configurations and driving circuits enabling safe operation in all circuits can be found in the literature. Most of these solutions nevertheless require additional components like a low voltage MOSFET with drawbacks like temperature limitation and increased parasitic inductance among others.

An interesting possibility would therefore be employing circuits especially suited for the stand-alone operation of normally-on devices. These circuits are characterized by the common property that the JFET current path can be interrupted by the control of other normally-off devices connected in series.

One first example would be the NPC inverter, where the internal switches normally operating at grid frequency can interrupt the current path in case both high frequency JFETs remain activated. Another example of inverter circuit is the so-called dual HF-Switch Voltage Source inverter as depicted below [63]. For operation at full active-power, S_1 and S_2 modulate the output waveform at high frequency, while S_3-S_4 are operated as an unfolding bridge. The high frequency devices could be implemented with JFETs, but this is not attractive due to the low voltage stress (each is clamped to half of the input voltage) enabling the use of highly efficient low-voltage Si MOSFETs.

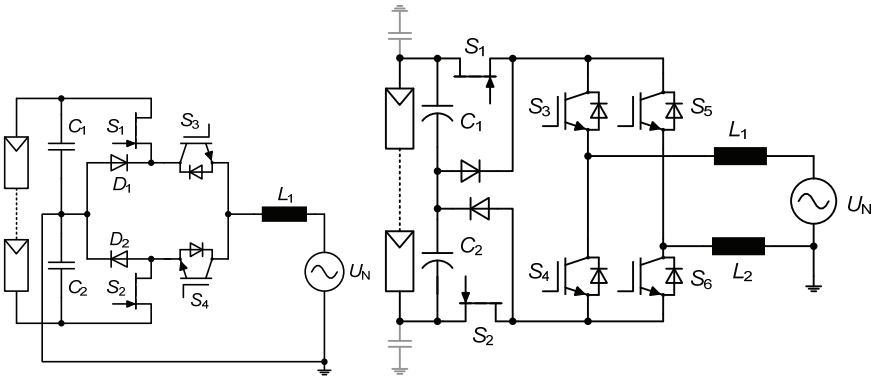


Fig. 126: Suitable circuits for stand-alone operation of normally-on JFET: NPC and dual-HF switch VSI.

Another possible circuit is the indirect current source inverter (I-CSI) being comprised of a step-down converter modulating a rectified sinus waveform, followed by an unfolding bridge [64]. A three phase variant relies on the current modulation performed by a bipolar step down, while the three phase bridge operating at grid frequency enabling the use of low-cost thyristors [65]. In both circuits, all high frequency switches can be implemented with stand-alone normally-on JFETs.

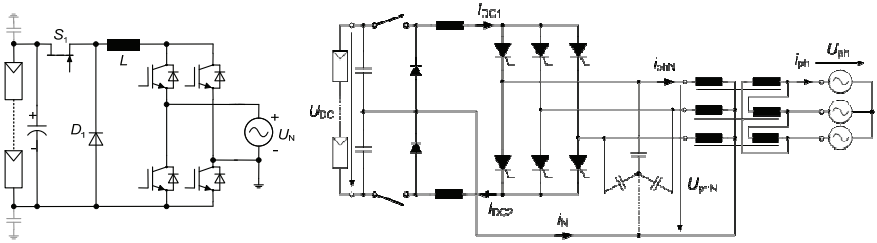


Fig. 127: Suitable circuits for stand-alone operation of normally-on JFET: I-CSI, Minnesota inverter.

All other topologies where the switch directly forms a closed circuit loop with the main DC-link, as is the case of classic full bridge circuits, are not suitable for the stand-alone application of the JFET. Problematic here is the stored energy in the DC-capacitance that will be in part burned in devices conducting the current, resulting in destruction. For single-phase inverters, the very high DC-link capacitance value to filter the 100 Hz ripple can store more than 20 J, while even the smaller capacitances in three phase inverters still have almost 10 J (due to the higher voltage levels). The fact that the power source is naturally limited on its maximum current (as is the case of a PV array) does not in the end avoids the referred problematic with the stored energy in the DC-link.

Having a large inductor in the referred current path may limit the current steepness but will still lead to destruction as any safety devices to interrupt the current flow are too slow (standard relays require more than 2ms for blocking) and would lead to high voltage peaks given the unavailable freewheeling path. An example in this case is a step-up converter.

8.2.1. Experimental results

A prototype rated at 1kW of the single-phase indirect current source inverter was built employing normally-on JFETs, as depicted below. Efficiency measurements with ohmic load indicated an efficiency of 98,6% at full load and a peak of 98,9%. From the experimental waveforms as presented on the right side of Fig. 128 it is

possible to observe the rectified sinusoidal inductor current (i_{L1}) and the output current after the unfolding bridge (i_N).

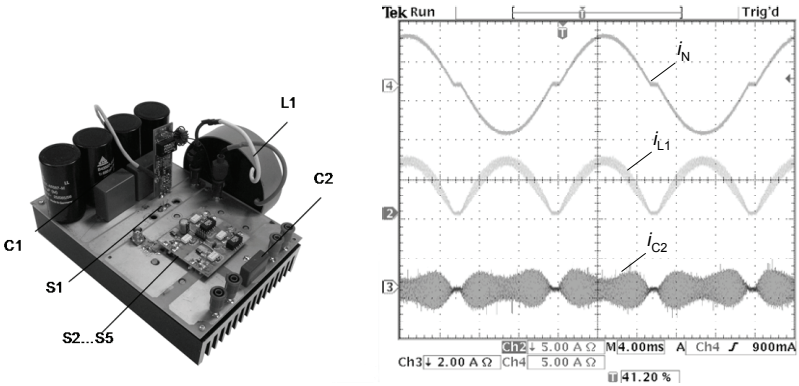


Fig. 128: Prototype photo and experimental waveforms.

8.2.2. Conclusions

Stand-alone operation of depletion mode JFETs is possible considering suitable topologies with other devices in series capable of interrupting fault currents. One common drawback of most of the presented circuits is the rather low voltage stress of the devices, normally resulting in a required voltage rating of about 600V. This in turn allows the use of highly efficient Si MOSFETs with Superjunction technology, reducing the attractiveness of using high voltage SiC devices.

8.3. Photovoltaic inverters for 1500V system voltage [54], [57]

One central role in the design of a PV system is played by the operational voltage levels, known as MPP range (maximum power point) and the maximum expected voltage when the array is not connected. This last value defines the so called system voltage which in turn is normally two times higher than the minimum operational level.

Considering the actual limit of 1000V, a boost converter rated at nominal power is required in all transformerless three-phase inverters. A reason for this is that for a maximum array open-circuit voltage under the above referred level, the normal operating range lies in part below the minimum DC-link voltage required to feed the grid, as presented in the table below. In the case of converters operating with

step-up transformer in the output (connected to the medium-voltage grid), despite the possible absence of the step-up converter, the input voltage is normally limited within the range of 450…820V in order to enable using 1200V devices.

Table 12 –Operational MPP ranges directly related to max. array voltage

Type	Required DC-link voltage	Min. MPP voltage	Max. MPP voltage	Max. Array voltage
1-phase	350	350	525	700
Boost + 3-phase 1000V	650	500	750	1000
3-phase 1500V	650	750	1125	1500

8.3.1. Optimal input voltage range

Increasing the system voltage from 1000V to 1500V would thus allow the elimination of the boost stage in the case of transformerless inverters, resulting in substantial savings regarding power devices and passive components. Discussions about increasing the maximum system voltage have in fact been under way for some time [58], as it was pointed out that a level of 1500VDC is already covered by some standards like the VDE0100-100 and the IEC61730-1 (applied to requirement construction of PV-modules). On the other hand, the standards concerning respectively connectors in PV-applications (VDE0126-5) and safety tests requirements for modules (IEC61730-2) are limited to 1000V. A harmonization of the limits from these standards is thus necessary in order to allow voltages up to 1500V.

Selecting very high voltage levels can nevertheless bring some drawbacks, what is especially valid for circuits directly connected to the grid. In this case, higher voltages result in a higher conversion effort (higher difference between input and output voltage), directly implying in larger magnetic elements and higher losses. It is therefore advisable to select and input range that is just high enough to enable eliminating the step-up stage. In the case of the proposed single stage transformerless approach, the input voltage shall always be superior to the double of the peak grid voltage (plus 10% variation according DIN IEC 60038 and with 5% control reserve). Under assumption of third-harmonic modulation for lower voltage values, a minimum input voltage of approximately 650V under worst-case conditions is necessary. Considering the data regarding the operational MPP

voltage range valid in central Europe, a maximum MPP voltage of 910V and an open circuit voltage of at least 1300V are required for directly feeding into the 230V grid without the step-up converter. It becomes clear at this point that it not necessary to go up to 1500V with the system voltage as this will only imply in higher losses and costs.

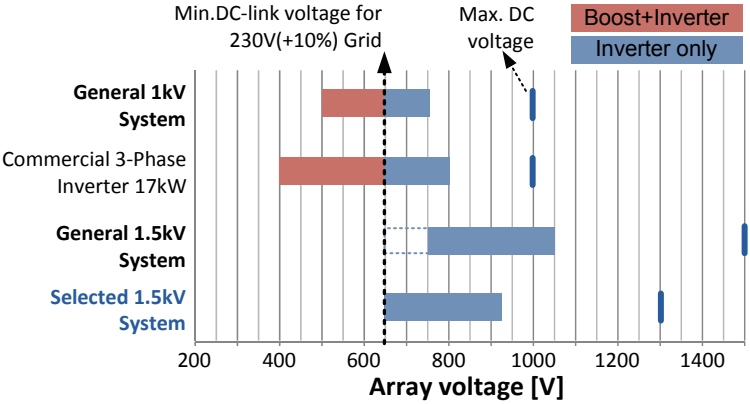


Fig. 129: Overview of input voltage ranges for different configurations.

An important issue at system level is that now a larger amount of modules need to be connected in series in order to attain the required voltage levels. In Fig. 130 is depicted the relation between the number of series connected modules in order to attain the minimum voltage of 625V and the resultant string power. Given the vast variance of module characteristics, a broad spectrum of possible configurations can be observed, though two major groups can be identified at power levels around 3,5 and 5,5kW with respectively 25 and 35 modules per string. As a remark, considering the higher amount of modules tracked now by a single MPP system, mismatch losses may be more relevant in such configurations.

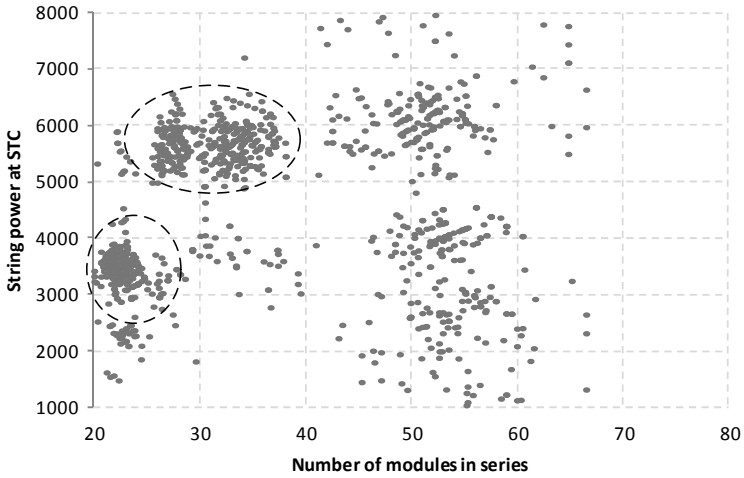


Fig. 130: Amount of modules in series and string power in Watts at STC (standard test conditions, 25°C, 1000W/m²) for a U_{MPP_MIN} of 650V.

8.3.2. Topology selection

Among the topologies suitable for such high voltage levels, then NPC circuit as depicted below could be a first alternative. By means of series connection of devices it is possible to still use 1200V-rated devices. Drawbacks of such solution are the series connection of the devices on the main current path, resulting in higher conduction losses and consequently larger chip area. Besides, the internal switches T_2 and T_3 are not clamped to the DC-link voltage, additional freewheeling diodes are required and finally three high side gate drivers are required per phase. In face of such drawbacks, the BS-NPC (bipolar switch neutral point clamped) topology was chosen for construction of the prototype. Highlights here are that only a single device in main current path and lower commutation voltage (half of total DC-link). Among the possible bipolar switch configurations, the common emitter is the most advantageous given same driving potential. The voltage stress over T_1/T_4 and T_2/T_3 (and freewheeling diodes) is respectively equal to the total and half value of the DC-link voltage. Thus the selected voltage ratings are 1700 and 1200V for a maximum DC-link voltage below 1500V. Under such prospect, the use of innovative SiC devices rated at 1700V is an attractive solution in order to avoid the costly and lossy series connection of switches.

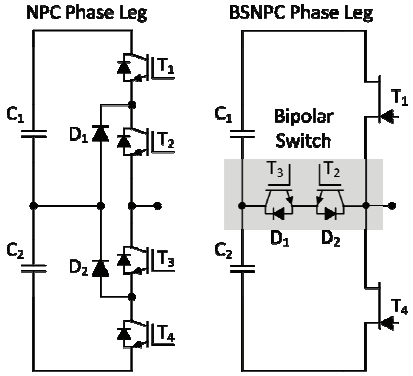


Fig. 131: Phase-legs of NPC and BS-NPC inverters

8.3.3. Experimental results

Three prototypes were constructed making use of 1700V-rated devices from the manufacturers CREE and Infineon. Switching frequency was selected at 48kHz with an input voltage range of 650-910V.

Below are depicted the circuits with Infineon 1700V-JFETs, as a single-phase (rated at 1,8kW) and in the three-phase version with integrated driving board, followed by the experimental measurements in the Fig. 133. The measured efficiency led to peak values over 98,5% with an European Efficiency of 98,6%, well above similar circuits found in the market operating at much lower switching frequency. From the calculated loss distribution, it is possible observe that the conduction losses remain the dominant factor on the converter efficiency, despite the high switching frequency. The inductor losses on the other hand indicate that further size reduction could be attained without significantly sacrificing the overall efficiency.

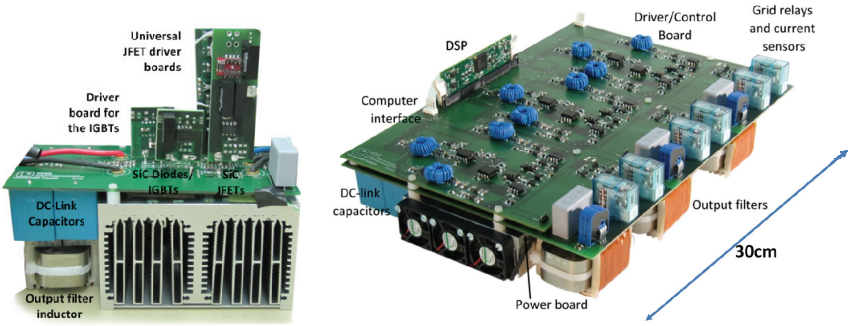


Fig. 132: Single-phase and three-phase prototypes with Infineon 1700V-JFETs.

In Fig. 134 is depicted the single-phase prototype with the 1700V-rated CREE MOSFETs, rated at 5.7kW. On the right side is depicted the constructed inductor for operation at 48 kHz in comparison with another one designed for 16 kHz. Both are rated for the same maximum current and maximum ripple limit (10% of peak value under worst case conditions). As was discussed in the item 4.2, such significant size reduction with low amount of losses was mainly attainable by using a different core material, namely Finemet. This in turn enabled obtaining an optimal level of core losses without sacrificing the possibility of operating with high flux density (what would happen in case of employing ferrite).

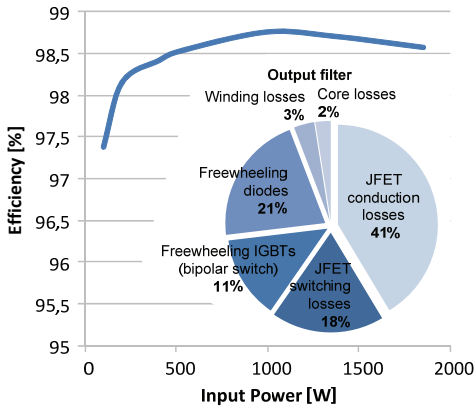


Fig. 133: Measured efficiency of the single-phase power stage at 750V input voltage and 230V output voltage with ohmic load; and calculated loss distribution at nominal power and cosφ=1.

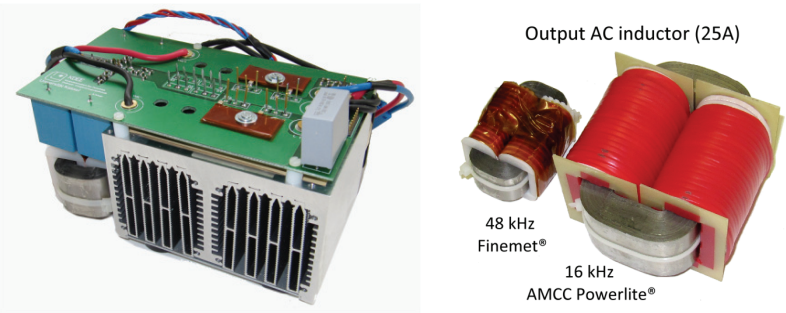


Fig. 134: Prototypes with CREE 1700V-MOSFETs and comparison of output filter size reduction by means of increased switching frequency

In upper part of Fig. 135 are presented the waveforms for operation at approximately 2,5kW output power with 700V input voltage. From the drain-source voltage across the high frequency switch T_1, it is possible to observe that the commutation takes place with half of the DC-link voltage, as already explained. The measured efficiency of the power stage is presented on the lower part of the same figure and led to peak values over 98,8%.

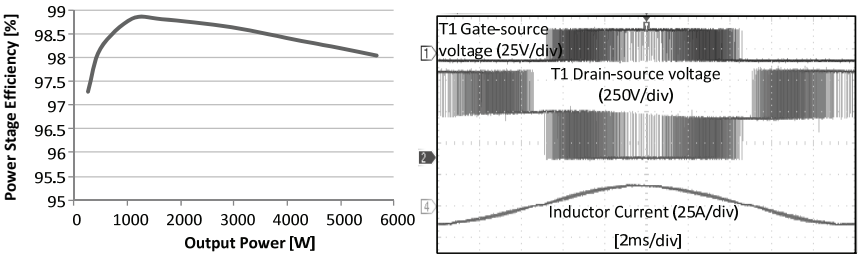


Fig. 135: Measured waveforms at 2,5kW output power and efficiency of power stage with 700V input voltage.

8.3.4. Conclusions

Increasing the system voltage in high power PV systems proves to be one of the most promising developments towards cost reduction, either due to the elimination of the step-up stage or simply because of lower expenditure with DC-cabling.

Such systems requiring 1700V-rated devices are on the other hand by far the most attractive field for SiC devices, which strongly outperform their Si counterparts not only regarding specific chip area resistance but also dynamic performance. From the obtained experimental results it was possible to demonstrate that it is possible

to simultaneously attain a high level of efficiency with simultaneous compact passive elements, opening interesting prospects regarding additional costs savings.

8.4. Highly compact step-up converter using SiC-BJTs [290]

From the presented investigations it was possible to assert that the BJT represents one of the most attractive SiC switch structures given the low specific resistance, fast switching and low temperature dependence. The device capabilities were investigated in a step-up converter for photovoltaic systems operating at high switching frequency and rated at 17kW. Main design issues of this investigation were obtaining low driving losses along with a compact input filter.

8.4.1. Driving circuit: alternative configuration for lower losses

The driver circuit fulfills two basic functions, namely providing fast charge/discharge of device capacitances enabling fast switching behavior and ensuring a continuous supply of base current avoiding increased forward losses and saturation.

Regarding the dynamic operation, an optimal strategy is relying on higher voltage levels to ensure faster transients. This is in fact only possible when using the BJT, as there is no driving voltage limitation like in the case of the MOSFETs. Furthermore in contrast with most normally-off SiC devices, the BJT does not require a negative driving voltage to increase noise immunity because the threshold voltage lies well above 2V, with the device being activated only with a continuous supply of base current.

For the static operation, it is in turn necessary to carefully select a suitable value of base current, considering a trade-off between conduction and driving losses. Despite the higher gain values (and thus lower base currents), driving losses can still be critical in the case of SiC BJT due to the higher forward voltage drop between base and emitter (due to the wider band-gap). Meanwhile as was observed in the forward performance characterization of the BJT, doubling the base current (from 0,5 to 1 A) results in a reduction of only 10 % in the equivalent resistance. The importance of the base current resides therefore not solely on reducing the conduction losses, but more importantly on shifting the saturation to higher levels. Such aspect is especially important when considering operation with higher levels of current ripple, as is the case of the step-up converter under investigation.

A base current of at least 1 A was therefore selected in order to enable a switching capability up to 40 A. With such value it is possible to calculate the static driving losses as a function of the selected driving voltage and value of input voltage (what indirectly implies the duty cycle value). From the graph below one can assert that high levels of driving voltage necessary to enable high switching speeds can also lead to almost 7 W losses, mainly concentrated on the base resistor. In order to deal with such limitation, an approach with separated voltage sources for dynamic and static operation was employed here [291]. The basic schematic is presented in the Fig. 136 and relies on "chopping" the control signal of the high voltage driver, so that it is enabled only during a brief interval of time during the switching transient. The static driving stage remains on the other hand activated during the whole turn-on time and is fed by a lower voltage, thus reducing the static losses.

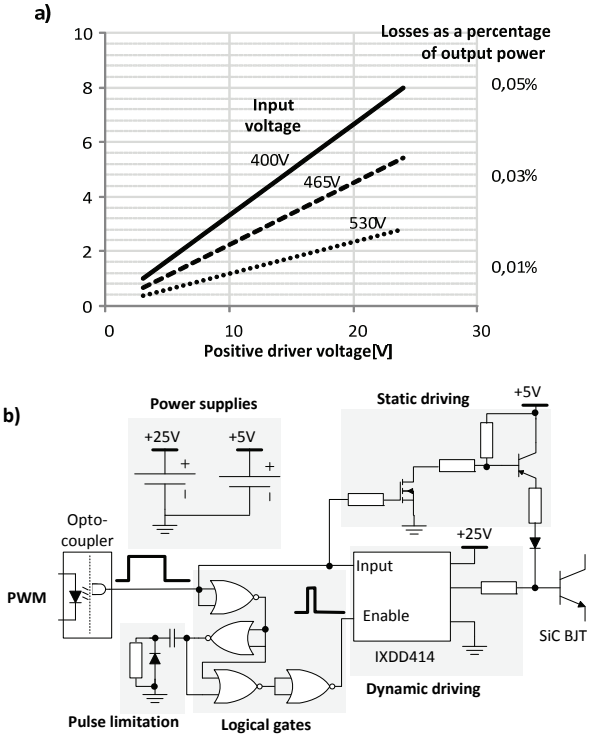


Fig. 136: a) Driving losses for different supply voltages, b) employed two-stage driving solution.

8.4.2. Input filter inductor: maximum size reduction with new materials

Here were investigated the capabilities of newly available cut-cores made with the thin-laminated nanocrystalline material Vitroperm 500F. On the top of very low level of losses and good high frequency operation, such material can also operate with high values of saturation flux, leading to a reduction on the core cross-section in comparison with ferrites. In order to enable a broader overview of such potentials, the inductor size factor as already presented in Fig. 76 is now calculated considering a much higher current ripple (40%) valid for the current application, being presented in the picture below.

From such results it is possible to draw some conclusions. Firstly, the size factors attainable with high flux materials like Vitroperm 500F can be reached with low-cost ferrites only when the frequency is significantly increased, thus resulting in higher switching losses and thus higher chip are expenditure. Going in the direction of very high values of switching frequency with SiC devices (near 1MHz) would on the other hand be attractive only in conjunction with core materials having very low specific losses like NiZn-based ferrites and in case of dramatically higher values of switching speed. In order to illustrate the attained size reduction, a comparison between the core size employed on the construction of the inductor and an equivalent possible solution based on ferrite is also presented below.

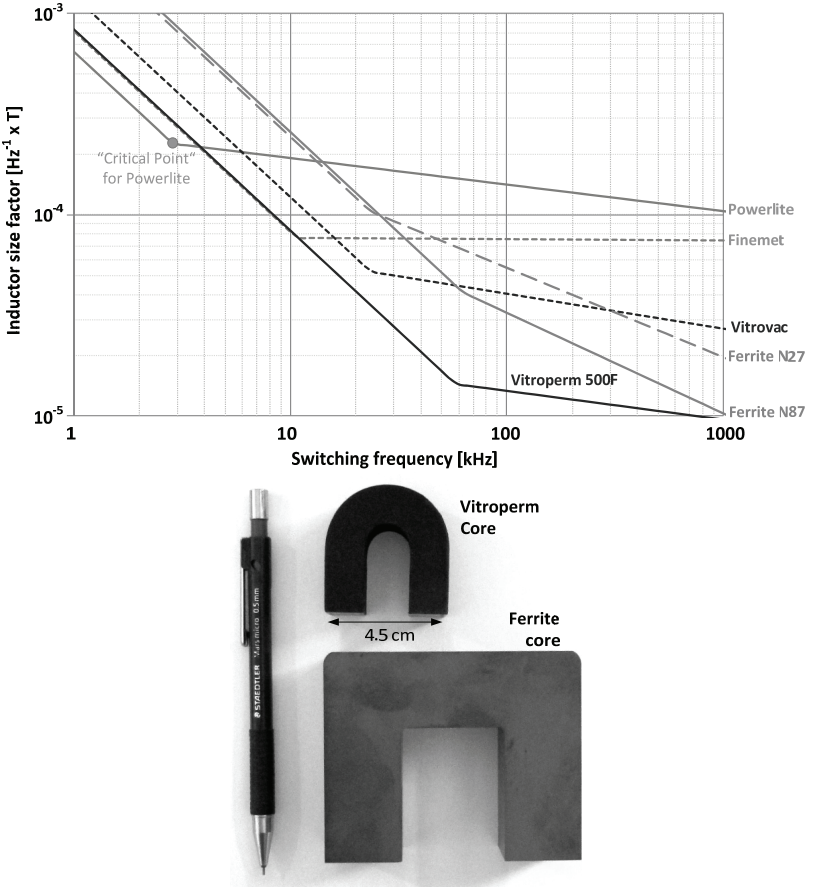


Fig. 137: Inductor size factor for different core materials as a function of frequency with size comparison between employed Vitroperm core and possible counterpart based on ferrite.

8.4.3. Experimental results

The efficiency of the power stage (also considering driving losses) is presented in the picture below for two levels of input voltage. From the application requirements, the maximum input current is limited to 32A, thus resulting at lower maximum power at 400V. A distribution of the losses according to the calculations

is presented near the curves, with a photo of the prototype on the right side of the picture.

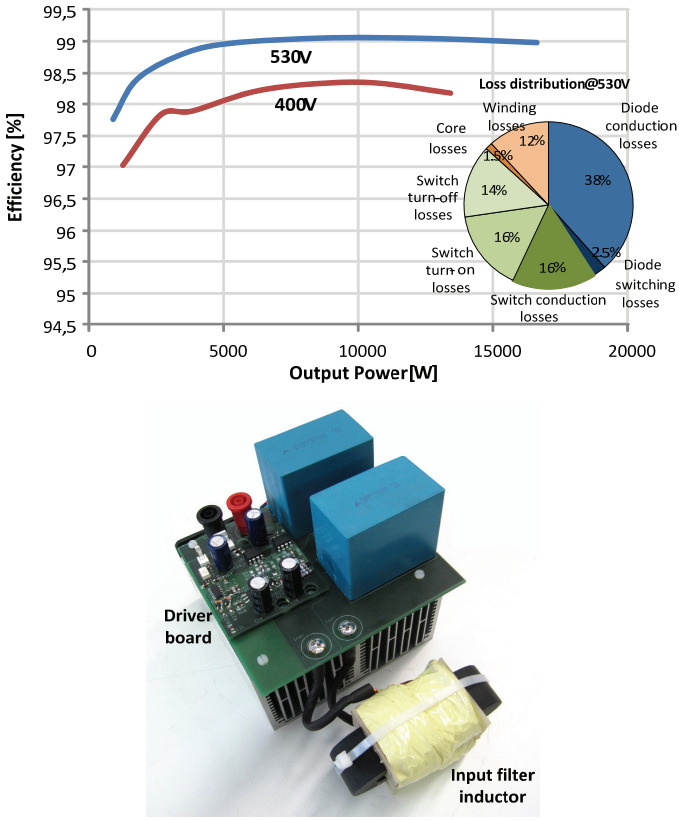


Fig. 138: Efficiency measurements and calculated loss distribution at 530V, photo of the prototype.

From the obtained results it is possible to draw some conclusions. Firstly, operation with high current loading with the BJT is possible, without reaching critical temperatures or saturation. In addition to this, the two-stage driving solution enabled a significant reduction of the driving losses, which according to the calculations corresponded to about 0,02% of the input power. From the loss calculation one can observe that the freewheeling Schottky diodes are operating under significant stress, especially in the case of higher input voltage. A more efficient solution could thus be obtained by substituting these diodes with a switch

operating in synchronous rectifying operation. Such operation is nevertheless, as previously referred, not possible with the BJT device.

One critical drawback of the presented driver is that turn-off takes place with only a low voltage (from +5 to 0V), consequently resulting in slower switching transient, as can be observed by the very low value of dv/dt (4V/ns) depicted below. A solution for this problem could thus be either changing the logic of the gate signals or including a negative voltage driving potential. Thermal measurements of the inductor indicated that the windings reached temperatures in excess of 50°C, with the core middle-section being the one with the highest temperature level.

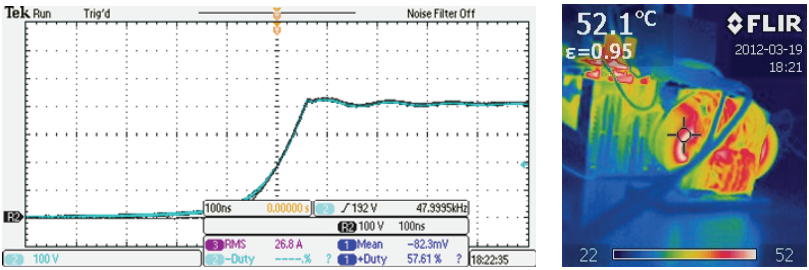


Fig. 139: dv/dt of turn-off transient [100V/div, 100ns/div] along with thermal imaging of output filter at nominal power.

8.4.4. Conclusions

From the results it was possible to verify that the BJT enabled attaining high levels of efficiency while operating with high current loading and high frequency. The common limitation attributed to the BJT, namely higher driving losses, was addressed by using a two-staged solution. Drawbacks of such approach are the increased complexity and higher turn-off losses. An alternative circuit with negative driving voltage needs therefore to be further investigated.

8.5. Switching speed and conducted interference [66]

In this investigation, operation at different switching speeds was evaluated in respect of possible gains in the efficiency and the related effect on the conducted interference emissions.

For such purpose, tests with a SiC-MOSFET and a 2nd generation Trench IGBT were initially performed in a switching cell. By changing the value of the gate

resistance, the charge/discharge current of the device capacitances can be modified and consequently the device switching speed. This holds true for the SiC-MOSFET but in the case of the IGBT, it is valid only for the turn-on transient, which is controlled by the intrinsic MOSFET that activates the BJT-array. At turn-off, the transient of the IGBT is dominated by the removal of the minority carriers from the drift layer of the bipolar array and is mainly affected by the device structure, doping profile and external electrical field (which is proportional to the blocking voltage).

8.5.1. Experimental investigation

The resultant slopes of voltage and current (dv/dt and di/dt) along with the switching energy obtained on the measurements with different resistors is presented below for the two investigated technologies. As expected, the turn-on speed of both IGBT and SiC-MOSFET can be finely regulated with the gate resistor. For turn-off the same is valid only for the MOSFET, as the IGBT operates at much lower speed levels and consequently with higher levels of losses.

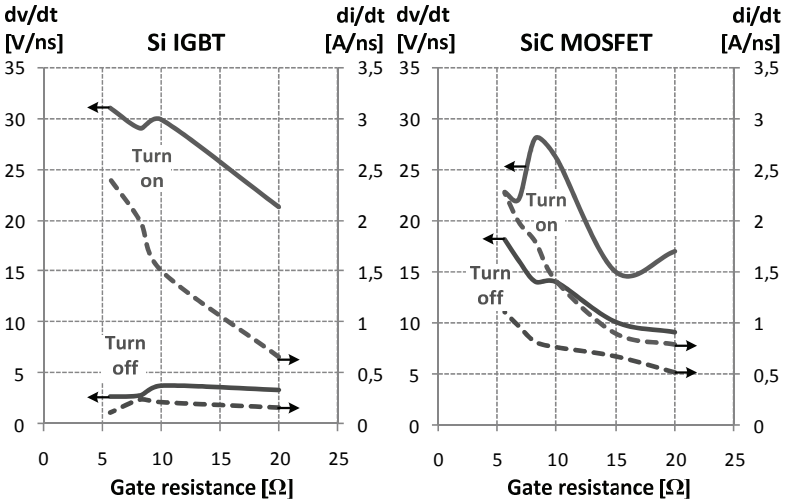


Fig. 140: Measured switching slopes for different values of gate resistor.

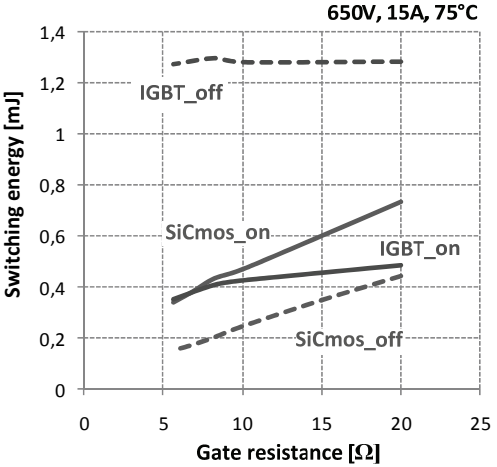


Fig. 141: Measured losses for different values of gate resistor.

Further measurements were then taken in a step-up converter rated at 4 kW operating at 16 kHz, with input and output voltages respectively of 400V and 650V. The measured efficiency of the power stage for both semiconductor configurations, along with higher speed operation of the SiC-MOSFET is presented below. From the measured losses, it is possible to observe that the semiconductor losses area reduced by 40% with the application of the SiC-MOSFET, while further reduction of 10% is attained by means of doubling the di/dt value.

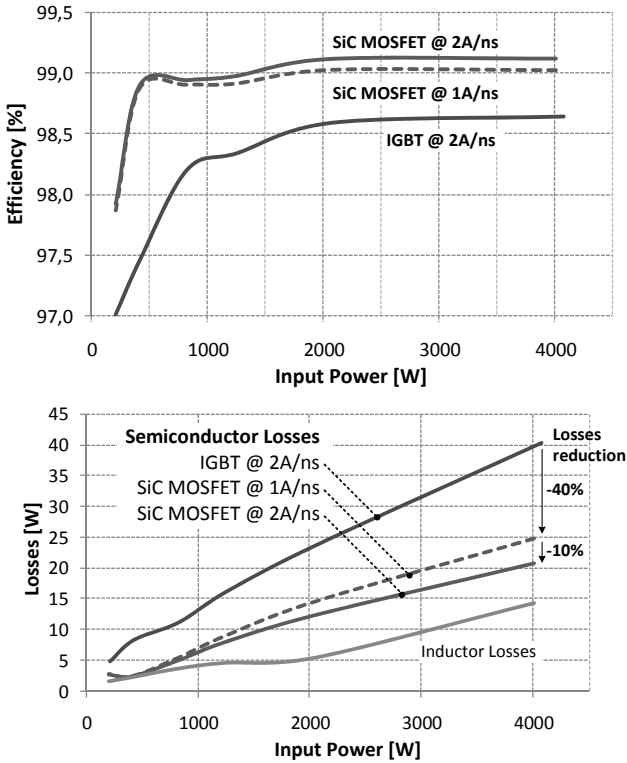


Fig. 142: Measured efficiency of the power stage and experimental loss distribution

In order to investigate the conducted EM emission from the boost converter related to different values of switching speed, a test setup was built consisting of a Line Impedance Stabilization Network (LISN) with a standardized impedance and EMC analyzer measuring the conducted EMI in the frequency range from 150 kHz to 30 MHz. No external filters were attached to converter in order to obtain a clear indication about the effect of high slopes in the switching transients. A comparison of the conducted EMI for operation of the step-up converter at nominal power with SiC-MOSFET at two different di/dt values, namely 1 and 2A/ns with the already referred gate resistances was performed. In the next two figures are demonstrated the conducted EMI spectra with the quasi-peak and average detector for both configurations.

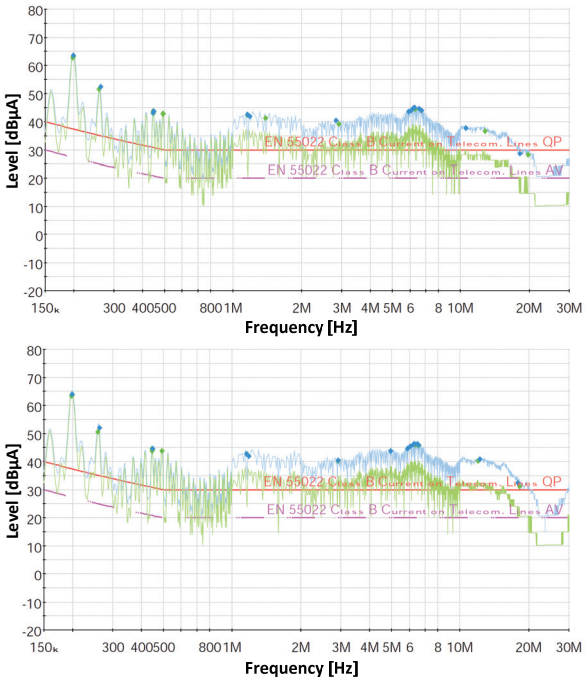


Fig. 143: Spectrum for SiC-MOSFET operating at 1A/ns and 2A/ms, measured from 150kHz to 30MHz

For the analyzed frequency range, small increases were observed starting from 1MHz, while the most significant changes occurred between 8 and 20MHz, with an average increase of 3dB. Such effect on the higher frequency range can be mainly explained by high frequency oscillations observed in the measurements and also the values of rise/fall time of the curves [67].

8.5.2. Conclusions

The obtained results here are in good accordance with the analysis performed in the item 4.1. From the rather conservative increase of speed investigated, it is possible to observe that most significant effect on the EMI was on at the upper frequency spectrum above 8 MHz. Because of the high frequency component of the switching transients, it is expected that the highest impact of higher switching speed is located on the radiated components.

9 Conclusions

9.1. Device level

Regarding the performed measurements with the SiC devices, it is possible to assert that most of the investigated devices present a very similar dynamic behavior regarding attainable switching losses. A reason for this was the established limits for the values of di/dt and dv/dt. Higher speeds and consequently lower amount of losses are attainable for all devices, but nevertheless not suitable under the assumption of employing discrete devices mounted in TO-cases, given the very high level of parasitic inductance. From the side of the manufacturers it is therefore necessary to go in the direction of more compact and low-inductive cases like is approaches from IRF and EPC for low-voltage GaN devices. An enhanced module integration of the commutation circuit can also be another possibility.

One distinctive factor regarding the overall performance of the devices was the temperature dependence of the chip resistance, especially considering high junction temperature levels to maximize the chip utilization. Under such conditions, the CREE SiC MOSFET present one of the lowest values of temperature dependence, followed by the Transic SiC-BJT. Meanwhile switching losses were practically temperature independent.

In order to benchmark the performance-expenditure ratio of the investigated technologies, a new figure of merit was proposed, based on real application conditions. The best values were attained by the JFETs, followed by the MOSFET and BJT.

The availability of very diverse switch technologies as was here presented offers from one side a broad spectrum of possible optimizations for the manufactures. On the other hand, such strong variance ends up limiting the possible expansion of the SiC market, as industrial consumers are rather insecure when simultaneously dealing with single suppliers and a still maturing technology without second-source. To make matters worse, very diverse driving requirements make the transition between technologies practically impossible without an extensive re-design of the board circuit.

9.2. Application level

Considering now the issues related to the application of WBG devices on power converter in renewable energy systems, it is possible to draw the following conclusions.

- High switching frequency and reduction of magnetic elements

The possibility of operation at high switching frequency is mainly attained by means of the very fast switching transients. Under rather conservative speed values, reduction of more than 75% against state-of-the-art IGBTs with similar ratings could already be attained.

Further investigations indicated that such levels can be reduced by 50% when higher speed levels are employed. Despite the fact that an acceptable amount of oscillations and overvoltage was observed on the tested devices, other issues stand in the path towards their practical implementation. The driver circuit is the first bottleneck, as most products currently available in the market are not rated to deal with such extreme speed values. Stress on the isolation of wound elements, including filter inductors to generators is another critical issue to be dealt in order to avoid problems with the system long-term reliability. At least but not last, higher speeds have a strong impact on the EMI levels, especially at frequencies above 5 MHz in both conducted and radiated spectrums.

The final device property related to high switching frequencies to be investigated was the transient increase of the conduction losses know as modulation effect. Experimental results demonstrated that such problematic can be clearly observed in all tested Si IGBTs, while being absent in all SiC devices. As a consequence, an increase of up to 10% in the conduction losses normally observed when employing IGBTs at high switching frequencies can be fully avoided with the adoption of SiC devices.

From the performed analysis it was possible to conclude that the possible size reduction of magnetic components due to higher switching frequencies is strongly affected by the currently employed material, besides specific operating conditions. In case of operation near the specific core losses limit, any further increase of the frequency results in only a minor size reduction. It is therefore necessary to employ other material grades with lower losses and similar capabilities regarding either the saturation flux density (for filter inductors) or permeability (high frequency transformers). An overview of such materials was presented in this work.

Given the fact that the turn-off energy is normally lower than the one at turn-on for SiC devices, operation at higher ripple values simultaneously offers the attractive possibly of reducing the semiconductor losses and enabling size reduction of

magnetics. Under some operating conditions, the savings with magnetics may be even higher than ones obtained with higher switching frequency. Very high ripple values are nevertheless not attractive, as they lead to increasing peak current values and consequently end up cancelling the effect of the smaller required inductance value. In addition to this it is necessary to note that the higher amplitude of the AC component has a strong impact on the winding losses.

- Cooling expenditure

The reduction of the cooling expenditure can in part be attained by making use of the capability of operation at very high values of junction temperature. Problematic here is the significant impact of the increasing device resistance, as was identified that full device loading before thermal runaway is normally attained at levels below 250°C for operation at 100 kHz. For lower switching frequencies, the temperature limits drop to levels below 180°C. Higher junction temperature values are still possible but require de-rating and are in face of the application requirements and device costs not attractive.

In addition to this, the reliable implementation of levels beyond 200°C is especially challenging at higher power levels. As a first conclusion it is possible to say that reducing the cooling expenditure by means of higher junction temperature is in the end a rather limited possibility concerning the current field of application.

A more attractive alternative is the reduction of the losses, which naturally comes as a result of the smaller chip resistance. In this case, even small increases on the efficiency can already result in significant savings not only with the expenditure with heatsinks but also on the power consumption of the cooling system.

- Chip area expenditure

Focus was given here to possible reduction of the chip area given the lower specific chip resistance and switching energy. Such aspect is of major interest not only to deal with the high specific costs of WBG materials but also to enable reduction on the semiconductor losses, under the assumption of similar levels of specific losses.

From the proposed analytical equations it was also possible to identify not only possible gains regarding operation at higher specific loss levels but also the necessary increase on chip area in case of operation at higher switching frequency.

- Analysis on potential savings

From the previous presented aspects at system level, it becomes clear that SiC devices enable higher levels of power density. Of interest for the applications in focus is not compactness alone but rather the reduction of the specific costs (€/W),

which can be attained either by reduction of converter size (smaller heatsink and magnetics) or with an increase of the power rating.

In this work was proposed a simplified cost savings analysis considering photovoltaic power conversion systems and back-to-back converters for wind power systems. One important remark regarding the presented results is that they can be strongly influenced by individual cost distribution factors and other individual operating conditions. The objective here was in this case not to present precise cost savings indicators, but rather to propose a methodology enabling the identification of tendencies and aspects to be considered when evaluating the application of WBG devices in renewable power systems. Some of the most important points are summarized below.

- The higher specific costs of WBG devices (cost/chip area) are in general the dominant in the analysis, surpassing in most cases any gains obtained with smaller passive elements and less cooling.
- Operation at higher switching frequencies requires more chip expenditure and brings gains only at rather smaller increases.
- Operation at higher loss density may be an option to simultaneously reduce the expenditure with cooling (not considered in the analysis) and chip area. Critical here is if the higher loss density is obtained either by better heat spreading or with operation at higher temperature. For the last case (not considered here), the over proportional increase of the chip resistance with increasing temperature for some technologies strongly limits any gains.
- Higher switching speed turns out to be an interesting alternative to enable further savings with chip area, especially if higher switching frequencies are targeted.

Other aspects at system level like increasing the system voltage in photovoltaic systems may enable in turn additional savings regarding installation and cabling. Wind power systems may also profit from the higher overload capability of WBG devices, enabling savings when selecting a suitable chip area.

- Experimental results

In the last and final chapter of this work was presented a brief overview of results obtained with power converters operating with SiC devices. One first conclusion here is that high levels of efficiency can already be achieved in systems employing Si switches and SiC diodes. Further increases with SiC devices under same operating conditions are therefore rather marginal. Meanwhile it was demonstrated that the operation at higher switching frequency levels with significant decrease on

the size of magnetic elements is still possible at high levels of efficiency, not only with 1200 but also with 1700V-rated devices.

Finally, it was also possible to identify some topologies suitable for the application of normally-on devices in stand-alone operation (without cascode) but with the common drawback of low levels of voltage stress.

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Abbreviations and symbols

2DEG	. . . . .	2-dimensional electron gas
α	. . . . .	frequency exponent of Steinmetz equation
A_{chip}	. . . . .	Chip area
A_{chip_device}	. . . . .	Device chip area
$A_{chip\_reduction}$	. . . . .	Relative chip area reduction
$A_{chip\_reference}$	. . . . .	Total chip area value used as reference
A_{chip_Si}	. . . . .	Required chip area using silicon power devices
A_{chip_SiC}	. . . . .	Required chip area using silicon carbide power devices
AlGaN	. . . . .	Alluminium Gallium Nitride
AlN	. . . . .	Alluminium nitride
Aopt	. . . . .	Optimal chip area
β	. . . . .	flux swing exponent of Steinmetz equation
$\beta_{current}$	. . . . .	Current gain of BJT
BFoM	. . . . .	Baliga figure of merit
BJT	. . . . .	Bipolar junction transistor
B_{max}	. . . . .	peak value of magnetic flux
$BV_{\_CBO}$	. . . . .	Collector-base breadkown voltage
$BV_{\_CEO}$	. . . . .	Open-base breakdown voltage
C_{GD}	. . . . .	Gate-drain capacitance
C_{GS}	. . . . .	Gate-source capacitance
C_{iss}	. . . . .	Input capacitance

C_{oss}	. . . . .	Output capacitance
$Cost_{ratio}$	. . . . .	Ratio between semiconductor material specific costs
C_{rss}	. . . . .	Reverse capacitance
DHEMT	. . . . .	Double heterojunction high electron mobility transistor
DIBL	. . . . .	Drain induced barrier lowering
D	. . . . .	Duty cycle
ε_0	. . . . .	Permittivity of vacuum
E_{crit}	. . . . .	Critical electrical field
ε_r	. . . . .	Relative permittivity
ESBT	. . . . .	Emitter-switched bipolar transistor
E_{sw_scale}	. . . . .	Switching energy of chips association
E_{sw_Si}	. . . . .	Switching energy from silicon power device
E_{sw_SiC}	. . . . .	Switching energy from silicon carbide power device
E_{sw_single}	. . . . .	Switching energy of single chip
FBL	. . . . .	Floating N-type buried layer BJT
FOM	. . . . .	Figure of merit
f_{sw}	. . . . .	switching frequency
f_{sw_max}	. . . . .	Maximum attainable switching frequency
f_{sw_ratio}	. . . . .	Ratio between switching frequencies using SiC and Si devices
f_{sw_Si}	. . . . .	Switching frequency using silicon power devices
f_{sw_SiC}	. . . . .	Switching frequency using silicon carbide power devices
GaN	. . . . .	Gallium Nitride

g_{FS}	. . . . .	Device transconductance
GIT	. . . . .	Gate injection transistor
GTO	. . . . .	Gate turn-off thyristor
HEMT	. . . . .	High Electron Mobility Transistor
HFET	. . . . .	Heterostructure field effect transistor
I_{avg}	. . . . .	Average current value across inductor
I_{base}	. . . . .	Steady state base current
I_{base_peak}	. . . . .	Base peak current
I_D	. . . . .	Drain current or commutation current
I_G	. . . . .	Gate current
i_{gate}	. . . . .	Average value of gate current
IGBT	. . . . .	Insulated gate bipolar transitor
I_{nom}	. . . . .	Nominal current loading capability
$I_{nominal}$	. . . . .	Nominal chip current
I_{out_Si}	. . . . .	Converter output current using silicon devices
I_{out_SiC}	. . . . .	Converter output current using silicon carbide devices
IPM	. . . . .	Intelligent power module
I_{ratio}	. . . . .	Ratio between new and original converter current rating
I_{rms}	. . . . .	Effective value of current loading across device
I_{sw}	. . . . .	Value of commutation current
JFET	. . . . .	Junction gate field-effect transistor
k	. . . . .	Factor representing division between conduction and switching losses
K_{enc}	. . . . .	Percental expenditure with enclosure

K_{mag}	. . . . .	Percental expenditure with magnetics
K_N	. . . . .	Fourier coeficient for n-th order component
$k_{Psw\_material}$	. . . . .	Ratio of switching losses from total specific chip losses
k_{Psw_Si}	. . . . .	Ratio of switching losses from total specific chip losses using silicon power devices
k_{Psw_Si}	. . . . .	Distribution between switching and conduction losses of system using Si devices
K_{rest}	. . . . .	Percental expenditure with other components
K_{sem}	. . . . .	Percental expenditure with semiconductors
λ	. . . . .	Thermal conductivity
L_{BOOST}	. . . . .	step-up converter filter inductance
L_{BUCK}	. . . . .	step-down converter filter inductance
M	. . . . .	voltage gain
MISFET	. . . . .	Metal insulatior semiconductor field effect transistor
μ_n	. . . . .	Electron mobility
MOS	. . . . .	Metal oxide semiconductor
MOSFET	. . . . .	Metal oxide semiconductor field-effect transistor
MPS	. . . . .	Merged PIN Schottky diode
n_{chips}	. . . . .	Number of chips in parallel
N_d	. . . . .	Doping concentration
n_i	. . . . .	Intrinsic carrier concentration
ν_{sat}	. . . . .	Electron saturated drift velocity
n_{SiC}	. . . . .	Proportion of expenditure with semiconductors affected by adoption of SiC

		devices
P_{cond}	. . . . .	Conduction losses
P_{cond_ratio}	. . . . .	Conduction losses ratio between investigated technologies
P_{driver}	. . . . .	power rating of driver
PIC	. . . . .	Power integrated circuits
P_{loss}	. . . . .	Total device losses
P_{loss_ratio}	. . . . .	Proportion of the overall losses being affected by the semiconductors
$P_{loss\_SiC/Si}$	. . . . .	Ratio between overall semiconductor losses using SiC and Si devices
P_{max}	. . . . .	Maximun specific power dissipation for given device
P_{norm}	. . . . .	New power converter cost normalized to original value
P_{sec_Psw}	. . . . .	Chip specific losses reserved to switching losses
P_{spec}	. . . . .	Maximum chip specific power dissipation
$P_{spec\_material}$	. . . . .	Total value of chip specific losses
P_{spec_Ratio}	. . . . .	Ratio between chip specific losses dissipation values
P_{spec_ratio}	. . . . .	Ratio between specific chip losses (W/cm²) between SiC and Si devices
P_{sw}	. . . . .	Switching losses
PV	. . . . .	photovoltaic
q	. . . . .	Electron charge
Q_{CBC}	. . . . .	Charge of base-collector capacitance
Q_{final}	. . . . .	Gate-charge for final charging of gate-source capacitance to final voltage level

Q_{gate}	. . . . .	Overall gate charge
Q_{gd}	. . . . .	Gate-drain capacitance charge
Q_{gs}	. . . . .	Gate-source capacitance charge
Q_{gs}*	. . . . .	Gate-source capacitance charge after gate voltage reaches thershold level
Q_{miller}	. . . . .	Miller capacitance charge
r	. . . . .	ripple factor
R_{ac}	. . . . .	AC winding resistance
R_{base}	. . . . .	Base resistor
R_{dc}	. . . . .	DC winding resistance
R_{dson}	. . . . .	Drain-source on-resitance
RESURF	. . . . .	Reduced surface field
RF	. . . . .	Radio frequency
R_g	. . . . .	Gate resistor
R_{on}	. . . . .	On-state resistance
R_{on_sp}	. . . . .	On-state specific chip resistance
R_{spec}	. . . . .	Specific chip resitance
R_{spec_Ratio}	. . . . .	Ratio between specific chip resistances
$R_{th\_ja\_norm}$	. . . . .	Normalized thermal resitance between junction-ambient
SBD	. . . . .	Schottky-barrier diode
Si	. . . . .	Silicon
SiC	. . . . .	Silicon Carbide
SIT	. . . . .	Surface induction transistor
SOA	. . . . .	Safe operation area
T_a	. . . . .	Ambient temperature
$t_{current,rise}$	. . . . .	Current rise time

$t_{delay,on}$	. . . . .	Delay time at turn-on
$t_{delay,off}$	. . . . .	Delay time at turn-off
T_{drop}	. . . . .	transient time towards nominal voltage drop
$t_{fall\_voltage}$	. . . . .	Approximate voltage fall time
T_j	. . . . .	Junction temperature
T_{ref}	. . . . .	Reference temperature level
$t_{rise\_current}$	. . . . .	Approximate current rise time
T_{sw}	. . . . .	Switching period
$T_{switching}$	. . . . .	Switching time
$t_{voltage,fall}$	. . . . .	Voltage fall time at turn-on
$t_{voltage,rise}$	. . . . .	Voltage rise time at turn-on
$V_{BC,sat}$	. . . . .	Saturation voltage of base-collector junction in the BJT
V_{be}	. . . . .	Base emitter voltage of the BJT
$V_{BE,sat}$	. . . . .	Saturation voltage of base-emitter junction in the BJT
V_{br}	. . . . .	Breakdown voltage
V_D	. . . . .	Commutation voltage
V_{GS}	. . . . .	Gate-source voltage
V_{GS_JFET}	. . . . .	Gate-source driving voltage of JFET
V_{GS_MOS}	. . . . .	Gate-source driving voltage of auxiliary MOSFET
V_{GS_ON}	. . . . .	Gate-source activation voltage
V_{in}	. . . . .	Input voltage
VJFET	. . . . .	Vertical junction field effect transistor
V_L	. . . . .	inductor volume

V_{nom}	. . . . .	nominal voltage drop for selected current value
V_{out}	. . . . .	Output voltage
$V_{plateau}$	. . . . .	Miller plateau voltage level
$V_{ratio\_heatsink}$	. . . . .	Proportion of enclosure volume affected by heatsink/cooling
V_{ratio_mag}	. . . . .	Proportion of enclosure volume affected by magnetics
V_{supply}	. . . . .	Supply voltage of driving circuit
V_{TH}	. . . . .	Gate threshold voltage
WBG	. . . . .	Wide Band Gap
w_{drift}	. . . . .	Width of the drift-layer
X_{enc}	. . . . .	Changes on expenditure with enclosure
X_{mag}	. . . . .	Changes on expenditure with magnetics
X_{sem}	. . . . .	Changes on expenditure with semiconductors
y_{Esw}	. . . . .	Relative switching energy of silicon carbide devices against Si devices
ΔB	. . . . .	magnetic flux swing
$\Delta I\%$	. . . . .	percentaged current ripple
ΔI_{max}	. . . . .	maximum current ripple

List of the Figures

List of the tables

The high breakdown field from WBG materials allows the construction of unipolar devices with very low specific chip resistance mainly characterized by very low conduction and switching losses, even at high blocking voltages. Suitable concepts for SiC and GaN range from traditional FET structures driven by a MOS interface or a PN-Junction, bipolar devices and even high-electron mobility transistors (HEMT). A detailed revision of the literature will be performed in this work with the objective of providing a broad overview of possible approaches, along with inherent advantages and limitations. In addition to this, a benchmarking of several SiC-based devices technologies rated for 1200 V and 1700 V will be performed against their state-of-the-art Silicon-counterparts.

Concerning the application of wide band gap devices in renewable energy systems, a significant cost reduction potential can be obtained due to smaller expenditure with magnetic filters and cooling, alongside higher efficiency levels. These aspects will be discussed in details in order to identify constraints and bottlenecks at application level with special focus on photovoltaic and wind power systems.

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