15 Elektrische Energiesysteme

Christian Jochen Felgemacher

Investigation of Reliability Aspects of Power Semiconductors in Photovoltaic Central Inverters for Sunbelt Regions

kassel university press

KDEE Kompetenzzentrum für Dezentrale Elektrische Energieversorgungstechnik

EVS Elektrische EnergieVersorgungsSysteme

Elektrische Energiesysteme

Band 15

Herausgegeben vom
Kompetenzzentrum für Dezentrale
Elektrische Energieversorgungstechnik

Investigation of Reliability Aspects of Power Semiconductors in Photovoltaic Central Inverters for Sunbelt Regions

Christian Jochen Felgemacher

kassel university press

This work has been accepted by the Faculty of Electrical Engineering / Computer Science of the University of Kassel as a thesis for acquiring the academic degree of Doktor der Ingenieurwissenschaften (Dr.-Ing.).

Supervisor:	Prof. Dr.-Ing. habil. Peter Zacharias, University of Kassel
Co-Supervisor:	Prof. Dr.-Ing. Marco Liserre, Christian-Albrechts-Universität zu Kiel
Defense day:	30th January 2018

Bibliographic information published by Deutsche Nationalbibliothek
The Deutsche Nationalbibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data is available in the Internet at http://dnb.dnb.de.

Zugl.: Kassel, Univ., Diss. 2018
ISBN 978-3-7376-0494-9 (print)
ISBN 978-3-7376-0495-6 (e-book)
DOI: http://dx.medra.org/10.19211/KUP9783737604956
URN: http://nbn-resolving.de/urn:nbn:de:0002-404959

© 2018, kassel university press GmbH, Kassel
www.upress.uni-kassel.de

Printed in Germany

Acknowledgements

The research that this dissertation is based on was performed while I worked at the department of Electrical Power Supply Systems (EVS) within the Centre of Competence for Distributed Power Technology (KDEE) at the University of Kassel from February 2012 to March 2017.

During my time in Kassel I had the pleasure to work with many great colleagues. I thank all of you for making the department an enjoyable workplace, for being available to discuss ideas and solve problems together and for all your support. Many of you have become good friends. Thank you!

I also thank everyone I worked with in industrial partner companies and research institutions which were partners in the different projects. I have learned a lot, met many very nice and helpful people and received much support and advice.

Most importantly I thank Prof. Dr.-Ing. habil. Peter Zacharias for giving me the opportunity to join the department in 2012 and giving me the chance to gather my first experience in the vast field of power electronics. I also thank him for his frequent input of great ideas and many interesting discussions. I further thank Prof. Dr.-Ing. Marco Liserre for taking interest in my work and investing his time as second examiner and to Prof. Dr. rer. nat. Ludwig Brabetz and Prof. Dr.-Ing. Mike Meinhardt who took part as examiners in the thesis defence.

I gratefully acknowledge that a large share of the research that went into this dissertation was conducted as part of the research projects *GigaPV* and *HHK* which were funded by the German Federal Ministry for Education and Research. Responsibility for all results presented here lies solely with the author.

Finally, I thank my parents for always supporting me in so many ways - not only on my journey of education - and Yvonne for providing the motivation and encouragement that helped me complete this work.

Tönisvorst, February 2018 Christian Felgemacher

Kurzfassung

Hohe Zuverlässigkeit und Systemlebensdauern im Bereich von 30 Jahren sind für Systeme zur Nutzung erneuerbarer Energien essentiell zur Minimierung der Kosten für die gewonnene elektrische Energie. Es ist daher wichtig, dass Photovoltaik-Wechselrichter neben einem hohen Wirkungsgrad auch ein hohes Zuverlässigkeitsniveau sowie lange Lebensdauern aufweisen. Dies ist zu erreichen während gleichzeitig herausfordernde Kostenziele einzuhalten sind.

In dieser Dissertation werden Aspekte der Zuverlässigkeit von Leistungshalbleitern in Photovoltaik-Zentralwechselrichtern untersucht. Die durchgeführten Arbeiten sollen einen Beitrag dazu leisten Methoden aufzuzeigen um die auftretenden Belastungen zu Bewerten und so die Entwicklung zukünftiger Systeme zu unterstützen.

Auf Bauteilebene wurde eine umfassende Messkampagne zur Ermittlung der spannungsabhängigen Ausfallrate von Silicium und Siliciumcarbid Leistungshalbleitern auf Grund von Single-Event-Burnout durch Höhenstrahlung durchgeführt. In Kapitel 3 werden die Untersuchungsmethode sowie die betrachteten Halbleitern beschrieben und die erzielten Messergebnisse werden diskutiert.

Auf Systemebene wurde eine Simulation entwickelt um die Temperatur- und Spannungsbelastungen der Leistungshalbleiter (IGBT Module) in Photovoltaik-Zentralwechselrichtern die in verschiedenen Regionen der Welt betrieben werden zu ermitteln. Es wurde gezeigt, wie die ermittelten Belastungen in Relation zur Belastbarkeit der Bauteile gesetzt werden können (z.b. zur spannungsabhängigen Ausfallrate auf Grund von Single-Event-Burnout und zur Zyklenfestigkeit der Module) um zu evaluieren ob ein bestimmtes Design die Spezifikationen erfüllt.

Die entwickelte Simulation wurde außerdem verwendet, um Methoden zu untersuchen um die Regelung des Kühlsystems zu optimieren um die Belastung der Halbleitermodule durch Temperaturzyklen zu minimieren.

Außerdem wurde eine Methodik zur Messung der Chiptemperatur von IGBTs während dem Betrieb von Leistungswandlern erfolgreich in einem Laboraufbau eines dreiphasigen Wechselrichters implementiert.

Abstract

High reliability and a system lifetime in the range of 30 years are essential for renewable energy systems such as photovoltaic power plants to achieve minimal cost for the generated electric energy. In addition to the key requirement of a photovoltaic inverter design to achieve a high conversion efficiency it is therefore very important to maintain or even improve the level of reliability over a long lifetime while meeting challenging cost targets.

In this dissertation aspects concerning the reliability of power semiconductors in photovoltaic central inverters are investigated. The work that was carried out aims to contribute to the development of future systems by presenting methods that can be used to assess the stresses that occur in the application.

On the device level an extensive measurement campaign to determine the voltage dependent failure rate of Si and SiC power semiconductor devices due to single-event-burnout caused by terrestrial cosmic radiation was undertaken. In chapter 3 the experimental method and the investigated semiconductors are described and the obtained measurement results are discussed.

On the system level a simulation was developed to determine the temperature and voltage stress on power semiconductors (IGBT modules) in photovoltaic central inverters operated in different regions of the world. It was shown how the determined stresses can be related to the robustness of the devices (e.g. the measured voltage dependent failure rate due to single-event-burnout and the cycling capability of the modules) to evaluate whether a certain design meets the specifications.

The developed simulation was also used to investigate ways to optimise the control of the cooling system in order to reduce the temperature cycling stress on the power semiconductor modules.

Additionally, a methodology to measure the chip temperatures of IGBTs during operation of a power converter was implemented successfully in a laboratory set-up of a three phase inverter.

Previous publications

Parts of the information presented in this dissertation was previously included in the following publications:

Christian Felgemacher, Wolfram Kruschel, Lars Döring and Peter Zacharias. 'Herausforderungen für Zuverlässigkeit und Lebensdauer leistungselektronischer Systeme in der Energieversorgung'. In: *Konferenz für Nachhaltige Energieversorgung und Integration von Speichern (NEIS)*. 2013.

Christian Felgemacher, Wolfram Kruschel, Christian Nöding and Peter Zacharias. 'Reliability Aspects of a Power Electronic Voltage Regulator for Active Low-Voltage Distribution Networks'. In: *IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*. June 2015. DOI: 10.1109/PEDG.2015.7223018.

Christian Felgemacher, Samuel Araújo, Christian Nöding, Peter Zacharias, Alexander Ehrlich and Martin Schidleja. 'Evaluation of Temperature Cycling Stress imposed on Power Electronic Modules in Photovoltaic Central Inverters in Sunbelt Regions'. In: *CIPS 2016 - 9th International Conference on Integrated Power Electronic Systems*. 2016.

Christian Felgemacher, Benjamin Dombert, Christian Nöding and Peter Zacharias. 'IGBT Online-Temperature Monitoring using Turn-Off Delay as a Temperature Sensitive Electrical Parameter'. In: *CIPS 2016 - 9th International Conference on Integrated Power Electronic Systems*. 2016.

Christian Felgemacher, Samuel Araújo, Peter Zacharias, Karl Nesemann and Artjom Gruber. 'Cosmic Radiation Ruggedness of Si and SiC Power Semiconductors'. In: *28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. 2016, pp. 51–54. DOI: 10.1109/ISPSD.2016.7520775.

Christian Felgemacher, Samuel Araújo and Peter Zacharias. 'Benefits of increased cosmic radiation robustness of SiC semiconductors in large power-converters'. In: *PCIM Europe 2016*. 2016.

Christian Jochen Felgemacher, Christian Nöding, Samuel Vasconcelos Araújo and Peter Zacharias. 'Verfahren zur Steuerung einer Kühlvorrichtung zur Lebensdauererhöhung Abwärme erzeugender Komponenten und Kühlvorrichtung'. Offenlegungsschrift DE 10 2014 112 458 A1.

Christian Jochen Felgemacher, Christian Nöding, Peter Zacharias and Samuel Vasconcelos Araújo. 'Method for Controlling a Cooling Device for Increasing the Lifetime of Components Generating Waste Heat, and Cooling Device'. Patent Application Publication US 2016/0065126 A1.

Contents

Acknowledgements v

Kurzfassung vii

Abstract ix

Previous publications xi

1. Introduction 1
- 1.1. Motivation . . . 2
- 1.2. Research objective and overview of work . . . 4

2. Background 5
- 2.1. Introduction . . . 5
- 2.2. Lifetime and reliability . . . 5
- 2.3. Photovoltaic inverters in utility scale systems . . . 8
- 2.4. Power semiconductor modules . . . 9
  - 2.4.1. Packaging related failure mechanisms . . . 10
  - 2.4.2. Device related failure mechanisms . . . 11
- 2.5. Methodology for reliability evaluation . . . 13
- 2.6. Conclusion . . . 16

3. Cosmic radiation ruggedness of power semiconductor devices 17
- 3.1. Introduction . . . 17
- 3.2. Background on cosmic radiation . . . 18
  - 3.2.1. Origin and characteristics of cosmic radiation . . . 18
  - 3.2.2. Factors influencing the terrestrial neutron flux . . . 19
  - 3.2.3. Conclusion . . . 21
- 3.3. Single-event-burnout in power semiconductors . . . 22
  - 3.3.1. Description of the SEB failure mechanism . . . 22
  - 3.3.2. Failure rates for SEB in power semiconductors . . . 23
  - 3.3.3. Conclusion . . . 24

3.4. Methodology for SEB failure rate measurements 25
3.4.1. Neutron irradiation facility 25
3.4.2. Experimental set-up 26
3.4.3. Measurement procedure 30
3.5. Devices under test 31
3.6. Experimental results 32
3.7. Comparison of results with data from literature 38
3.8. Long-term experiment for result validation 40
3.9. Conclusion 41

4. Lifetime and reliability of IGBT modules in PV central inverters 45
4.1. Introduction 45
4.2. Photovoltaic system simulation 46
4.2.1. Topology of the investigated photovoltaic system 46
4.2.2. Overview of photovoltaic system simulation 47
4.2.3. Simulation of photovoltaic generator 49
4.2.4. Behavioural model of the photovoltaic inverter 57
4.2.5. Computation of semiconductor losses 59
4.2.6. Thermal model of the power electronic stack 61
4.2.7. Simulation outputs 65
4.2.8. Summary of simulation features 71
4.3. Evaluation of stresses on power semiconductors 72
4.3.1. Estimation of lifetime limits due to cycling load 72
4.3.2. Estimation of single-event-burnout failure rate 73
4.4. Investigated scenarios 74
4.5. Results 76
4.5.1. Temperature cycling stress on IGBT modules 76
4.5.2. Semiconductor failure rate due to cosmic radiation 79
4.6. Conclusion 83

5. Cooling system control strategy to reduce temperature cycling 85
5.1. Introduction 85
5.2. Approach to optimise cooling system control 86
5.2.1. Option A: Incremental set-point adjustment 87
5.2.2. Option B: Use of prognosis to determine daily set-point . 88
5.3. Comparison of cooling system control strategies 89
5.3.1. Temperature cycling stress 90
5.3.2. Average stack temperature 92
5.3.3. Energy utilisation for cooling system 93
5.4. Conclusion 94

6. On-line temperature measurement of IGBTs **95**
6.1. Introduction 95
6.2. Methods to measure IGBT temperatures 96
6.3. Temperature sensitive electrical parameters of power semiconductors 97
6.3.1. Collector-emitter saturation voltage 97
6.3.2. Internal gate resistance 99
6.3.3. Threshold voltage 100
6.3.4. Switching delay times 100
6.3.5. Switching transients 101
6.3.6. Summary 102
6.4. Gate-drive circuit with turn-off delay measurement 104
6.5. Experimental investigation of turn-off delay as a TSEP of IGBTs 106
6.5.1. Measurement of turn-off delay of a single IGBT 107
6.5.2. Turn-off delay of parallel IGBTs with different temperatures 110
6.5.3. Turn-off delay of an IGBT in a large power module 112
6.6. Implementation of IGBT temperature monitoring in a three-phase inverter 113
6.6.1. Calibration measurements and model fitting 115
6.6.2. On-line temperature measurement during converter operation 118
6.7. Conclusion 121

7. Summary and Conclusion **123**

A. Perez model for diffuse irradiance on a tilted surface **127**

B. Details of thermal model of power electronic stack **129**

C. Simulation results using different thermal model structures **133**

D. Simulation results using different sets of climatic data **137**

Bibliography **139**

Acronyms **153**

List of symbols **155**

List of Figures **163**

List of Tables **165**

1. Introduction

In the 1990s when grid-tied photovoltaic (PV) systems were first installed in Germany in larger numbers as part of the 1000-roof program the specific cost was around 12.400 €/kWp. Such installations were not profitable for their operators even considering the large subsidies. [1]

This changed in 2000 as a high feed-in tariff for electricity from photovoltaic systems was introduced by the 100.000-roof-program within the new Renewable-Energy-Law[1], leading to a significant increase in the number of new installations in Germany. Since then photovoltaic systems with a total rated power in excess of 38 GWp have been installed in Germany alone [2]. As a consequence of scale effects and technological innovation the cost for new roof installations has dropped to less that 1.300 €/kWp in December 2014 [3].

As a result of the cost decrease photovoltaic installations can be competitive with traditional energy generation in more and more situations today. Naturally, photovoltaic electricity generation is most cost effective in regions with high solar irradiance. In some locations in so called *sunbelt regions* the levelised cost of electricity (LCOE) of large scale photovoltaic power plants was already at a level comparable to the price paid for electricity by industrial customers in 2013 [4] as a consequence of the reductions in investment costs over the last years.

Therefore, *sunbelt regions* can be considered future key markets for large scale photovoltaic power plants. However, the challenging climatic conditions in these regions put extra stress on many components and need to be taken into consideration when designing systems that have to operate reliably for operating periods in the range of 20 years.

[1] German: Erneuerbare-Energien-Gesetz (EEG)

1.1. Motivation

The main factors determining the LCOE of a photovoltaic system are the initial investment costs for the power plant, K_0, the operating costs, A_t, during the plant's lifetime and the energy output in each period, Y_t, as shown in the following equation (adapted from [5, p. 169]).

$$LCOE = \frac{K_0 + \sum_{t=1}^{n} \frac{A_t}{(1+WACC)^t}}{\sum_{t=1}^{n} \frac{Y_t}{(1+WACC)^t}} \tag{1.1}$$

In order to highlight the effect of a power plant's operating period, the lifetime of the power electronic inverters and the expected operation and maintenance (O&M) costs on the LCOE the calculations performed by Döring in [4] were extended to include variations of the factors system lifetime, inverter lifetime and operating cost [6].

The effect of the overall operating period of the entire photovoltaic power plant on the LCOE is highlighted in Figure 1.1. The diagram shows, that by extending the operating period from twenty to thirty years the LCOE in the analysed scenarios is reduced by approximately 15 %.

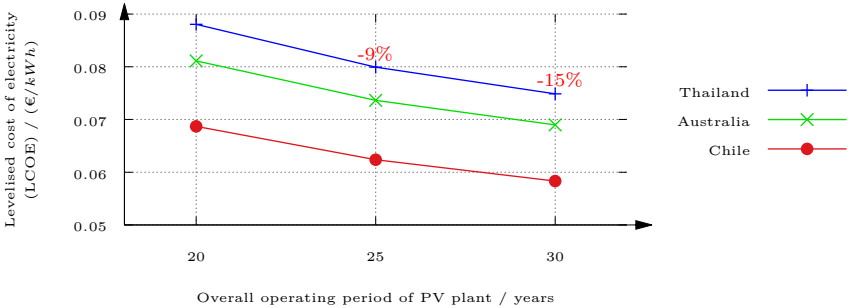


Figure 1.1.: Influence of system lifetime on LCOE for very large scale PV power plants in selected sunbelt locations. Re-plot of figure previously published in [6].

Two main components of a photovoltaic power plant are the photovoltaic generator consisting of large arrays of photovoltaic modules and the power electronic

inverters, which convert direct current from the PV generator into grid-compatible alternating current. Manufacturers of photovoltaic modules offer modules with 20 years of warranty or more. However, the average warranty period for inverters in 2012 was as low as five years [7]. This suggest that inverters may need to be replaced multiple times during the lifetime of a PV system. The effect of such replacements on the LCOE from a photovoltaic power plant was investigated using a scenario for a photovoltaic power plan in Thailand for which an overall operating period of 30 years was assumed. Initially, it was assumed that the inverters can be used for the entire operating period. As can be seen in Figure 1.2 replacing the inverters after 15 years increases the LCOE by 3 %, while replacing them every 10 years increases the LCOE by 6 %.

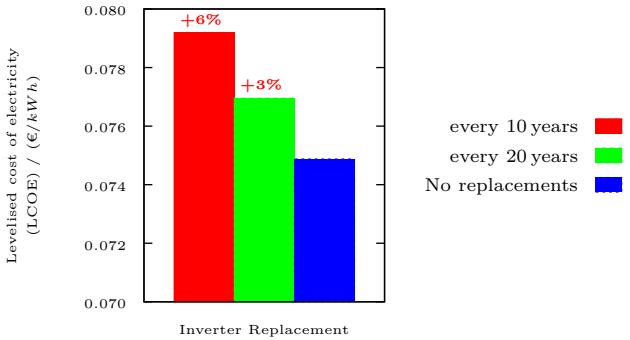


Figure 1.2.: Influence of inverter replacement periods on LCOE (Thailand, overall system lifetime 30 years). Re-plot of figure previously published in [6].

The O&M costs of a power plant also have an influence on the LCOE. In [4] O&M costs for PV power plants were assumed to be in the range of 1 % of the original investment cost per year. To highlight the effect of the O&M costs on the LCOE, this parameter has been varied between 0.5 % to 3 % of the original investment cost per year. The analysed scenario is a PV plant in Thailand with an overall system lifetime of 30 years. Figure 1.3 shows that the O&M cost have a strong influence on the LCOE.

The analysis of the factors influencing the LCOE of photovoltaic power plants shows that all components of a photovoltaic power plant need to have long operational lifetimes and operate reliably to minimize O&M costs and hence ensure profitability.

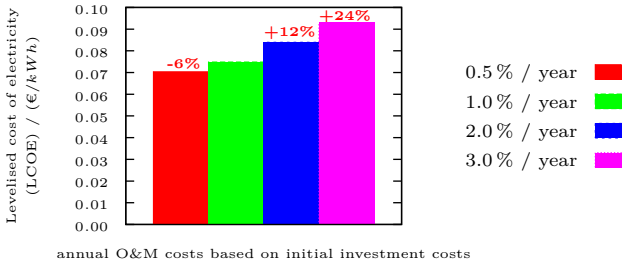


Figure 1.3.: Influence of different levels of O&M cost on LCOE (Thailand, overall system lifetime 30 years). Re-plot of figure previously published in [6].

1.2. Research objective and overview of work

The research presented in this thesis focuses on investigating aspects of the reliability of power semiconductor modules in photovoltaic central inverters in *sunbelt* regions.

On the component level an experimental investigation to determine the voltage dependent failure rate of power semiconductor devices due to terrestrial cosmic radiation was conducted. Details of the investigation are provided in Chapter 3.

On the system level a simulation to estimate the stress on the power semiconductors in a photovoltaic central inverter from realistic mission profiles comprising of climatic data and information about the set-up of the photovoltaic system and the design of the inverter was developed. Details of the simulation are provided in Chapter 4. Using the simulation the expected failure rate of the semiconductor devices in the application due to cosmic radiation induced failures is estimated and the lifetime limit due to wear-out as a consequence of temperature cycles is investigated.

The simulation was further used to investigate how changes to the control of the cooling system can be made in order to reduce the temperature cycling stress on the power semiconductor modules. Details of this investigation are shown in Chapter 5.

Finally, the results obtained from implementing an online temperature sensing solution for insulated gate bipolar transistors (IGBTs) in a small scale laboratory demonstrator of a three phase inverter are presented in Chapter 6.

2. Background

2.1. Introduction

In this chapter the terminology of *lifetime* and *reliability* is briefly introduced. Additionally, a short overview over inverters for utility scale photovoltaic systems is given and the reasons to focus on the power semiconductor modules in such inverters are discussed. Finally, some failure mechanisms relevant to power semiconductor modules are introduced and methods for reliability estimation of power converters are mentioned.

2.2. Lifetime and reliability

Reliability is a characteristic of an entity. According to the online *IEC Electropedia* [8] the reliability of an item is defined as the "ability to perform as required, without failure, for a given time interval, under given conditions". Based on this definition a statement about the reliability of an entity such as a technical product is required to include information about the required function of the product, the time duration for which the product is expected to provide this function and the conditions under which the product is operated.

In the case of a photovoltaic inverter it is expected that it converts the direct-current output of the photovoltaic generator to grid-compatible AC current within the limits of its specifications. The operating conditions are variable over time and depend on the design of the photovoltaic system as well as the location it is installed in.

The familiar bathtub curve shown in Figure 2.1 is used to explain how the terms *reliability* and *lifetime* will be used for the purpose of this investigation. The bathtub curve shows how the failure rate of a population of a product varies over time. The time can be divided into three periods. [9, p.111],[10]

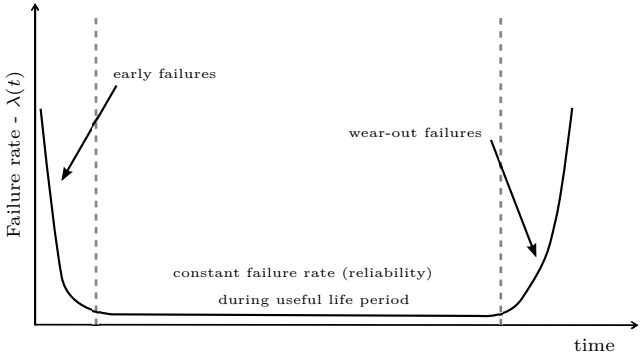


Figure 2.1.: Typical bathtub shape of a plot of the failure rate of a population of items over time. (also see [9, p.111],[10])

In the initial period the failure rate is dominated by early failures that result from weaknesses in components or materials or that are results of random weaknesses introduced in the production process. Burn-in tests are used to ensure that these early failures are caught before products are shipped.

The second period is the useful life period. During this period it is assumed that the product has a constant and hopefully low failure rate. The failure rate in this period can be used as a measure for the reliability of a product. Instead of the failure rate the mean time to failure (MTTF) is often given as a reliability metric. While the MTTF is typically expressed in years it is important to note that it expresses the average time between failures of a population in entity-years and does not give any indication of the lifetime of a product.

The third period is the wear-out period in which the failure rate increases due to deterioration of system components caused by ageing. The transition from the useful life period to the wear-out period is considered the end of lifetime for this study. While not all products will fail at that point the failure rate will start to increase.

To illustrate the difference between reliability and lifetime the failure rate over time and the survivability over time of two fictional product populations is shown in Figure 2.2. The dashed lines in the diagram represent the failure rate (hazard rate) of the two product populations while the solid lines illustrate the survivability of the population, which corresponds to the share of entities that

are still functional at a certain point in time. From the diagram one can see that products of type A have a higher reliability (lower failure rate) during the useful life period than products of type B. However, wear-out occurs much earlier for the products of type A. As a result of the increased failure rate once wear-out starts to cause failures the lifetime of the product (if one defines lifetime as the point in time where 63 % of the population have failed) is much less for product B.

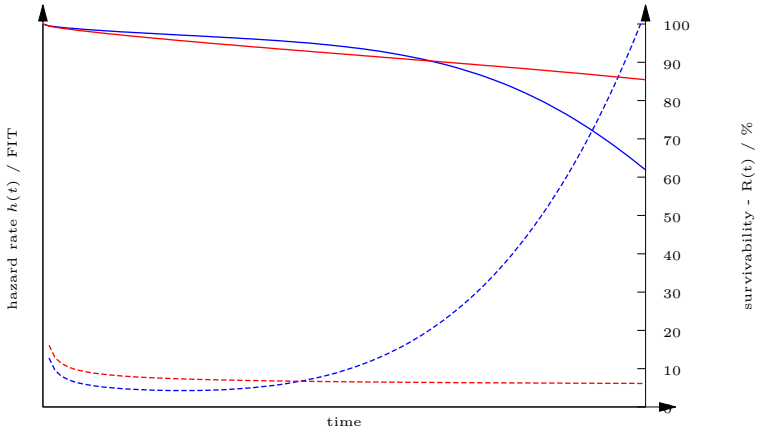


Figure 2.2.: Failure rates (dashed lines) and survivability (solid lines) of two products. (Blue: Product A, Red: Product B)

The above comparison shows that during the design of the product steps have to be taken to ensure that the onset of this increase in the failure rate due to wear-out occurs after the specified lifetime. Therefore, failure mechanisms that may occur at any time during the life cycle of the product as well as wear-out related failure mechanisms that will only appear after a certain time need to be taken into consideration to design a product that will have the desired reliability for the desired lifetime.

2.3. Photovoltaic inverters in utility scale systems

In large utility scale photovoltaic systems central inverters with power ratings upwards of a few hundred kW are commonly used. The maximum open-circuit voltage of the photovoltaic array is typically 1000 V. It is expected that systems with a maximum open circuit voltage of up to 1500 V will soon become the norm to achieve cost advantages especially through reduced costs for cabling [11].

Large photovoltaic converters are typically realised as voltage-source-converters with a DC/AC conversion stage with buck-characteristic. As a result the peak of the output voltage waveform of these converters is always less than the input voltage. While the two-level B6-topology is a well established topology for the DC/AC stage in photovoltaic central inverters, as the simple commutation circuit allows low stray inductance designs, other topologies such as interleaved B6-bridges or multi-level topologies are viable options [11].

Depending on the choice of output voltage a DC/DC converter with a boost characteristic is sometimes added as an input stage to the central inverter in order to extend the range of input voltages that the converter can operate at. An overview of DC/DC converter topologies suitable for the application can be found in [11].

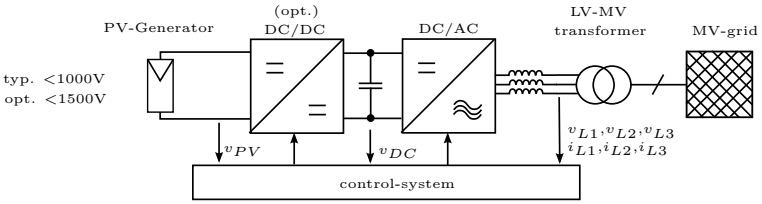


Figure 2.3.: Overview of structure of a photovoltaic central inverter. Subsystems such as auxiliary supplies, DC and AC contactors, gate-drives, etc. are not shown for clarity.

While all components in the block diagram shown above need to have high reliability and have to meet the lifetime requirement the focus of this investigation is on the power semiconductors. This choice is based on the results of a survey conducted by Yang et. al. in 2008 [12] to identify the reliability issues experienced by industry. As part of the survey the responders were asked to identify fragile components in power electronic systems. 'Power devices' were identified as most

fragile, followed by capacitors and gate drives [12]. A distribution of failure root causes reproduced by Wang in [7, 10] supports that capacitors and semiconductors are the most critical components.

Today, IGBTs are commonly used as active switches in photovoltaic central inverters. The voltage and current ratings of the IGBTs depends on the choice of topology and overall power rating of the converter. The large power ratings common in central inverters (hundreds of kW) lead to the use of power semiconductor modules that contain multiple IGBT and diode chips connected in parallel to achieve the necessary current ratings.

2.4. Power semiconductor modules

The internal structure of an industry standard power electronic module, is shown in Figure 2.4. As can be seen, the module is made up of a stack of different materials. A direct copper bonded (DCB) ceramic substrate is soldered on top of the module baseplate (Cu). The semiconductor chips (Si) are soldered to the DCB and top-side interconnections are made using aluminium bond-wires. Typically, a number of IGBT chips and diode chips are connected in parallel to achieve the desired current rating of the module.

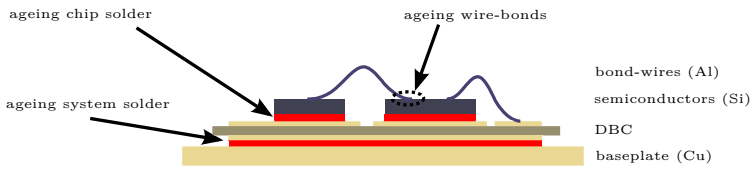


Figure 2.4.: Cross section of standard power module - also see [13, 14]

Failures of power semiconductor modules can be attributed either to the semiconductor device itself or to the package. Alternatively, one could also classify the failures as wear-out failures (usually package related) or catastrophic failures caused by overstress of the device. Information on the different failure mechanisms can be found in many publications in literature (see e.g. [13–19]).

2.4.1. Packaging related failure mechanisms

Losses in the semiconductor chips result in the heating of the chips as well as the various materials in the thermal path. The semiconductor losses change over time since the power output of the inverter varies as a consequence of solar irradiance. Hence, temperature swings occur at the interfaces between the materials inside the power electronic module. Since each of the materials within the IGBT module has a different coefficient of thermal expansion (CTE) the temperature swings lead to thermo-mechanical stress. Over time this stress leads to deterioration of the bond-wire (Al) to chip (Si) interface as well as at the die-attach solder and the substrate to baseplate solder. [16, 19, 20]

In the past years many technological advances were made to improve the standard module as described above in order to increase the cycling capability. Lutz provides an overview of the approaches that are used to increase the cycling capability in [13]. Amongst the approaches to increase the cycling capability are the use of Cu wire-bonds as well as the replacement of solder layers by sintered silver layers or diffusion soldering [21]. Other approaches are to completely eliminate the wire-bonds and replace them by a flexible foil sintered to the top-side of the devices [22].

Modern IGBT modules with optimised wire-bonds and solder / sinter layers (e.g. Infineon .XT technology) as well as modules that make use of sinter layers and have eliminated the wire-bonds (e.g. Semikron SKiN technology) far exceed the cycling capability of the standard module shown in the beginning of this section [21, 22].

The robustness of a certain power semiconductor module technology against wear-out failures induced by temperature cycles is commonly evaluated by conducting accelerated tests. Two main types of tests are conducted: (active) power cycling and (passive) thermal cycling tests.

Passive thermal cycling tests are conducted by placing the modules into a thermal chamber and repeatedly changing the temperature to expose the modules to a certain temperature swing. To conduct active power cycling tests losses are generated in the semiconductor chips within the module by applying a suitably high current for a time in the region of a few seconds. The heating current is then turned off and the chip cools down.

In both types of accelerated tests the electrical and thermal parameters of the devices under test are continuously monitored to detect deteriorations. Failure criteria have to be defined (e.g. a certain percentage increase in forward voltage

or thermal resistance) and testing is done until measurements on the device under test (DUT) show that the failure criteria are exceeded.

Based on cycling tests models for the cycling capability of the models are formulated. Models for the power cycling capability of standard modules such as the LESIT model [23] or the CIPS08 model [24] are available in literature. The LESIT model relates the number of cycles until failure N_f to the junction temperature swing ΔT_j and the mean temperature T_m as per the following equation

$$N_f = A \cdot \Delta T_j^{\alpha} \cdot exp\left(\frac{Q}{R \cdot T_m}\right) \tag{2.1}$$

where $A = 640$, α = -5, $R = 8.314\,\mathrm{J\,mol^{-1}\,K}$ and $Q = 7.8 \times 10^4\,\mathrm{J\,mol^{-1}}$ [23]. The CIPS08 model also takes into consideration the pulse on-time, the voltage rating of the chip, the current per bond-wire and the bond-wire diameter [24].

From the point of view of a system designer instead of using literature models it is preferable to obtain cycling capability data for the relevant modules from the module manufacturer. Such data is usually provided in the form of diagrams that illustrate the permissible number of cycles as a function of temperature swing, either for the chip temperate or for the case temperature. Additional factors such as the pulse on-time may also be given as discussed in [25].

To evaluate whether a module will withstand the cycling stress in a certain application the temperature cycles expected during the desired operating time need to be estimated. It is therefore necessary to find out during the design phase of a power electronic system how many power / temperature cycles of a certain temperature swing and average temperature the power semiconductor modules will be exposed to. For that purpose electro-thermal simulations taking into consideration the mission profile for the relevant application can be conducted.

2.4.2. Device related failure mechanisms

In [17] Wu et. al. review 'catastrophic failures' of IGBTs and further classify these as either short-circuit or open-circuit failures. The open-circuit failures are a consequence of bond-wire lift-offs or gate-driver failures, while the discussed short-circuit failures occur as a consequence of *high voltage breakdown*, *latch-up*, *second breakdown* or *energy shocks* [17].

Another failure mechanism at the device level is the *degradation of the gate-oxide*. Gate oxide degradation can occur quickly if the oxide is over-stressed or over a longer time period at lower stress. [16] For the purpose of this investigation it is assumed that gate voltages are always maintained within the specified ranges in a converter and that these specifications are defined to avoid issues with the gate oxide.

Most of the failures that occur at the device level due to the mentioned failure mechanisms are consequences of exposing the IGBT to stresses outside its capabilities. Examples for such over-stresses are an excessive collector-emitter voltage V_{CE} or excessive currents (e.g. short-circuit currents). These failures mechanisms due to over-stress will not be further considered within this investigation, as it is assumed that design measures are taken to avoid such over-stresses from destroying the semiconductors in a converter. As no actual design for a large converter will be done these are outside the scope of this investigation.

The impact of a high energy terrestrial cosmic radiation particle in a voltage blocking semiconductor can lead to catastrophic failure as was first discovered in the 1990s [26–29]. The failure rate of a given device due to cosmic radiation induced failures depends strongly on the voltage applied to the semiconductor device as is shown for example in data for power semiconductors in [30, 31]. In the same source the dependence on altitude (due to increasing terrestrial cosmic radiation with altitude) and device temperature is also shown.

The system designer needs to estimate the voltage stress in a given application in order to compute the estimated failure rate based on the cosmic radiation robustness of the considered device. If the estimated failure rate is above the level acceptable for the reliability of the system devices with a higher robustness need to be used. In many cases this results in the use of devices of a higher voltage class or multi-level topologies, which increases system complexity and cost.

2.5. Methodology for reliability evaluation

To evaluate the reliability of a design for a power electronic converter the so called parts-count-method or parts-stress methods can be used as discussed by Walter in [32]. To estimate the failure rate using the parts-count method failure-rates for each component from a failure-rate catalogue such as MIL-HDBK-217F [33] are used. The estimate for the total failure rate is obtained by summing the failure-rates across all components in a system. The parts-stress method additionally assigns stress level dependent scaling factors to the failure rate for each device. These factors are also obtained from a catalogue such as MIL-HDBK-217F. This has the advantage of including some information regarding the stress applied to the component in the application.

In [32] Walter presents a methodology to compare the reliability of different power electronic converter designs. The stresses on the different components in a converter are obtained through electrical and thermal simulations and the failure rates are estimated based on handbook data and some additional factors.

The disadvantage of the parts-count and parts-stress methodologies is their reliance on data in reliability handbooks and failure rate catalogues. As the catalogues are based on historical data (e.g. MIL-HDBK-217F was last updated in 1995) the data may not be applicable to the components available for new designs. Also, the failure rates calculated from the handbook methods do not give any indications of the causes of the failures [10]. Furthermore, calculated MTTF values obtained by using the handbook methods generally assume constant failure rates and that no wear-out occurs. If these assumptions are not met significant inaccuracies can be expected [10].

An altogether different approach to predict the reliability of a certain power electronic converter system is to follow design for reliability (DfR) procedures that take into consideration the physics-of-failure method as illustrated for example by Wang et. al in [10]. Instead of using historical data for the expected failure rate of each component the detailed failure mechanisms are analysed and models are formulated that relate the stress to the failure-rate based on the underlying physical process that leads to the failure. An example is to link the change in electrical and thermal behaviour of a power semiconductor module to the temperature cycling stress which causes crack-growth due to electro thermal stress.

If the failure mechanisms affecting a certain component are known, suitable models of the failure mechanisms are available, and the relevant stresses can be

identified from the mission profile (e.g. by using a simulation) the stresses can be related to the strength of the component and a failure-rate or lifetime limit for the component can be identified. In Figure 2.5 the process of looking at every imaginable failure mechanisms for every component in a system to evaluate the reliability / lifetime of the system is illustrated.

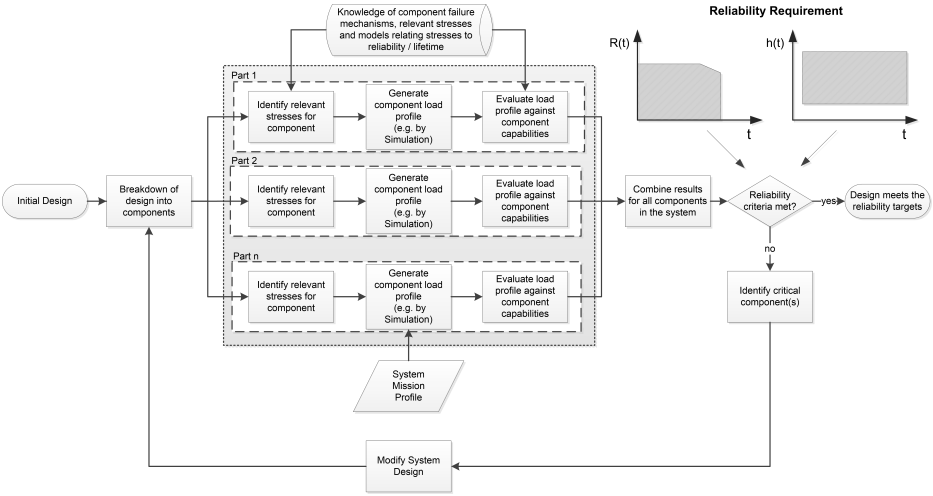


Figure 2.5.: Flowchart for the reliability prediction of power electronic systems. Similar illustration previously published in [34]

To combine the results of analysing each component and failure-mechanism for an entire system the estimated information can be combined along the branches of a fault-tree that illustrates how failures of individual components may combine to cause a system failure as illustrated in Figure 2.6. Such a fault tree can be obtained for an entire system for example by performing a fault tree analysis (FTA) For information on the FTA see e.g. [9, pp.251].

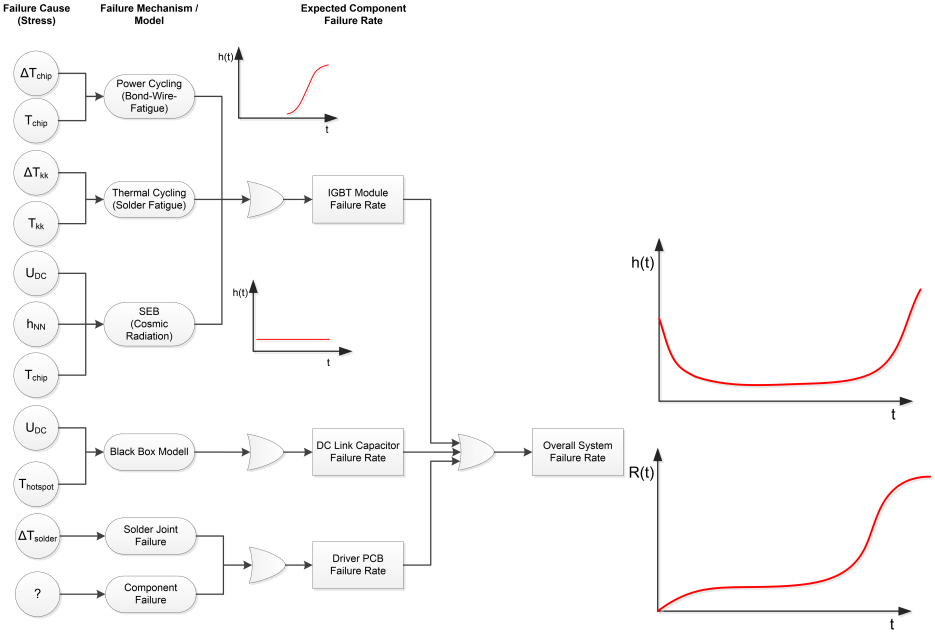


Figure 2.6.: Combining failure rates to estimate system the system failure rate.

In chapter 4 a system level simulation of a photovoltaic central inverter will be presented that allows stresses on the power semiconductor to be estimated from a mission profile for a certain location. Estimating the stresses on a component is necessary to perform investigations using physics-of-failure-based models to estimate the reliability and lifetime of the power semiconductor modules in photovoltaic central inverters.

Similar work is described for various applications in literature. Wang et. al. [10] provide an overview of the physics of failure based design for reliability approach along with a case study in which the temperature cycling stress in a 2.3 MW wind power converter is analysed. In [35] Senturk et. al. analyse the temperature

cycling stress on the semiconductors in the grid side converter of a large wind turbine. In [36] a lifetime estimation for a wind power converter is taken out. The cycling load on the components in a three phase BS-NPC silicon carbide (SiC) PV-inverter with 12 kV A rated power is estimated in [37].

2.6. Conclusion

In this chapter the terminology of reliability and lifetime used in the remainder of this investigation were introduced. Additionally, the key specifications of photovoltaic central inverters as the key elements of very large photovoltaic power plants were briefly discussed.

Since the focus of the investigation presented in this work is on the power semiconductor modules within photovoltaic central inverters a brief overview of the relevant failure mechanisms for state of the art IGBT modules was provided. Finally, the physics of failure based method of reliability and lifetime prediction was introduced.

3. Cosmic radiation ruggedness of power semiconductor devices

3.1. Introduction

A very important failure mechanism of power semiconductor devices is the occurrence of single event failures triggered by cosmic radiation. The term single event burnout (SEB) is used in this investigation to denote all catastrophic failures as a consequence of impacts of high energy particles from terrestrial cosmic radiation, even though multiple underlying failure modes (SEB / single event gate rupture (SEGR)) exist.

The objective of the research presented in this chapter is to analyse the susceptibility of different types of power semiconductors, specifically those made of silicon carbide (SiC) and silicon (Si), to terrestrial cosmic radiation.

To introduce the investigation the characteristics and origins of terrestrial cosmic radiation are described and an overview of the failure mechanism that causes power semiconductors to fail due to terrestrial cosmic radiation is presented. The experimental method that was followed to measure the cosmic radiation susceptibility of semiconductors is then described. Afterwards, the measurement results obtained from the experiments are presented. Finally, the experimental results are discussed, compared with the available information from literature and conclusions are drawn from the investigation.

The research presented in this chapter was conducted as part of the research project *HHK*[1]. The results of the performed measurements along with information about the experimental set-up and measurement procedure were previously published by the author in [38].

[1] Joint research project funded by the German Federal Ministry of Education and Research

3.2. Background on cosmic radiation

3.2.1. Origin and characteristics of cosmic radiation

When talking about cosmic radiation it is important to distinguish between the primary cosmic radiation that strikes the earth's atmosphere from outer space and the terrestrial (secondary) cosmic radiation observed on the earth's surface.

Primary cosmic radiation is a high energy particle radiation consisting of stable, charged particles, mainly hydrogen and helium nuclei, accelerated to very high speeds in the range of 1 MeV up to and exceeding 300 EeV [39]. The flux rate of particles exponentially decreases as particle energies increase and is illustrated for example in [39–41]. In comparison, the LHC at CERN can accelerate protons to 3.5 TeV [42] which highlights the immense energy of some of the primary cosmic radiation particles.

Particles with energies below 1 GeV can mainly be attributed to the sun and up to 10 GeV the flux measured on earth is modulated by solar activity [40]. Particles with higher energies originate from outside our solar system and possibly even outside our galaxy [40]. Research into the mechanisms that accelerate the primary particles to extremely high energies is ongoing [39, 40].

The primary cosmic radiation particles do not reach the earth surface as they collide with molecules in the atmosphere (mainly O_2 and N_2) creating cascades of secondary particles. The secondary cosmic radiation that can be observed on the earth surface is a result of these collisions and consists of photons (γ-radiation), electrons and positrons, muons and hadrons (neutrons, protons, pions). [40]

As discussed by Kaindl [43] and Weiß [44] the components of the secondary cosmic radiation which are most relevant for interactions with silicon atoms inside of power semiconductors are the nucleons (neutrons and protons). As the number of neutrons reaching the earth's surface is much higher than that of protons [45] and since shielding against protons is relatively simple [44], neutrons are the relevant component of terrestrial cosmic radiation when considering single-event-effects in power semiconductors. Thus, for the remainder of this investigation only the terrestrial neutron flux rate induced by cosmic radiation will be considered.

The reference spectrum of the flux of neutrons at sea level for New York City (NYC) as given in JESD89A is shown in Figure 3.1. The total flux of the spectrum above 10 MeV is 3.6×10^{-3} n/cm^{2}s. [46]

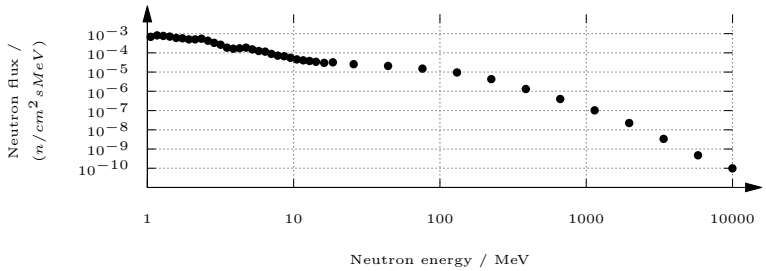


Figure 3.1.: Reference neutron flux for New York City. (Source of data: [46])

3.2.2. Factors influencing the terrestrial neutron flux

The main variable influencing the local neutron flux rate is the altitude above sea level. At an altitude of 3000 m the neutron flux is approximately 10 times greater than at sea level [46], which illustrates that the elevation of a site at which power electronic equipment is to be installed has to be taken into account when estimating the local neutron flux and hence the component failure rates.

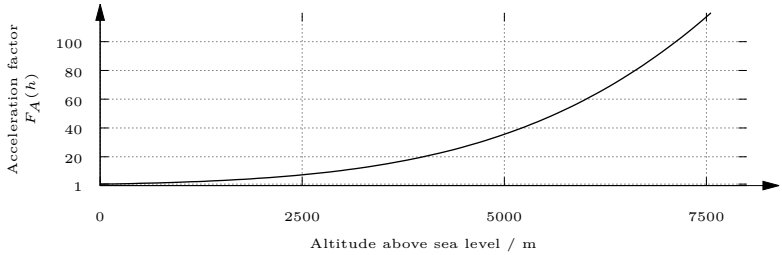


Figure 3.2.: Altitude dependent acceleration factor for terrestrial neutron flux. (for underlying equation see: [46])

Additionally, the flux rate is influenced by the position of a location within the earth's geomagnetic field. The maximum difference in neutron flux rate between two locations due to variations in the geomagnetic field can reach a factor of 2 to 3 (at the highest inhabited altitudes) [46]. The third factor influencing the neutron flux rate is the solar activity. As can be seen from Figure 3.3 the neutron flux rate varies periodically with a period of around 12 years.

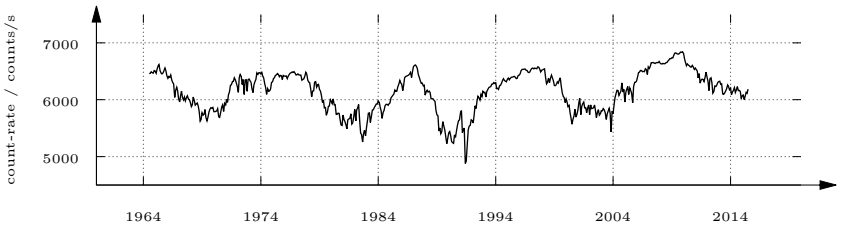


Figure 3.3.: Monthly averages of recorded neutron count rate at Oulu Neutron Monitor for a period of 51 years. (Source of data: [47])

According to [46] the neutron differential flux at any location can be expressed as the product of the reference spectrum and the scaling factors for altitude, F_A, and for the influence of the geomagnetic location and solar modulation, F_B. The combined dependency of the neutron flux on the altitude and the geomagnetic rigidity is illustrated in the map[2] in Figure 3.4.

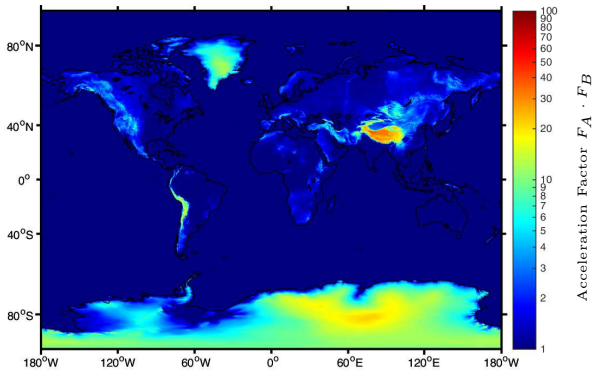


Figure 3.4.: Relative neutron flux rate based on location (scaling factor $F_A \cdot F_B$) at average solar activity. Calculated using the method and rigidity cut-off data from [46] in combination with global elevation data from [48].

[2]Plotted using Rich Pawlowicz's M_Map toolbox: `https://www.eoas.ubc.ca/~rich/map.html`

Figure 3.4 shows that areas with high elevation above sea level as well as regions close to the poles exhibit large terrestrial neutron flux rates, as is expected. However, also in areas with moderate elevations significant increases in the neutron flux rate can be observed.

To illustrate the importance of considering the local neutron flux rate for the estimation of failure rates the calculated scaling factors for a number of sunbelt regions is shown in the Figure 3.5. The values show that in some sunbelt locations, which are attractive for the installation of photovoltaic power systems, a neutron flux of up to five times the intensity than at the reference location is to be expected.

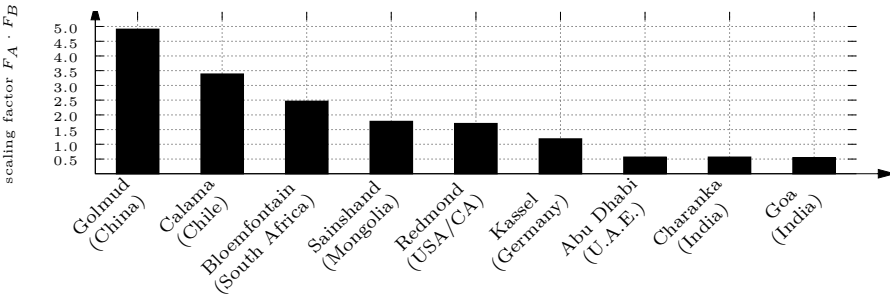


Figure 3.5.: Scaling factor for terrestrial neutron flux in sunbelt locations with potential for large scale photovoltaic installations.

3.2.3. Conclusion

Terrestrial cosmic radiation is omnipresent on the earth's surface. For power semiconductors the neutron flux is the most damaging component of the terrestrial cosmic radiation as it can trigger catastrophic single-event failures.

To estimate the probability of equipment failures due to terrestrial cosmic radiation it is essential to know the stress at a given location, which depends on the elevation and geomagnetic conditions. The methodology described in JESD89A [46] can be used to calculate the neutron flux for any location relative to the reference of New York City.

Since it is not feasible to shield power semiconductors against the neutron flux accurate knowledge of the failure rates that have to be expected is required to be able to calculate the probability of a cosmic radiation induced failure of power electronic equipment.

3.3. Single-event-burnout in power semiconductors

In this section the failure mechanism known as single event burnout (SEB) in power semiconductor devices is summarised briefly. Additionally, data on the susceptibility of different power semiconductor devices that is available from literature is presented. Finally, based on the presented information the motivation to undertake a testing campaign to characterize different semiconductor devices is given.

3.3.1. Description of the SEB failure mechanism

The underlying process leading to single event burnout in a power semiconductor as a consequence of a collision between a high-energy atmospheric neutron and a silicon nucleus is described as a three stage process in the work of Weiß [44, pp.13] and is very briefly summarised in the following paragraphs.

- **Step 1: Neutron impact**
  A high energy atmospheric neutron passing through the space charge region of a voltage blocking semiconductor will collide with a silicon nucleus with a certain probability. Through a nuclear reaction light ions, which have kinetic energies in the region of 10 to 100 MeV, are created. This first step happens within the first few 10 ps after the neutron impact.
- **Step 2: Formation of a conductive channel**
  The deceleration of the ions produced as a consequence of the neutron impact leads to the creation of a localised electron-hole plasma and the electric field in this location breaks down. At the edges of the plasma very steep field peaks occur. As a consequence charge carriers are accelerated and generate more charge carriers through impact ionisation, causing the plasma channel to expand. Above a certain threshold voltage the plasma channel can expand through the entire device, causing a short-circuit. The formation of the plasma channel - called a streamer - takes around 200 ps.
- **Step 3: Self-heating in the plasma channel**
  Once the plasma channel is established a highly conductive path short circuits the device. While the plasma channel disappears after around 20 ns the self heating during this time can lead to a temperature rise that can exceed the melting temperature of silicon, resulting in the permanent destruction of the device.

A detailed description of the process leading to the destruction of a Si PiN diode and coupled electro-thermal device simulations of the process are presented by Weiß in [44]. Based on numerical simulations as well as experiments which confirm the results the following design parameters are identified by Weiß as having an influence on the failure probability in Silicon PiN diodes:

- The level of doping in the base material (n- layer)
- The width of the base area
- The design of the cathode (depth and level of doping)
- The field-stop layer
- The design of the anode

It is shown by Weiß [44] that the process leading to cosmic radiation induced failures of switching power devices such as IGBTs and metal oxide field effect transistors (MOSFETs) can be investigated using simulation methods similar to the one for the PiN diode.

A designer of a power electronic converter typically uses commercially available semiconductor devices and thus will not have the detailed information about the semiconductor chip's design that are necessary to undertake such simulations. Therefore, one has to rely on failure rate data provided by the device manufacturer or obtained through ones own measurements.

3.3.2. Failure rates for SEB in power semiconductors

Data for the SEB robustness of semiconductor devices is not included in device data-sheets. However, failure rates for some devices can be obtained from application notes (e.g. [30, 31]) and some results of measurements of device failure rates can be obtained from literature (e.g. [49–53]). Such literature data was used to plot the voltage dependent failure rate for a small set of semiconductors in Figure 3.6.

From the data one can see that each device has a certain threshold voltage below which the failure rate is so small that even in accelerated experiments no failures are observed. Once the voltage at which the first failure are observed is exceeded the failure rate increases exponentially with increasing voltage. One can also see that the SiC devices appear to be more robust when looking at this limited set of data, as most of the red data points are further on the right of the diagram.

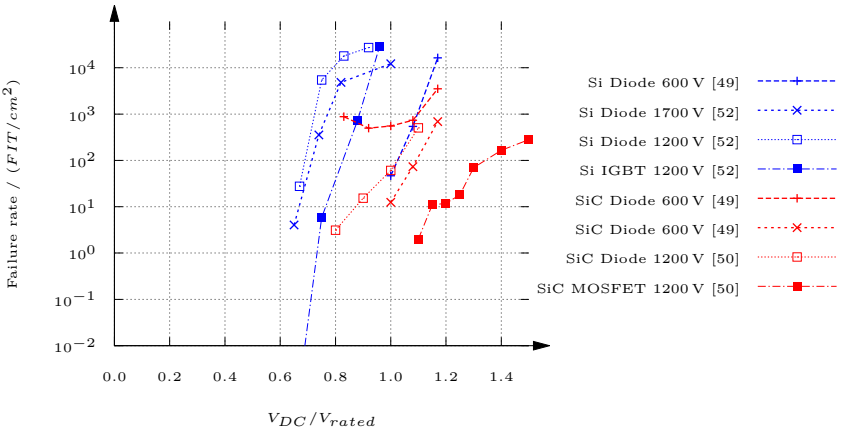


Figure 3.6.: Exemplary failure rates for Si (blue) and SiC (red) power semiconductors. (Source of data: [49, 50, 52])

However, as very little information is available about the tested devices and their characteristics, it is difficult to draw any conclusions from this information. In fact, in [54] it was shown that while 1200 V SiC Schottky diodes appear to be more robust than silicon (Si) diodes, the opposite was true for the tested 600 V devices. This highlights the need to perform measurements of the SEB failure rate of state of the art SiC diodes and MOSETs and to conduct detailed comparisons with state of the art Si devices.

3.3.3. Conclusion

A brief summary of the failure mechanism of single event burnout (SEB) as it is described in [44] was presented. It was mentioned that in [44] a numerical simulation method has been presented that enables investigations of a semiconductor's SEB robustness if detailed knowledge of the semiconductor design is available.

As a user of power semiconductors, the designer of a power electronic converter usually has limited knowledge of the internal structure of the available power semiconductors and can not conduct such numerical simulations. Yet, knowledge of the voltage dependent failure rate of the power semiconductors used in a design is essential to ensure that reliability criteria are met. Therefore, measurements of the SEB failure rate are required.

A look at SEB failure rate data for Si and SiC power semiconductors published in literature suggests that SiC devices may be more robust than Si components. To investigate whether this is the case for the devices available today, a testing campaign has to be conducted. In addition to the measurements of the voltage dependent failure rates due to SEB it is important to measure further device parameters such as the breakdown voltage in order to identify if differences that may be found can be attributed to the capabilities of the materials or whether they are a result of the way a particular device is designed.

3.4. Methodology for SEB failure rate measurements

In this section the experiment that was conducted to measure the failure rate of different power semiconductors due to cosmic radiation induced single-event-burnout is described. Initially, the neutron irradiation facility at the *The Svedberg Laboratory* in Uppsala, Sweden is introduced. Afterwards, a detailed description of the experimental set-up and the procedures that were followed to conduct the experiment is provided.

3.4.1. Neutron irradiation facility

Conducting measurements of the robustness of power semiconductors against cosmic radiation induced single-event-burnout is only feasible if the experiment is accelerated significantly, as it is necessary to measure very low failure rates in the region of 1 FIT. Carrying out such measurements without artificial increase of the stress (in this case the amount of neutrons passing through the devices under test) would take many years, even if a few thousand devices were tested at the same time. Therefore, a facility at which a large neutron flux is available is required to accelerate the experiment. Ideally, the spectrum of neutrons provided at such a facility should resemble the natural spectrum on the earth's surface (see Figure 3.1).

The experiments conducted in this study were performed during a one-week testing campaign at the ANITA facility at the *The Svedberg Laboratory* at the *Uppsala University* (Sweden). At this facility a cyclotron is used to accelerate protons to form a 180 MeV proton beam which is led to a tungsten target. From the nuclear reactions induced in the tungsten target by the protons the neutron beam is formed. At the standard-user-position 2.5 m from the tungsten target

a neutron beam with a circular cross-section with a diameter of up to 39 cm is available. [55]

In Figure 3.7 the neutron flux at the ANITA facility is plotted by computing the spectral neutron fluence per incident proton using information from [55] and multiplying with a factor corresponding to the used beam intensity[3]. The diagram shows that the neutron spectrum at the ANITA facility is comparable to the scaled reference spectrum up to around 150 MeV.

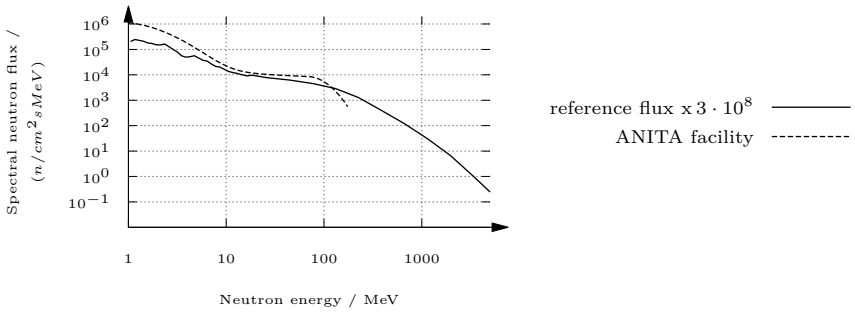


Figure 3.7.: Spectral neutron flux at ANITA facility computed from spectral neutron fluence per incident proton given in [55] multiplied by beam current compared to the reference terrestrial neutron flux given in [46] scaled by 3×10^8.

The maximum energy integrated flux available at the standard-user-position is approximately 1×10^6 n/cm^{2}s. Compared to the reference neutron flux at sea level (3.6×10^{-3} n/cm^{2}s [46]) this corresponds to an acceleration factor of approximately 2.8×10^8. Further information about the ANITA facility can be found in [55].

3.4.2. Experimental set-up

The experimental set-up was developed based on information in MIL-STD-750 test method 1080: 'Single-event burnout and single-event gate rupture' [56], descriptions of experimental set-ups in literature (e.g. [49, 50, 57–59]) and previous experience with SEB measurements that project partners within the project *HHK* have shared.

[3]Beam current of 215 nA or 1.34×10^{12} protons/s. Information kindly provided by email by Prof. Alexander Prokofiev, TSL, Uppsala University.

As described by Liu et. al. in [60] it is possible to perform SEB testing non-destructively by placing a load resistor in series with each DUT. However, to determine the appropriate value of the protection resistor knowledge of the voltage at which SEB is expected to occur and the level of SEB current are required. For the purpose of this investigation it was decided to perform destructive SEB testing to ensure that conditions are comparable to the actual application.

In order to be able to measure low failure rates within relatively short times and to enable the detection of at least 10 failures at each measuring point around 200 samples of a given semiconductor need to be exposed to the neutron beam and their status needs to be monitored. To quickly isolate failed devices each sample was connected to the high-voltage source using a fast-blowing 50 mA fuse as illustrated in Figure 3.8.

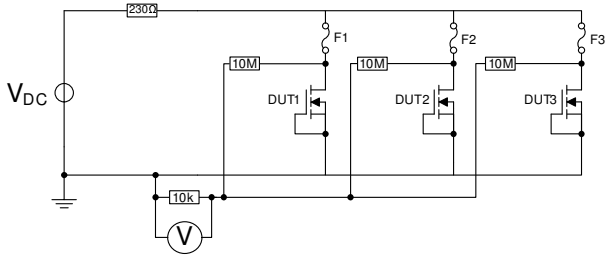


Figure 3.8.: Circuit to detect device failures for SEB failure rate measurement. Exemplary drawing for a group of three DUTs. In the experimental set-up each group had space for either 12 or 14 DUTs. (Principle circuit previously shown in [38])

To detect the status of each fuse and hence to monitor device failures, a high-voltage resistor is connected to each fuse. By measuring the voltage dropped across the 10 kΩ resistor the devices remaining active can be computed using Equation 3.1, where V_{meas} is the voltage measured across the 10 kΩ resistor, V_{DUT} is the DC-voltage applied to the devices-under-test and $R*$ and R_{meas} are the 10 MΩ and 10 kΩ resistances shown in Figure 3.8.

$$N_{DUT,intact} = \frac{V_{meas} \cdot R*}{R_{meas} \cdot (V_{DUT} - V_{meas})} \tag{3.1}$$

For the experiments, printed-circuit-boards as shown in Figure 3.9 were developed. Each such circuit board can accommodate a maximum of 52 DUTs on two smaller circuit-boards, which act as "carriers" for the DUTs. To monitor the status of the DUTs four groups of circuits as previously described (see Figure 3.8) are present on each main-board.

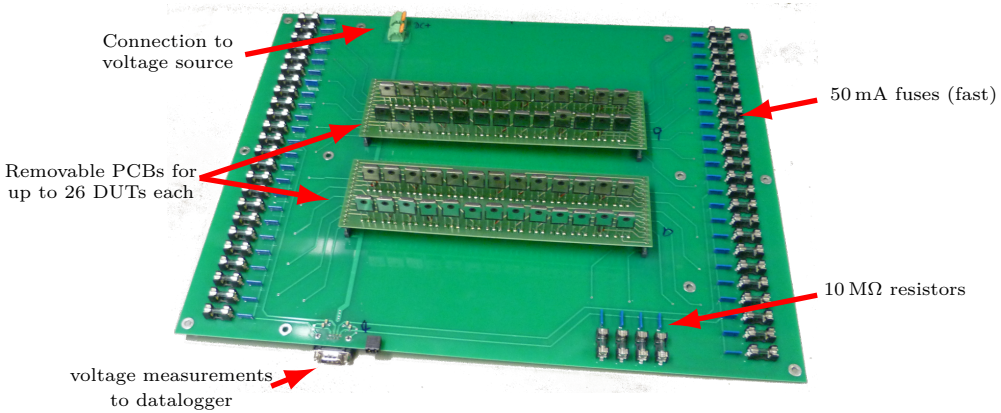


Figure 3.9.: Main printed-circuit-board for SEB testing. A maximum of 52 DUTs can be connected using two smaller printed circuit boards (PCBs) that are plugged into the main-board.

The DUTs are connected to the main PCB using smaller circuit-boards. This gives the flexibility to either use discrete devices or bare-die chips bonded onto test DCBs. Furthermore, by replacing the small circuit-boards and replacing the burned-out fuses on the main PCB the test set-up can be made ready for another experiment with different DUTs very quickly.

A total of four main boards were placed in parallel with a distance of 70 mm between each board. Depending on whether bare chips on ceramic substrates or discrete semiconductors in TO-247/TO-220 packages were tested the orientation of the set-up in the beam line was adapted to ensure that the maximum cross-sectional area of the chips was exposed to the beam. According to [57] irradiation from the front of the devices is the worst-case orientation.

The experimental set-up had to be controlled remotely via Ethernet connections. To enable this, a remote control solution for the used voltage sources was developed. A software program that allowed the entire experiment to be controlled through a single user interface was also developed. Using this program, the state of the DUTs was continuously monitored and the voltage applied to the DUTs was

controlled. All measured values were also recorded in a log file for later analysis. Additionally, safety shut-down features were implemented to protect the DUTs by turning off the voltage supply in case too many devices fail in a very short time. An overview of the experimental set-up is provided in Figure 3.10.

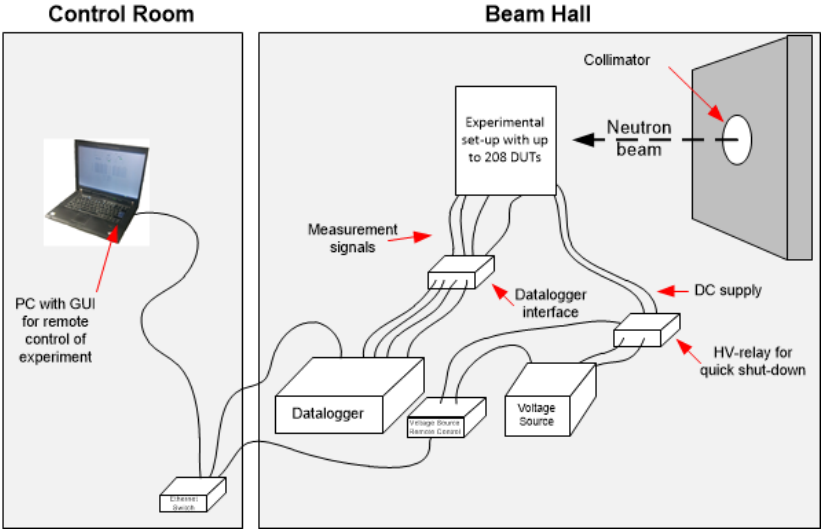


Figure 3.10.: Overview of experimental set-up.

3.4.3. Measurement procedure

Prior to starting the neutron flux through the DUTs the voltage applied to the DUTs was set and the number of DUTs detected by the remote control system as functional was recorded. A maximum neutron fluence ($\frac{n}{cm^2}$) was selected in the beam control system which would yield a test time of approximately 30 min. The beam was then activated until either the previously set fluence limit was reached or until 10 devices had failed. After turning off the beam the number of remaining DUTs was recorded and the voltage applied to the DUTs was adjusted for the next measuring point.

According to [9, p. 506] the estimate of the exponential distribution, which can be used to describe a random failure mode, is given as

$$\overline{\lambda} = \frac{k}{\sum_{i=1}^{k} t_i + (n-k) \cdot t_k} \tag{3.2}$$

where k is the number of observed failures, n is the number of samples at the start of the test, t_i is the time of the i-th failure and t_k is the time at which the experiment is stopped. The total dosage of neutrons (in n/cm^2) that passed through the DUTs from the time the experiment is started until its end is recorded along with the number of DUTs at the start of the test and the number of failures. The estimate of the failure rate was calculated using this information as

$$\overline{\lambda} = \frac{k}{k \cdot \frac{t_{k,eq}}{2} + (n-k)\, t_{k,eq}} \cdot 10^9 FIT \tag{3.3}$$

where n is the number of DUTs at the beginning of the irradiation, k is the number of devices that failed during the irradiation and $t_{k,eq}$ is the time it would take under non-accelerated conditions for the recorded dosage of neutrons to pass through the test set-up, which is calculated as

$$t_{k,eq} = \frac{neutron\,dosage}{ref.\,neutron\,flux} = \frac{neutron\,dosage}{12.96} \cdot \frac{(n/cm^2)}{(n/cm^2 h)} \tag{3.4}$$

where the reference neutron flux of 12.96 n/cm^{2}h corresponds to the flux at the reference location (New York City) [46]. For each measurement the confidence interval was computed for a confidence level of 95 % based on the number of observed failures n according to the equations in [9, p.512]. The confidence intervals are shown as error bars in the diagrams in the results section.

3.5. Devices under test

A total of ten devices were tested for their SEB robustness. The tested devices are listed in Table 3.1 along with their nominal voltage and the measured breakdown voltage at room temperature.

Table 3.1.: Important metrics of the semiconductors tested in this study.

Identifier	V_{nom} / V	Device type	V_{bd} [a] / V
Si-MOSFET-A	600	SJ MOSFET (Si)	679
SiC-MOSFET-A	650	Trench MOSFET (SiC)	1151
Si-IGBT-A	1200	IGBT (Si)	1361
Si-IGBT-B	1200	IGBT (Si)	1349
SiC-MOSFET-B	1200	Trench MOSFET (SiC)	1642
SiC-Diode-A	1200	Diode (SiC)	1422
Si-Diode-A	1200	CAL Diode (Si)	1421
Si-IGBT-D	1700	IGBT (Si) Trench+FS	2161
SiC-MOSFET-C	1700	D-MOSFET (SiC)	2650
Si-Diode-B	1700	CAL Diode (Si)	1887

[a] Measured at room temperature on three devices of each type (mean)

3.6. Experimental results

The failure rates obtained through measurements are provided in the following figures. To aid comparison between the different devices the failure rates were normalised to the chip size.

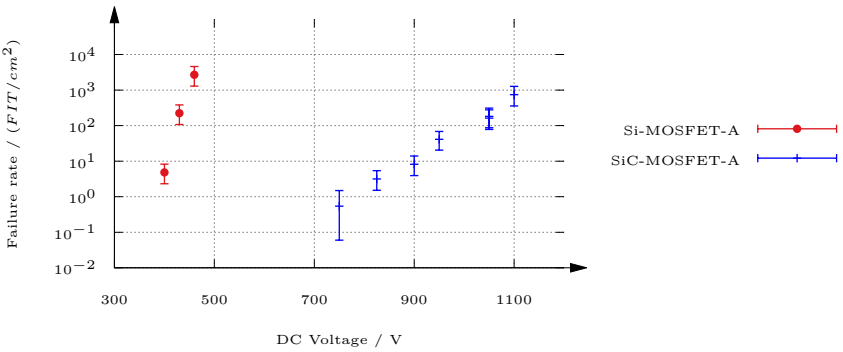


Figure 3.11.: Measured failure rates for 600 V semiconductor switches at sea level and room temperature, normalised to chip area. (data previously shown: [38])

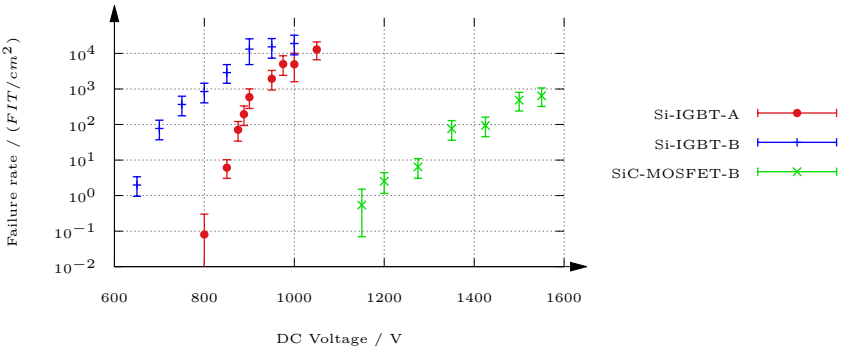


Figure 3.12.: Measured failure rates for 1200 V semiconductor switches at sea level and room temperature, normalised to chip area. (data previously shown: [38])

The above results show that in the 600 V as well as in the 1200 V class the robustness of the SiC devices is much higher than that of the tested Si transistors. For the application this means that SiC-MOSFET-A can be operated at its rated voltage of 650 V without expecting failures. For SiC-MOSFET-B a very low failure rate is to be expected at the rated voltages of 1200 V and at 1000 V no failures have to be expected.

To explore whether the reason of the increased robustness can be attributed to the observed high breakdown voltages of the SiC devices the failure rates were plotted again in Figure 3.13 with the horizontal axis rescaled to the ratio of the applied voltage to the measured breakdown voltage of the devices.

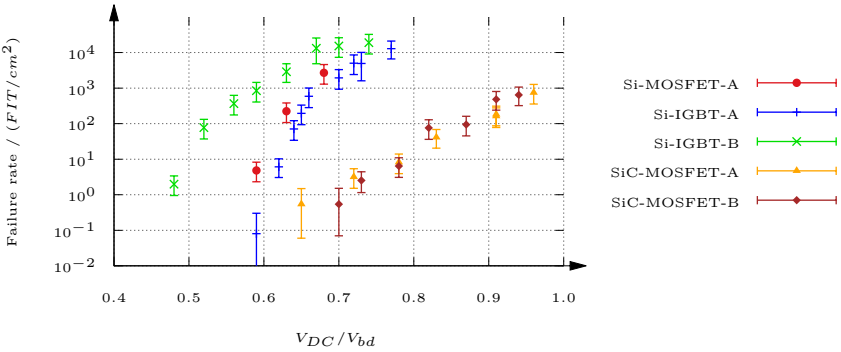


Figure 3.13.: Measured failure rates for 650 V and 1200 V semiconductor switches at sea level and room temperature, normalised to chip area and actual breakdown voltage of the devices. (data previously shown: [38])

The data in Figure 3.13 shows that the relative voltage at which the tested SiC devices start showing the first failures is only slightly higher than for the robust Si devices. Therefore, at least part of the robustness exhibited by the SiC devices has to be attributed to the high breakdown voltages of these devices. Nevertheless, the slope at which the failure rate for the SiC devices increases with higher voltage is much shallower than in the case of Si devices, showing that the tested SiC devices appear to be more robust, even when removing the advantage of the very high breakdown voltage through the normalisation. This suggests, that from the point of view of the SEB robustness less de-rating may be required for SiC devices than for Si switches, even if the breakdown voltage is reduced by the manufacturers in the future.

The measured failure rates for a 1700 V Si IGBT and a SiC MOSFET of the same voltage rating are shown in Figure 3.14.

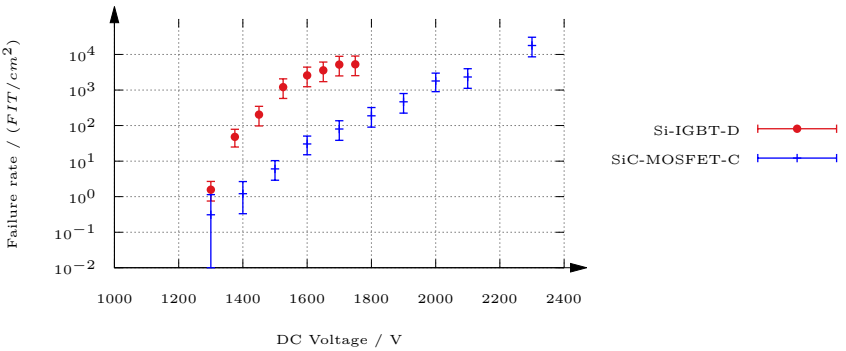


Figure 3.14.: Measured failure rates for 1700 V semiconductor switches at sea level and room temperature, normalised to chip area. (data previously shown: [38])

The results show that both tested 1700 V devices start to show failures at around 1300 V, but the failure rate increases faster for the Si device than for the SiC device as the voltage is increased. In Figure 3.15 the results are plotted normalised to the actual breakdown voltage of the devices.

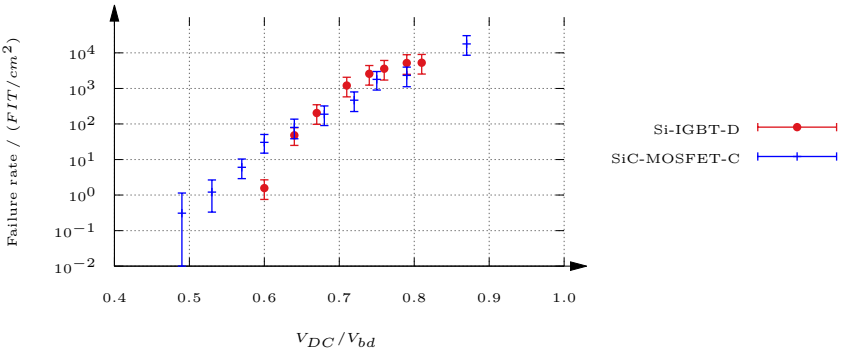


Figure 3.15.: Measured failure rates for 1700 V semiconductor switches at sea level and room temperature, normalised to chip area and actual breakdown voltage of the devices. (data previously shown: [38])

As can be seen from Figure 3.15 the SiC MOSFET starts to show failures at just below 50 % of the blocking voltage. This is significantly different from the result observed for the 650 V and 1200 V SiC MOSETs (compare Figure 3.13 and Figure 3.15).

Use of the 1700 V SiC device in a 2-level photovoltaic inverter specified for a maximum open-circuit DC voltage of 1500 V appears to be possible, if the operating time at high voltages is sufficiently low. The maximum expected failure rate remains at less than 10 FIT/cm^2 at 1500 V, which is two orders of magnitude lower than the value for the tested Si IGBT. Hence, only very few failures will occur in the application if the operating time at high voltages is low.

The results for the tested diodes are shown in Figure 3.16 and Figure 3.17. Literature data from [52] for two state of the art silicon diodes is included in the plots for comparison purposes.

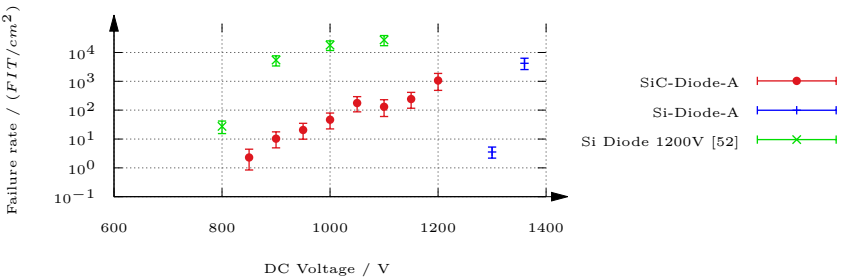


Figure 3.16.: Measured failure rates for 1200 V diodes at sea level and room temperature, normalised to chip area. Failure rates for a standard Si diode from [52] is shown for reference. (data previously shown: [38])

It can be seen that the SiC diode starts to show failures at a slightly higher voltage than typical Si diodes and that the failure rate increases slower for the SiC diode. Therefore, the SiC diode is more robust than the state of the art Si diode it was compared with. The tested controlled axial lifetime (CAL) diodes (Si-Diode-A and Si-Diode-B) are even more robust. Failures can only be observed above 85 % of the nominal voltage for the 1700 V type and no failures can be observed for the 1200 V device below its rated voltage.

In a final test the experimental set-up was placed in an insulated metal enclosure as shown in Figure 3.18 and the inside temperature was adjusted to 100 °C before measurements were conducted on Si-IGBT-A. It has to be noted that the

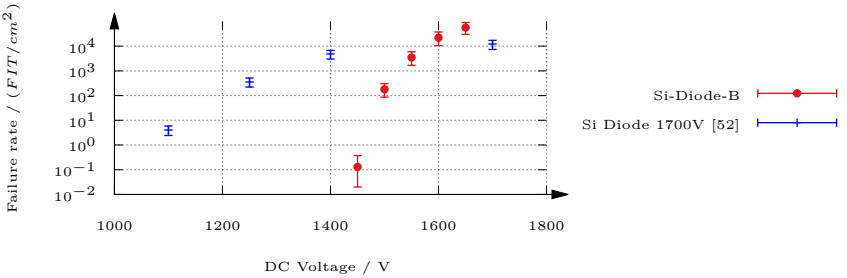
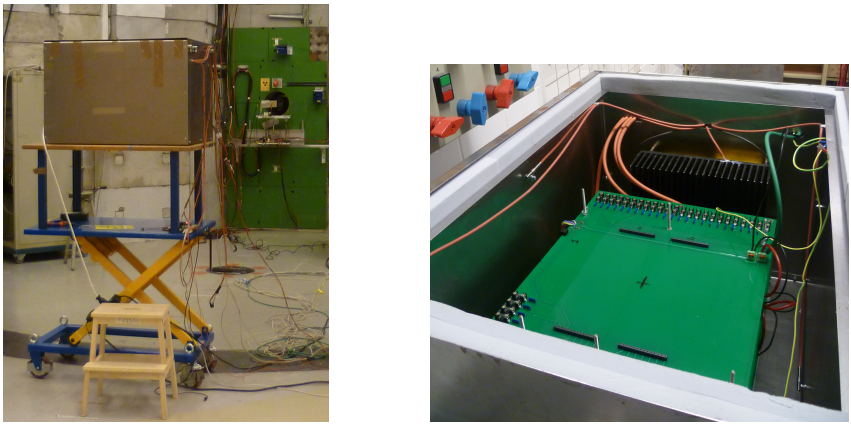


Figure 3.17.: Measured failure rates for 1700 V diodes at sea level and room temperature, normalised to chip area. Failure rates for a standard Si diode from [52] is shown for reference. (data previously shown: [38])

beam intensity measurement for this test was not recalibrated to account for the shielding of the 3 mm steel and approximately 40 mm of insulating foam that made up the wall of the thermal chamber.



(a) Thermal chamber in beam line

(b) View into thermal chamber

Figure 3.18.: Experimental set-up within a purpose built thermal chamber that was used to heat the DUTs to 100 °C while placed in the beam-line.

In Figure 3.19 the measurement results for Si-IGBT-A are shown for room temperature and the elevated temperature. It can be seen, that the failure rate

at increased temperature is reduced significantly. This result agrees with the information given in [30, 31]

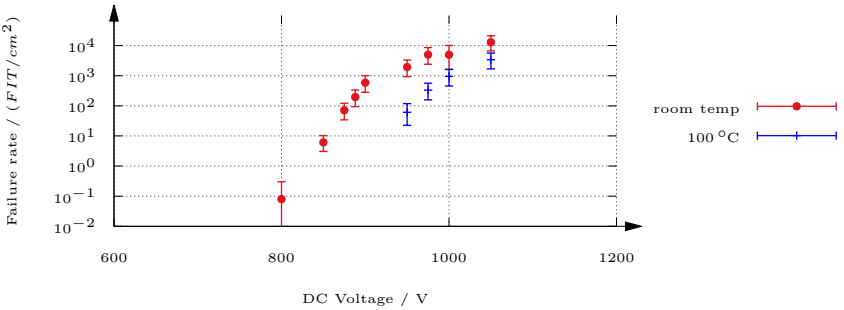


Figure 3.19.: Measured failure rates for Si-IGBT-A at room temperature and at 100 °C at sea level, normalised to chip area (measurement at 100 °C not recalibrated to account for shielding of thermal chamber).

To investigate the reason for the temperature dependency the failure rates is plotted in the following figure with the voltage normalised to the measured breakdown voltage at the different temperatures.

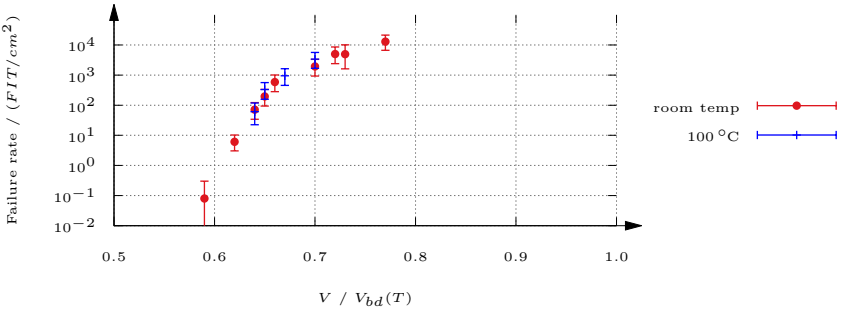


Figure 3.20.: Measured failure rates for Si-IGBT-A at room temperature and at 100 °C at sea level, normalised to chip area and normalised to the measured breakdown voltage at the different temperatures (V_{bd} @ room temp = 1361 V, V_{bd} @ 100 °C = 1491 V, measurement at 100 °C not recalibrated to account for shielding of thermal chamber).

In the plot in Figure 3.20 it is no longer possible to determine a difference between the failure rate measurements at the two temperatures. This supports the conclusion that the increased robustness at 100 °C is a consequence of the higher breakdown voltage of the device than at room temperature.

3.7. Comparison of results with data from literature

Since some of the tested devices have previously been tested at other facilities by different researches it was possible to compare the measured results to the data available from literature [50, 52].

The 1200 V SiC diode that was tested in this study has already been evaluated for robustness against SEB by Asai et.al. [50] at the Research Center for Nuclear Physics (RCNP) in Japan, where a neutron source with a spectrum similar to the terrestrial spectrum in the range of 5 to 300 MeV is available.

In [52] failure rates for 1200 V and 1700 V CAL diodes are presented. The measurements were conducted at the Paul-Scherrer-Institute in Villigen, Switzerland using a mono-energetic proton beam with an energy of 200 MeV.

A comparison of the measurements conducted in this study with the data from [50] and [52] is provided in Figure 3.21.

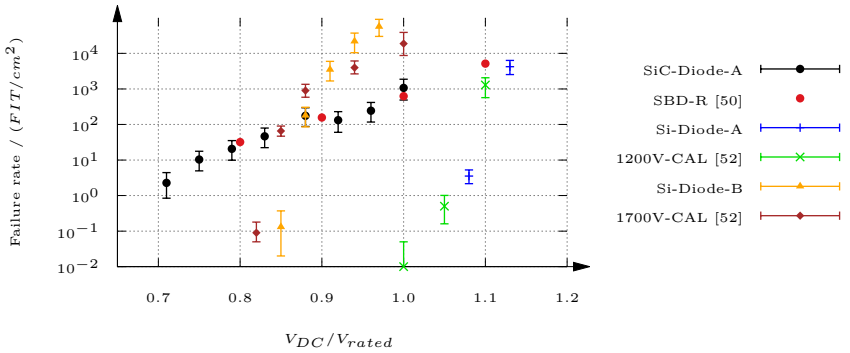


Figure 3.21.: Measured failure rates for diodes compared to data from [50] and [52] (comparison of data previously shown: [38])

The comparison shows very good agreement between the measurements conducted by Asai et.al. (SBD-R) and the measurements conducted on SiC-Diode-A during the campaign at the TSL.

A slight disagreement between the measurements and the data of Scheuermann and Schilling [52] can be observed for the 1700 V CAL diode. In the investigation presented here the first failures were observed at slightly higher voltages and the failure rates observed at high voltages are higher than those measured by Scheuermann and Schilling. For the 1200 V device a comparison of the results is difficult to make, as only very few data points are available.

Overall, the comparison shows very similar results for the two different measurements, but a small disagreement does exist, which can maybe be attributed to the different types of particle beam used (i.e. mono-energetic protons with 200 MeV vs. wide spectrum neutrons of up to 150 MeV).

3.8. Long-term experiment for result validation

To perform a validation of the experimental results of the accelerated measurements a long-term test was set up in the lab. A constant DC voltage of 1100 V was applied to 26 samples of Si-IGBT-A and 70 samples of Si-IGBT-B that were left over from the experiments conducted at the The-Svedberg-Laboratory. The long-term experiment was performed between November 2015 and October 2016. The experiment was stopped a total of five times due to faults of the test experiments and to allow for downtime during holiday periods. Overall, the voltage was applied to the devices for 4572 h.

A total of six failures were observed for Si-IGBT-B and one of the samples of Si-IGBT-A failed during the test time. The failures are distributed over time as shown in the following table.

Table 3.2.: Observed failures during long-term experiment. Applied DC voltage: 1100 V, overall experiment duration: 4572.1 h.

failure number i	**time of i-th failure t_i**
1	4406.4 h

(a) Si-IGBT-A

failure number i	**time of i-th failure t_i**
1	1617.2 h
2	1921.1 h
3	2063.0 h
4	2862.4 h
5	4313.8 h
6	4446.0 h

(b) Si-IGBT-B

Based on the measurement results the failure rates were calculated using equation 3.2. The failure rates are plotted in Figure 3.22 to compare them with the accelerated measurements conducted at the ANITA facility. The measurement results of the accelerated measurement at 1100 V were discarded from the results presented in previous sections of this chapter as the failures at these voltages occurred very rapidly (10 failures in less than 60 s) and as a result the DC voltage applied to the DUTs was not stable. They are shown here only for comparison with the long term measurement and should not be relied upon.

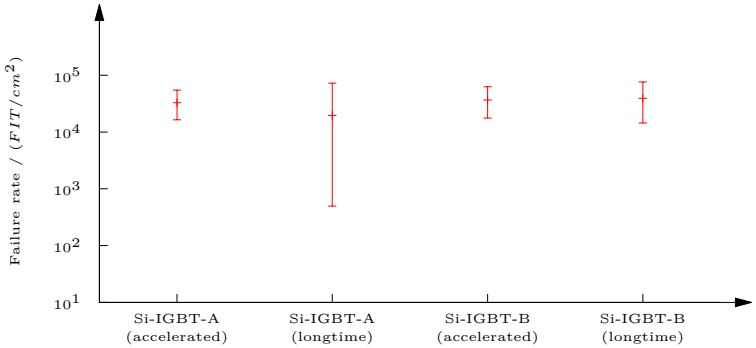


Figure 3.22.: Comparison of failure rates observed failures during long-term experiment and measurements at ANITA facility at $V_{DC} = 1100\,\mathrm{V}$. The measurement data of the accelerated measurement was originally discarded because failures occurred too fast for accurate measurement. Overall duration of long-term measurement: 4572.1 h.

Due to the limited number of observed failures in the long-term experiment for Si-IGBT-A the comparison with the accelerated measurement run is of limited value. However, the comparison for Si-IGBT-B is more valuable as a larger number of failures were observed. The comparison shows that the long term measurements agree with the accelerated measurements.

3.9. Conclusion

A measurement campaign to determine the robustness of ten power semiconductor devices against single-event-burnout due to terrestrial cosmic radiation was conducted at the ANITA facility of the The Svedberg Laboratory at Uppsala University in Uppsala, Sweden.

The results show that the tested SiC MOSFETs in all three voltage classes that were investigated (600 , 1200 and 1700 V) are more robust than the tested Si IGBTs and Si SJ MOSFETs. The increased robustness allows use of the 1200 V SiC MOSFET in a photovoltaic inverter specified at a maximum voltage of 1000 V without having to expect any failures due to SEB. Similarly, the tested 1700 V SiC MOSFET can be operated in a 1500 V system provided that the operating

hours at voltages above 1400 V are limited and that the maximum expected failure rate of 10 FIT/cm^2 at 1500 V can be tolerated.

Additionally, the results show that the tested 1200 V SiC Schottky diode is more robust than state of the art silicon diodes (data from [52]). The measurements have also shown that Semikron CAL diodes have even higher robustness against SEB than the tested SiC device.

The results were further analysed to identify if part of the robustness of the SiC devices is a consequence of the high breakdown voltage that these devices have in relation to their nominal voltage. The analysis has confirmed that the robustness of the SiC devices has to be attributed in part to the high breakdown voltages of the tested SiC MOSFETs.

The analysis of the result for the 1700 V SiC MOSFET shows a significant difference to the SiC MOSFETs with 650 and 1200 V rating. If the failure rates are normalised to the actual breakdown voltage of the devices it can be observed that the 1700 V SiC MOSFET, which has a planar structure, starts to fail at around 50 % of its breakdown voltage. The 650 and 1200 V SiC MOSFETs, which have a trench structure, start to fail at approximately 65 % to 70 % of their breakdown voltage and the failure rate increases slower than for the tested Si devices in the same voltage classes. This suggest that maybe the design of the 1700 V SiC MOSFET is not optimised for SEB robustness. However, as the breakdown voltage of this particular device is very high, the device remains robust at normal operating voltages. More detail about the device designs would be needed to explore the reasons for the difference in robustness, but it is interesting to note that apparently the tested trench SiC MOSFETs are more robust in this comparison than the tested planar SiC MOSFET.

It is expected that future SiC MOSFETs will be designed with less margin in their breakdown-voltage to fully exploit the technological opportunities in terms of on-state losses. As a consequence the robustness of future generations of SiC MOSFETs against cosmic radiation induced single event burnout may be lower than of the devices that were available for this investigation. Therefore, it is advisable to conduct measurements of the SEB failure rate once new device generations are available.

The measurement of the failure rate of Si-IGBT-A at an elevated temperature of 100 °C has shown that the failure rate of state of the art silicon devices reduces with increasing temperature, which is in agreement with data available in [30, 31]. Analysis of the measurement results has suggested that the increasing breakdown voltage at higher temperature may be the reason for the observed increase in

robustness as temperature was increased. However, more work is required to validate this, as only one device type was measured at two temperatures in this study and the measurement of the beam intensity was not recalibrated for the shielding effect of the thermal enclosure for the measurement at 100 °C. For future investigations it is also suggested to investigate the temperature dependency of the failure rate due to SEB for SiC devices.

To enable more accurate predictions of the failure rate in an application it is advisable to conduct future measurements at the chip temperatures that are expected in the application. Otherwise, if failure rates are only measured at temperatures significantly lower than in the application the failure rate predictions based on such data may result in pessimistic failure rate estimations.

The accelerated measurement results for two DUTs were compared with results obtained during a long-term measurement run. The long-term experiment confirms the results that were obtained during the accelerated conditions.

Finally, the measurement results obtained for three devices were compared with results recently published by other researchers. The comparison has shown very good agreement with results obtained by Asai et.al. [50] at the neutron source at RCNP which provides a spectrum similar to that available at the ANITA facility at the The-Svedberg-Laboratory. Results of the measurements conducted by Scheuerman and Schilling. [52] using mono-energetic protons instead of neutrons with a wide spectrum of energies show some deviations but are otherwise very similar to the results obtained during the experiments at the TSL.

Overall, the good agreement with results obtained by other researches and the agreement between the measurements under accelerated and non-accelerated conditions gives confidence that the methodology yields reproducible results.

4. Lifetime and reliability of IGBT modules in PV central inverters

4.1. Introduction

Power semiconductors are the central components of any power electronic converter system. In large power converters such as the central inverters used in large scale photovoltaic installations power semiconductors modules are commonly used. The lifetime and reliability of these power semiconductor modules is affected by a number of failure mechanisms as was shown in Chapter 2.

The objective of the investigation presented in this chapter is to determine whether the power semiconductor modules in photovoltaic central inverters can withstand the stresses in sunbelt regions for a lifetime of 25 years and if an acceptable failure rate can be expected. For that purpose the stresses applied to the power semiconductor modules in photovoltaic inverters installed in sunbelt regions are investigated.

This investigation is an extension of the author's work that was done as part of the research project *GigaPV*[1]. Results of the investigation of the thermal stresses carried out as part of the project *GigaPV* were previously presented in [61]. For the work shown in this chapter the simulation was extended to include the photovoltaic system in order to be able to investigate effects of the system set-up (size / type of photovoltaic generator). Also, changes were made to the look-up-tables for the semiconductor losses and the way the fan-speed is adjusted in the simulation was changed. Furthermore, the voltage stress on the semiconductors is analysed in this work and compared to the measured voltage dependent failure rates of typical semiconductors presented in Chapter 3. Results of the analysis of the voltage stress on power semiconductors in PV central inverters were previously presented in [62].

[1] Joint research project funded by the German Federal Ministry of Education and Research

In the first section of this chapter the simulation structure and the models that were utilised to describe the behaviour of the different components of the photovoltaic system are presented. Afterwards, the methodology that was used to analyse the simulation outputs in order to estimate the lifetime and reliability of the power semiconductors is shown. Finally, the scenarios investigated in this study are introduced and the results are presented.

4.2. Photovoltaic system simulation

In order to quantify the stresses on the power semiconductor modules in a photovoltaic central inverter it is necessary to derive a mission profile for the inverter from climatic data and to infer the stresses on the semiconductor modules from that mission profile. For that purpose a simulation was developed using Matlab/Simulink. In this section the simulated system is introduced and details of the models that were used in putting together the simulation are described.

4.2.1. Topology of the investigated photovoltaic system

The system topology of the photovoltaic power plant simulated in this investigation is shown in Figure 4.1. It was assumed that a photovoltaic central inverter is connected to one large photovoltaic generator. The low-voltage output of the inverter is stepped up by a transformer to the medium-voltage range to enable the interconnection to the public grid.

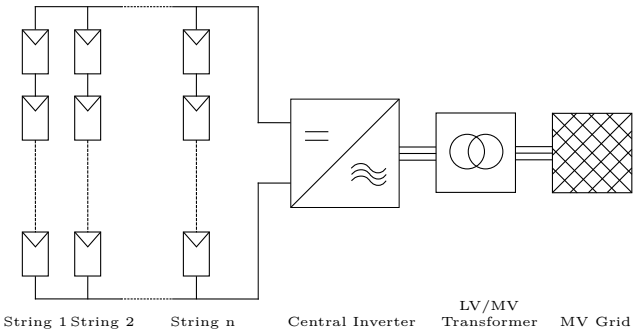


Figure 4.1.: Overview of the photovoltaic system considered in this investigation.

Photovoltaic generators for large scale photovoltaic power plants are comprised of a large number of individual photovoltaic modules. The modules are connected in series to form strings that reach the desired DC voltage. The strings are paralleled to obtain the required power rating.

Typically, the string-length is chosen to ensure that the maximum open-circuit output voltage of the photovoltaic generator reaches no more than 1000 V for the coldest expected conditions, which is the maximum tolerable input voltage specified for many inverters. In the future, systems with maximum generator voltages of 1500 V are expected to become the norm [63, 64], as the increase in system voltage reduces the overall system cost. Inverters designed specifically for 1500 V systems are available today [11, 65].

The output power of typical photovoltaic central inverters lies in the range of 1 MW to 3 MW. Multiple strings are combined in parallel to combine their output current and thus match the power rating of the photovoltaic generator. For system optimisation it is often desirable that the photovoltaic generator can be sized for a nominal power of up to 50 % higher than that of the inverter.

4.2.2. Overview of photovoltaic system simulation

The components of the system shown in Figure 4.1 were modelled and the individual models combined to create a single simulation of the entire system. A top level overview of the simulation is presented in Figure 4.2.

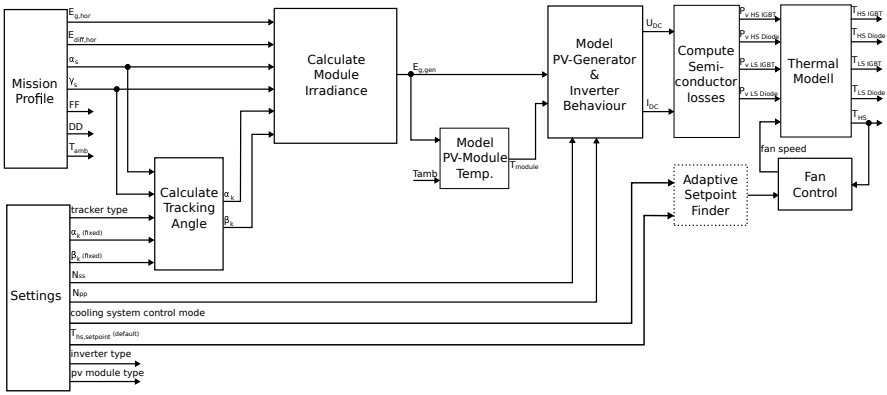


Figure 4.2.: Overview of the photovoltaic system simulation.

The inputs to the simulation are the mission profile and the simulation settings. The mission profile consists of the climatic conditions (i.e. solar irradiance, ambient temperature) at the investigated location for a certain time period which typically is one year with a time resolution in the range of 15 s to 1 min. The simulation settings relate to the set-up and size of photovoltaic generator (i.e. module tilt / orientation, type of tracking, size-ratio) and are summarised in Table 4.1 along with the possible values that the parameters may take. Additionally, the type of inverter and photovoltaic modules are provided as inputs to enable parameters for their models to be loaded from configuration files.

Table 4.1.: Parameters for simulation of photovoltaic system

Parameter	Description	Range of values
$SR = \frac{P_{gen,stc}}{P_{inv,ac-nom}}$	Size ratio of power of photovoltaic generator to nominal inverter power	1.0 to 1.5
$Type_{tracking}$	Type of photovoltaic generator	fixed, elevation-tracker, azimuth-tracker, 2-axis-tracker
α_{gen}	PV module azimuth	0 to 360°
β_{gen}	PV module inclination	0 to 90°

Using these inputs and the data loaded for the inverter and photovoltaic modules the simulation computes the number of photovoltaic modules that are connected in series in each string, N_{ss} and the number of strings that are connected in parallel, N_{pp} to form the photovoltaic generator. The value for N_{ss} is found by computing the open circuit voltage of the selected PV module type at the coldest expected temperature.

For the purpose of this investigation the coldest value recorded for a given mission profile is used as the worst-case temperature. The string-length is then fixed to the maximum permissible value that does not violate the maximum DC open-circuit voltage for a selected inverter. The number of strings connected in parallel is computed by dividing the desired power of the photovoltaic generator by the total power of each string.

Once all the configurations are loaded and the preliminary computations are completed the simulation is started. In the following section details of the models

used to determine the solar irradiation on the photovoltaic modules and their temperature as well as the model used to describe their electrical behaviour are provided. Afterwards, the behavioural model that was used to describe the electrical behaviour of the inverter is discussed and details for the electro thermal model used to determine the thermal stress on the semiconductors are provided.

4.2.3. Simulation of photovoltaic generator

The electrical behaviour of the photovoltaic generator depends primarily on the solar irradiation on the photovoltaic modules as well as their temperature. Therefore, it is necessary to compute the solar irradiance on the photovoltaic panels and model their temperature. The methodology described by Quaschning in [66, 67] was followed to estimate the irradiance on the photovoltaic modules. Shading effects were neglected in this investigation as it was assumed that large photovoltaic power plants are set-up to avoid shading issues.

Solar irradiance on horizontal surfaces

The total solar irradiance on a horizontal plane $E_{G,hor}$ is comprised of the direct $E_{dir,hor}$ and diffuse $E_{diff,hor}$ components:

$$E_{G,hor} = E_{dir,hor} + E_{diff,hor} \tag{4.1}$$

In this study solar irradiance data already broken down into the direct and diffuse components was used. If data that does not break down the solar irradiance into direct and diffuse components is to be used with the simulation the indirect component of the global irradiance can be determined using the following two equations, reproduced by Quaschning [67, p. 100] from the work of Reindl, Beckman and Duffie [68].

$$k_T = \frac{E_{G,hor}}{E_{0,hor} \cdot sin\gamma_s} \tag{4.2}$$

$$E_{diff,hor} = \begin{cases} E_{G,hor} \cdot (1.020 - 0.254 \cdot k_T + 0.0123 \cdot sin\gamma_s), k \leq 0.3 \\ E_{G,hor} \cdot (1.400 - 1.749 \cdot k_T + 0.177 \cdot sin\gamma_s), 0.3 < k_T \leq 0.78 \\ E_{G,hor} \cdot (0.486 - 0.182 \cdot sin\gamma_s), k \geq 0.78 \end{cases} \tag{4.3}$$

The constant $E_{0,hor}$ is the solar constant which equates to 1367 W/m^2 [67, p. 99] and γ_s is the sun elevation, as described in the following section.

Calculation of sun position and incidence angle

Photovoltaic modules are mounted at a certain inclination β_{gen} in order to maximise the energy yield and allow dirt to be washed off by rainfall [67, pp. 100-101]. To be able to calculate the solar irradiance on a tilted photovoltaic module from the solar irradiance on a horizontal plane the sun position and the angle of incidence of the direct irradiance on the module surface need to be known.

The sun position can be described by the sun azimuth α_s and the sun elevation γ_s as illustrated in Figure 4.3 and depends on the geographical location as well as on the date and time. For the purpose of this investigation the algorithm described in DIN 5034 [69] was implemented to calculate the sun position.

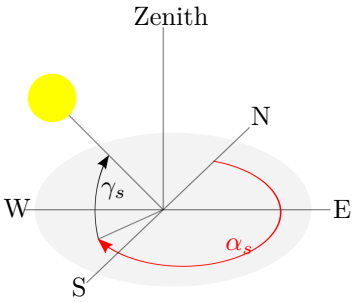


Figure 4.3.: Description of sun position according to DIN 5043 [69], also see [66, 67].

In Figure 4.4 the angles defining the module inclination β_{gen} and the module azimuth α_{gen} are illustrated. For this investigation the module azimuth is defined as the direction that the active surface of the module faces. A south facing module thus has an azimuth of $\alpha_{gen} = 180°$. This differs from the definition used in [66, 67], but was used here because the author considers this to be more intuitive.

From the module orientation and the sun elevation and azimuth the incidence angle θ_{gen} between the normal of the photovoltaic module and the vector to the sun can be calculated according to an equation given by Quaschning [67, p. 99]

which was adapted to account for the different definition of the module azimuth used in this investigation:

$$\theta_{gen} = arccos(cos\gamma_s \cdot sin\beta_{gen} \cdot cos(\alpha_s - \alpha_{gen}) + sin\gamma_s \cdot cos\beta_{gen}) \tag{4.4}$$

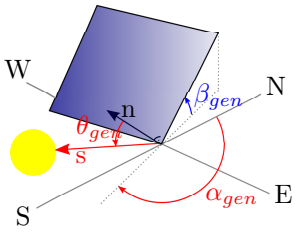


Figure 4.4.: Photovoltaic module orientation. (see [67, p.98][66], α_{gen} defined differently)

Insolation on tilted photovoltaic module

The total solar irradiance on an inclined panel $E_{G,gen}$ is comprised of three parts, the direct irradiance $E_{dir,gen}$, the diffuse irradiance $E_{diff,gen}$ and the irradiance reflected from the ground in front of the panel $E_{refl,gen}$ [67, p. 101].

$$E_{G,gen} = E_{dir,gen} + E_{diff,gen} + E_{refl,gen} \tag{4.5}$$

The direct irradiance on the tilted surface can be calculated using the incidence angle θ_{gen} and the sun elevation γ_s [67, p. 101].

$$E_{dir,gen} = E_{dir,hor} \cdot max\left(0, \frac{cos\theta_{gen}}{sin\gamma_s}\right) \tag{4.6}$$

The radiation reflected from the area in front of the panel can be expressed by

$$E_{refl,gen} = E_{G,hor} \cdot A \cdot \frac{1}{2} \cdot (1 - cos\beta_{gen}) \tag{4.7}$$

where A is the Albedo coefficient, which expresses the reflectivity of the area in front of the panel [67, p. 101]. Since Albedo coefficients for the investigated

locations were not available a value of $A = 0.2$ was used, as suggested in [67, p. 102].

A number of models for the diffuse irradiation on an inclined surface exist. An overview of different models is provided in [70] and [67, pp. 102-103]. For the purpose of this study the Perez-model [71–73] in the version presented in [73] and described by Quaschning in [66, 67] was used. The model incorporates the anisotropic nature of the diffuse solar irradiance and is considered to be very accurate [67, 70]. The equations and coefficients of the model that were used to compute the diffuse irradiance are included in Appendix A.

Computation of tracking angles

Tracking systems for photovoltaic systems can be controlled in two ways as described by Märtel [74]. One option is to calculate the elevation and/or azimuth angle of the sun and point the photovoltaic modules in that direction to maximise the direct irradiance on the modules. Alternatively, a closed loop control system can vary the tracking angle in order to determine the azimuth and/or elevation angle that results in the maximum energy harvest. Such a control system can particularly be suitable in locations where significant cloud cover is to be expected regularly [74].

For the purpose of this investigation the first method was used. The sun elevation γ_s and azimuth α_s calculated using the method described in DIN 5034 [69] were used to determine the expected optimal module tilt and elevation angles.

This approach was selected to avoid the need for a closed loop controller or an iterative approach to find the optimum module orientation at every step in time to maximise the simulation speed. Also, the risk of introducing errors into the simulation, e.g. if a controller or search algorithm incorrectly selects a local but not global optimum, were avoided.

Model of thermal behaviour of photovoltaic modules

The temperature of a photovoltaic module has an influence on the voltage/current characteristic of the module. Therefore, the actual temperature that is expected in the application should be considered.

An approximated cell temperature can be obtained using the normal operating cell temperature (NOCT) provided in the data-sheet of photovoltaic modules.

The NOCT is defined as the temperature of the cells if the module is in open-circuit condition, exposed to a solar irradiance of $800\,\mathrm{W\,m^{-2}}$ and at an ambient temperature of 20 °C and a wind speed of $1\,\mathrm{m\,s^{-1}}$ [75]. The temperature of a module in open-circuit condition can be calculated as

$$T_{module} = T_{amb} + E_{G,gen} \cdot \frac{T_{NOCT} - 20^{\circ}}{800} \tag{4.8}$$

where $E_{G,gen}$ is the irradiance on the module, T_{amb} is the ambient temperature and T_{NOCT} is the normal operating cell temperature as given in the module data-sheet [75]. In most cases the photovoltaic module is not operated in open-circuit condition, but at the maximum power point (MPP). The above equation is modified to account for the power extracted from the module to give the following equation for the temperature while operating at the MPP [76].

$$T_{module} = T_{amb} + E_{G,gen} \cdot \frac{T_{NOCT} - 20^{\circ}C}{800 \cdot (1 + \eta_{MPP})} \tag{4.9}$$

In this equation $E_{G,gen}$ is the irradiance on the module, T_{amb} is the ambient temperature, T_{NOCT} is the normal-operating-cell-temperature and η_{MPP} is the module efficiency at the maximum power point [76].

The main limitation of using the NOCT to estimate the module temperature is that the actual wind speed at a given location may be significantly different than the $1\,\mathrm{m\,s^{-1}}$ that the NOCT is defined at. In the literature different models for the module temperature that take into consideration the wind speed are discussed (e.g. [75, 77]). A balance of energy approach is usually used to compute the temperature based on the energy absorbed from the sun, the energy converted to electricity and the energy dissipated as heat to the environment. This approach requires knowledge off the heat transfer coefficient between the photovoltaic module and the surrounding air, which depends on the wind-speed as well as the way of mounting the modules.

Measured photovoltaic module temperature data was not available for this investigation. Also, it was expected that the way in which modules are mounted will have a significant influence on the heat transfer coefficient. It would not have been possible to verify if the models suggested in the literature along with the proposed heat transfer coefficients are applicable to the selected photovoltaic modules and the most likely mounting solution. Therefore, it was decided to compute the module temperature using the simple approximation based on the

NOCT, even though the effect of changing wind speeds is not reflected in this calculation.

For very similar reasons (i.e. the lack of models or data that a model could be derived from) the thermal capacitance of the photovoltaic modules was also neglected in this investigation.

Model of electrical behaviour of photovoltaic generator

The basic building block of any photovoltaic generator is an individual photovoltaic module. Such a photovoltaic module in turn is made up of a number of photovoltaic cells. Different electrical circuits as described by Quaschning [66, pp.190-195] can be used to describe the behaviour of a photovoltaic cell with different levels of detail. As photovoltaic modules consist of a series connection of cells these models can also be used to describe the module behaviour.

Using circuit simulation tools a photovoltaic system can be modelled using an equivalent circuit for the photovoltaic generator with appropriately selected values for the components in the equivalent circuit model. However, such an electrical simulation can lead to long simulation times. Also, a closed loop controller to find the MPP of the photovoltaic generator needs to be implemented in such a simulation. To speed up the simulation of the photovoltaic generator the analytical description of a photovoltaic generator presented by Alqahtani et.al. [78] was used.

According to [78] the IV-characteristic of the PV generator is expressed as

$$I = I_{sc}\left(1 - C_2\left(e^{\frac{V}{C_1 V_{oc}}} - 1\right)\right) \tag{4.10}$$

where C_1 and C_2 are expressed as follows:

$$C_1 = \frac{\frac{V_{mpp}}{V_{oc}} - 1}{ln\left(1 - \frac{I_{mp}}{I_{sc}}\right)} \tag{4.11}$$

$$C_2 = \left(1 - \frac{I_{mp}}{I_{sc}}\right) e^{\frac{-V_{mpp}}{C_1 V_{oc}}} \tag{4.12}$$

The short-circuit current I_{sc}, the open-circuit voltage V_{oc} and the maximum-power point voltage V_{mpp} and current I_{mpp} are expressed by Alqahtani et.al. [78] through the following equations, which depend on the module irradiance $E_{G,gen}$ and the number of photovoltaic modules in series, N_{ss}, as well as the number of strings connected in parallel, N_{pp}.

$$I_{sc}(E_{G,gen}) = N_{pp} \cdot I_{sc,stc} \frac{E_{G,gen}}{E_{stc}} \tag{4.13}$$

$$V_{oc}(E_{G,gen}) = N_{ss} \cdot V_{oc,stc} + N_s V_T log\left(\frac{E_{G,gen}}{E_{stc}}\right) \tag{4.14}$$

$$I_{mpp}(E_{G,gen}) = N_{pp} \cdot I_{mpp,stc} \frac{E_{G,gen}}{E_{stc}} \tag{4.15}$$

$$V_{mpp}(E_{G,gen}) = N_{ss} \cdot V_{mpp,stc} + N_s V_T log\left(\frac{E_{G,gen}}{E_{stc}}\right) \tag{4.16}$$

In addition to the irradiance the module performance is influenced by the temperature. The temperature dependence is represented by Alqahtani et. al. [78] in the following equations

$$I_{sc}(T) = I_{sc}(T_{stc}) + K_I \cdot (T - T_{stc}) \tag{4.17}$$

$$V_{oc}(T) = V_{oc}(T_{stc}) + K_V \cdot (T - T_{stc}) \tag{4.18}$$

$$I_{mpp}(T) = I_{mpp}(T_{stc}) + K_I \cdot (T - T_{stc}) \tag{4.19}$$

$$V_{mpp}(T) = V_{mpp}(T_{stc}) + K_V \cdot (T - T_{stc}) \tag{4.20}$$

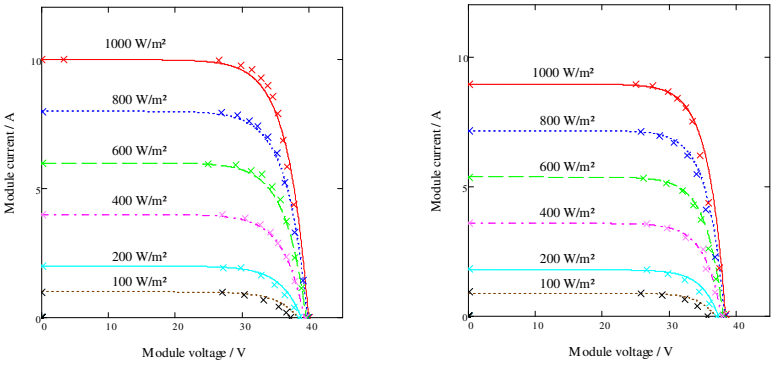
The parameters to the above equations are summarised in Table 4.2. All the information required can be readily obtained from photovoltaic module datasheets.

To illustrate that the analytical description reproduced above from [78] is suitable for poly-silicon as well as mono-crystalline silicon PV modules a comparison of

Table 4.2.: Constants and parameters for model of PV module

Variable	Description	Unit
I	PV module terminal current	A
V	PV module terminal voltage	A
I_{sc}	PV module short-circuit current	A
V_{oc}	PV module open-circuit voltage	V
V_{mpp}	PV module MPP voltage	V
I_{mpp}	PV module MPP current	A
V_T	thermal voltage constant	mV
K_V	Temperature coefficient of MPP voltage	%
K_I	Temperature coefficient of MPP current	%
N_s	Number of PV cells in module	
N_{ss}	Number of PV modules per string	
N_{pp}	Number of strings in parallel	

the IV-characteristic predicted by the model and the data provided in two module data-sheets [79, 80] was done in Figure 4.5. The data extracted from the plots in the data-sheets is shown as crosses and is in good agreement with the plotted lines predicted by the model.



(a) Solarworld SW 290 mono

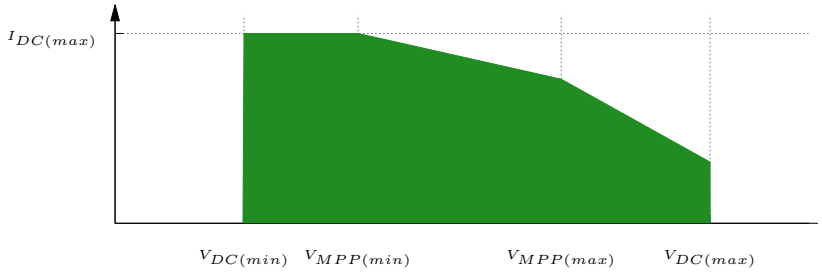
(b) Solarworld SW 260 poly

Figure 4.5.: Modelled IV-characteristic (lines) vs. points taken from IV-characteristics in the data-sheets of the two PV modules [79, 80]. ($T_{module} = 25\,^{\circ}\mathrm{C}$)

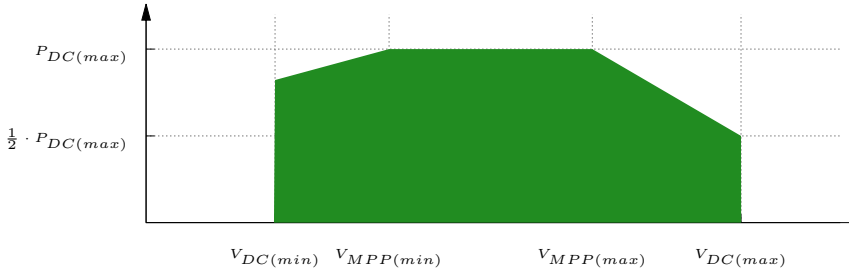
4.2.4. Behavioural model of the photovoltaic inverter

In order to maximise energy yield from the photovoltaic generator the photovoltaic inverter attempts to track the MPP of the generator. This is typically done by an MPP tracker in the control system of the inverter. For the purpose of the simulations the MPP is found using equations 4.16 and 4.15.

If the MPP of the photovoltaic generator lies within the operating range of the inverter as illustrated in Figure 4.6 the computed MPP is assumed as the operating point of the inverter. Otherwise, the operating voltage of the photovoltaic generator is increased and the new output current is computed using equation 4.10. This process is repeated until an operating point is found which lies within the permissible operating range of the inverter.



(a) Input current limits



(b) Input power limits

Figure 4.6.: Possible operating ranges for the inverter (similar illustration previously published in [62]).

If no permissible operating point can be found (e.g. if the irradiance is too low and hence the open-circuit output voltage of the photovoltaic generator lies below the minimum DC voltage of the inverter) the inverter is assumed to cease operating in which case the input voltage to the inverter will be the open-circuit voltage of the photovoltaic generator and the input current will be zero.

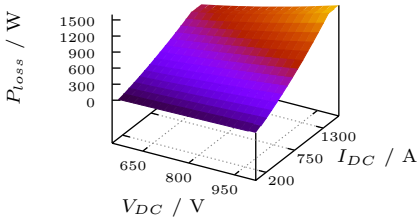
4.2.5. Computation of semiconductor losses

In order to identify the temperature cycles at the semiconductors and at the baseplate (case) of the used semiconductor modules thermal simulations need to be carried out which consider the electrical losses of the semiconductors as well as the performance of the cooling system. Such multi-domain simulations have the tendency to take very long, as the smallest possible time-step in the electrical simulation of a power electronic converter is determined by the frequency at which the semiconductors are switched [81]. Full-resolution electro-thermal simulations using mission profiles in the range of years are thus not feasible using full time resolution.

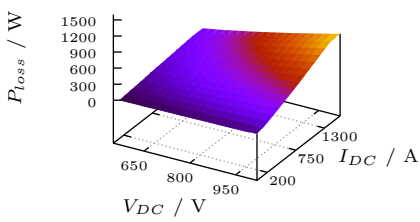
To overcome this problem and yet enable coupling between the electrical and thermal simulations (i.e. to represent the temperature dependency of the semiconductor losses) a simulation strategy similar to the work presented by Drofenik et.al. [81] was employed. A large look up table (LUT) of the average semiconductor losses that occur at different converter operating points and semiconductor temperatures is generated. This look up table (LUT) is then used to obtain temperature dependent transient losses during the thermal simulation.

To generate the LUT of the semiconductor losses the tool *TopBench* developed at the EVS/KDEE by Nöding [11] was used. This tool uses a database of measured device characteristics to calculate the average semiconductor losses over a period of the fundamental waveform (i.e. 20 ms in a 50 Hz grid-frequency inverter). The conduction-losses are computed by modelling the device currents and multiplying them with the measured collector-emitter voltage drop in the case of IGBTs and the measured forward voltage in the case of diodes. To obtain the switching losses the device current and commutation voltage for each switching event are modelled. The switching energies are then obtained from a database created based on loss-measurements for the desired semiconductor and summed over the fundamental period to obtain the average losses. Details about the methodologies used to calculate the losses can be found in [11].

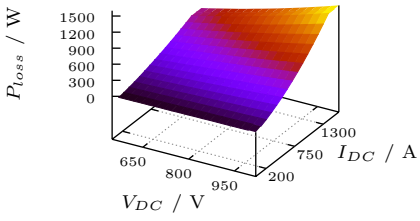
A scripting interface to *TopBench* allows a look-up-table of the average semiconductor losses at a large number of converter operating points to be created in very little time. Using a circuit simulation to obtain this data would require much more time. The content of an exemplary LUT of the semiconductor losses at a fixed chip temperature and AC voltage is shown for different DC operating points in Figure 4.7. The actual LUT in the simulation contains this data also for different AC voltages and chip temperatures which are not shown here for better readability.



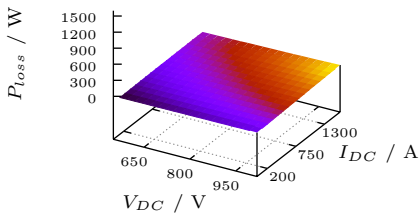
(a) HS IGBT



(b) HS diode



(c) LS IGBT



(d) LS diode

Figure 4.7.: Exemplary look-up-table of semiconductor losses for a single IGBT module (two are connected in parallel for each phase) with $V_{ac} = 360\,\mathrm{V}$, $T_j = 150\,^{\circ}\mathrm{C}$ and $cos\phi = 1$.

4.2.6. Thermal model of the power electronic stack

A thermal model of the power-electronic-modules and the cooling system is required to estimate the temperature transients from the transient losses and the varying ambient temperature. It is assumed that the three phase arms of the investigated 2-level inverter (B6 topology) are built as three independent but identical power stacks, which allows the model to be simplified to represent just one phase arm.

In Figure 4.8 the structure of a Foster type thermal model that is used to model the IGBT modules that make up one phase-arm of the converter is shown. The phase arm consists of two IGBT modules on a common heat-sink and it is assumed that the set-up is symmetrical and that the two IGBT modules can thus be modelled by just modelling the four switches. It has to be noted that the Forster type model is a mathematical representation of the thermal impedances and not a physical representation of the heat flow.

The thermal coupling between neighbouring devices (the IGBT and the anti-parallel diode chips are in close proximity) was neglected in this investigation, because measurement data from which the thermal impedances between the devices within the power module could have been extracted were not available.

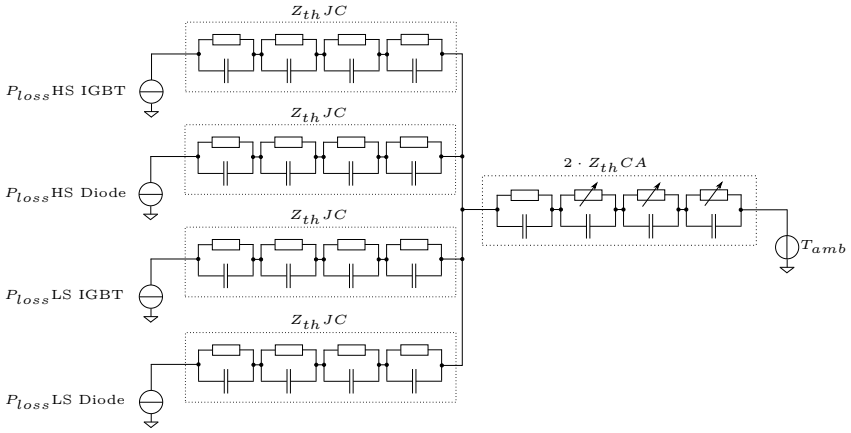


Figure 4.8.: Structure of Foster type thermal model for one phase-arm of B6 inverter.

A set of twelve cooling curves measured on a power stack with two parallel half-bridge IGBT modules was available for this investigation[2]. The datasets contain the (maximum) temperature of one of the IGBT/diode chips in which losses were generated by a large DC current in each module. Additionally, the temperature of the NTCs inside each module, the surface temperature of the heat-sink at a point between the two modules and the measured ambient temperature were included in the datasets. The cooling curves in the dataset were recorded at six different fan speed settings and with either the diodes or the IGBTs heated.

For the junction-to-case thermal impedances data-sheet values for the investigated IGBT modules were used [82]. Using the known thermal impedance of the junction-to-case the transient case temperatures were computed and a fitting process was used to find the values for the case-to-ambient thermal impedance $Z_{th}CA$. The latter impedance contains variable thermal resistances to account for the changing speed of the cooling fan. Thermal capacitances were kept constant for all fan-speeds to ensure energy conversation when changing the fan-speed setting in later simulations. The parameters for the thermal model are summarised in Table B.1 in Appendix B.

The disadvantage of the Foster type thermal model shown above is that changes in the ambient temperature are immediately seen across the entire model. Also, the model structure is not a physical representation of the heat flow. However, it is possible to convert a Foster type model into an equivalent Cauer type model as is also done for example in [83, 84]. A method to carry out such a conversion is described in [85]. The structure of a Cauer type model that can be used to model the IGBT modules of one phase-arm of the converter considered in this investigation is shown in Figure 4.9.

A Matlab script based on a script by Ufnalski [86] was used to carry out the conversion of the models for the different fan speeds. Finally, the capacitances were set to the average taken across the capacitances for fan speeds of 20 % to 100 % as they have to be maintained constant to conserve energy when the fan speed is changed.

The parameters for the Cauer type thermal model are provided in Table B.2 in Appendix B. Also shown in Appendix B are the recorded cooling curves and simulation results of step responses for both the Foster type and Cauer type model. The Foster type model is in good agreement with the measured cooling curves, which is expected as the model was fitted to these curves.

[2]The measured cooling curves were provided by a project partner within the project *Giga-PV*

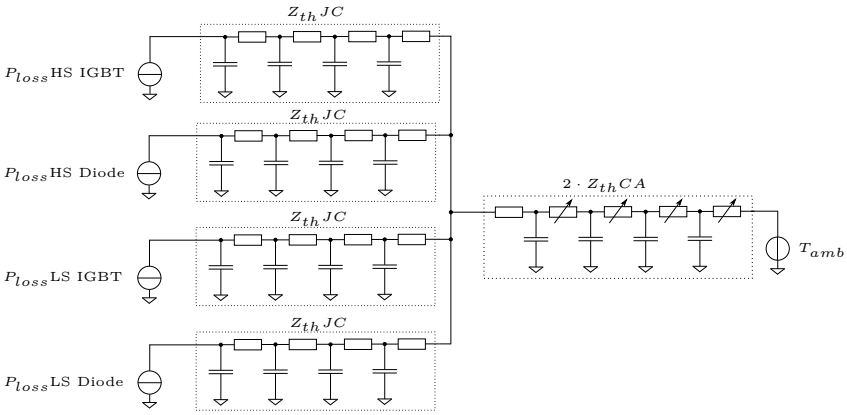


Figure 4.9.: Structure of Cauer type thermal model for one phase-arm of B6 inverter.

The Cauer type model is in relatively good agreement with the recorded cooling curves for fan speeds of 20 % and above. The difference between the Foster and Cauer models is a consequence of averaging the thermal capacitances in the Cauer models of each fan speed after the conversion from the Foster to the Cauer model to obtain a single model for the different fan speeds. This step is necessary to ensure conservation of energy when the fan speed is varied.

As a result a difference not only between the Foster and Cauer models is observed, but also between the Cauer model and the measured cooling curves. It would be beneficial to directly fit the Cauer model to the cooling curve with the constraint of constant thermal capacitances, as was done for the Foster model. However, this fitting process is significantly more complex as no simple closed form description of the Cauer network in the time domain is available. As discussed by März and Nance in [87] the cooling curves could be transformed to the Laplace domain to carry out the curve fitting there. This approach was not tested here but could be explored for future work.

The Cauer type model is used in the remainder of this investigation even though there are some deviations between the cooling curves and the simulated step responses due to the conversion step from the Foster to the Cauer model because its structure is physically meaningful.

For a number of investigated scenarios simulations were also performed using the Foster model. The results of a comparison conducted on the results of the simulations with the different thermal models is included in Appendix C. The comparison has shown, that the main limitation of the Foster model is that ambient temperature changes directly influence the predicted temperatures. This is a consequence of the structure of the model and is another factor why the Cauer model structure was finally selected for the further investigations in this work.

In the application a closed-loop controller will typically be used to set the fan-speed in order to maintain the heat-sink temperature at a certain level. In the simulation the fan-speed is set by calculating first the required thermal resistance $R_{th,req}$ from the known losses and the difference between the desired heat-sink temperature $T_{hs,set}$ and the ambient temperature T_{amb} as

$$R_{th,req} = \frac{T_{hs,set} - T_{amb}}{P_{loss}} \tag{4.21}$$

The fan-speed is then obtained through a look-up-table that relates the cooling system R_{th} to the fan-speed. This approach will not yield perfect results as the thermal capacitance and hence the delay of the cooling system's response to a change in losses is neglected. However, the approach has the advantage that the simulation without a closed-loop controller is very fast and stable.

4.2.7. Simulation outputs

The output of the main simulation are transients of the computed quantities. In post-processing scripts these transients are analysed to quantify the expected stresses on the semiconductor modules.

Transient signals

Aside from configuration data which is constant over time the simulation uses transient input data that is taken from the selected mission profile. The input temperature and solar irradiance are shown in Figure 4.10 for an exemplary five day period.

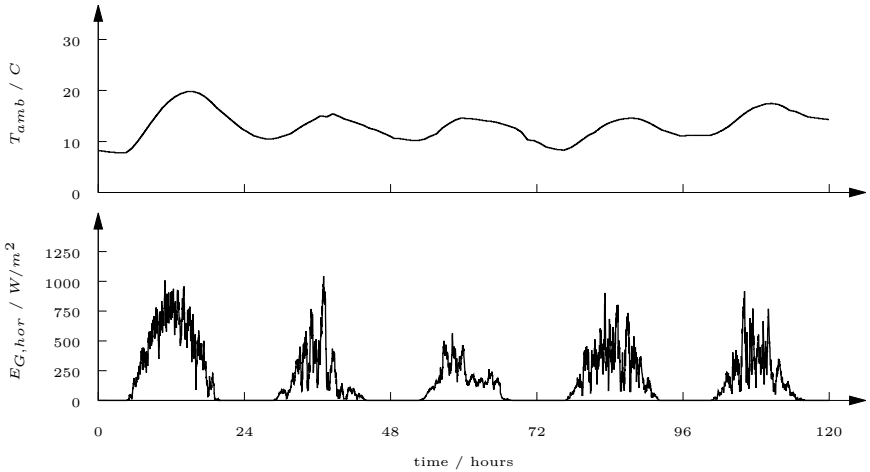


Figure 4.10.: Exemplary simulation inputs (Kassel, days 135 to 139)

From the input transients intermediate data is generated when executing the simulation. As examples the irradiance on the tilted photovoltaic modules and their temperature are shown in Figure 4.11.

The irradiance conditions shown in Figure 4.11 are converted into a load profile for the photovoltaic inverter. The resulting load profile (input current and voltage) is shown in Figure 4.12.

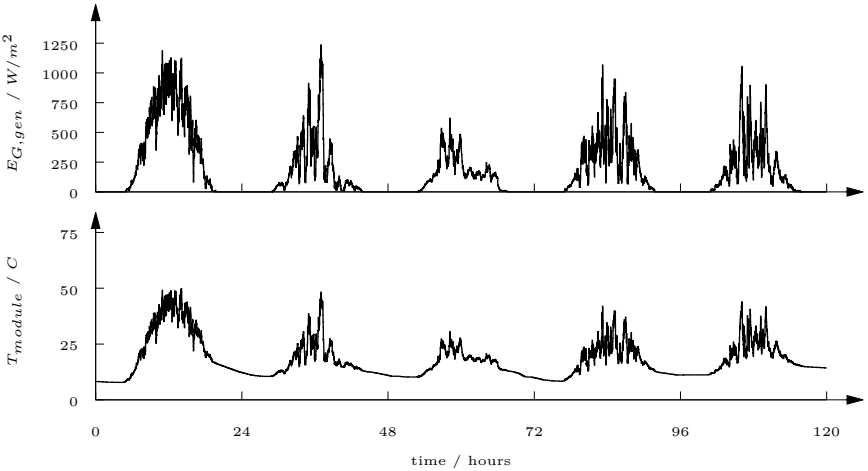


Figure 4.11.: Exemplary transient photovoltaic generator irradiance and module temperature (Kassel, days 135 to 139, fixed tilt modules)

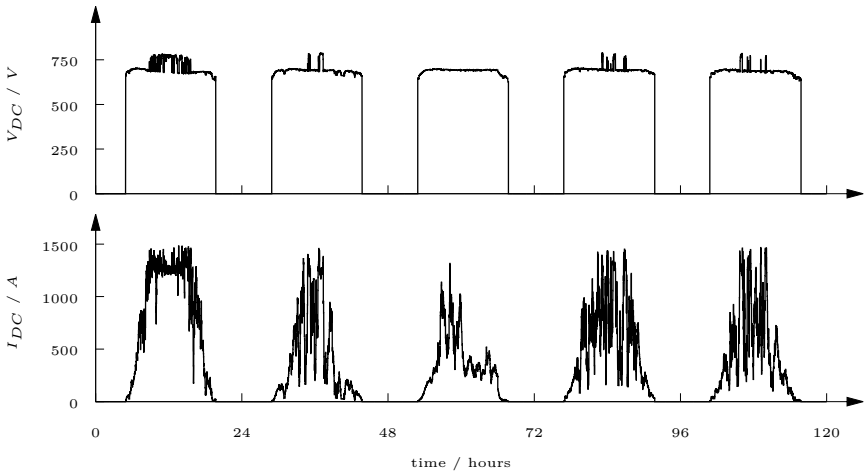


Figure 4.12.: Exemplary inverter input transients (Kassel, days 135 to 139, size-ratio 1.5, fixed tilt modules)

Finally, the semiconductor losses are calculated and applied to the thermal model. The semiconductor losses (sum of losses for all four devices in one half-bridge power electronic module) and the resulting temperatures of the high-side IGBT and the module baseplate alongside the speed of the cooling fan are shown in Figure 4.13.

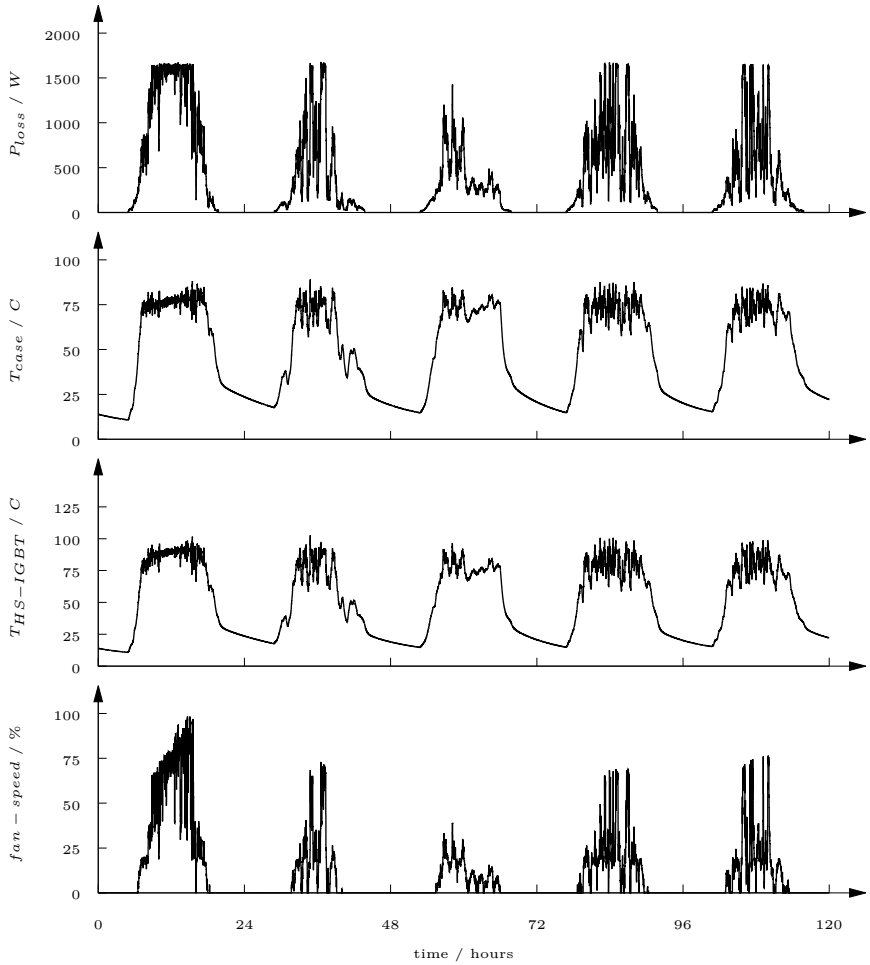


Figure 4.13.: Exemplary transients of semiconductor losses (total in one IGBT module), temperatures of high-side IGBT and heat-sink and simulated fan speed (Kassel, days 135 to 139, size-ratio 1.5, fixed tilt modules)

Predicted temperature cycles

From the simulated transient temperatures the temperature cycles at the semiconductor chips and at the baseplate of the IGBT module are extracted using the *rainflow algorithm* [88] as implemented by Nieslony [89]. Compared to other methods of counting cycles the rainflow algorithm gives the lowest error and ensures that the largest cycles are captured [90]. The cycles expected to occur at the semiconductor chips as well as at the module baseplate are provided as outputs of the simulation for later analysis.

In Figure 4.14 the temperature cycles predicted to occur at the baseplate of a three-phase inverter during one year of operation in Kassel (Germany) with a photovoltaic generator with fixed modules and a nominal power of 1.5 times the rated power of the inverter are shown.

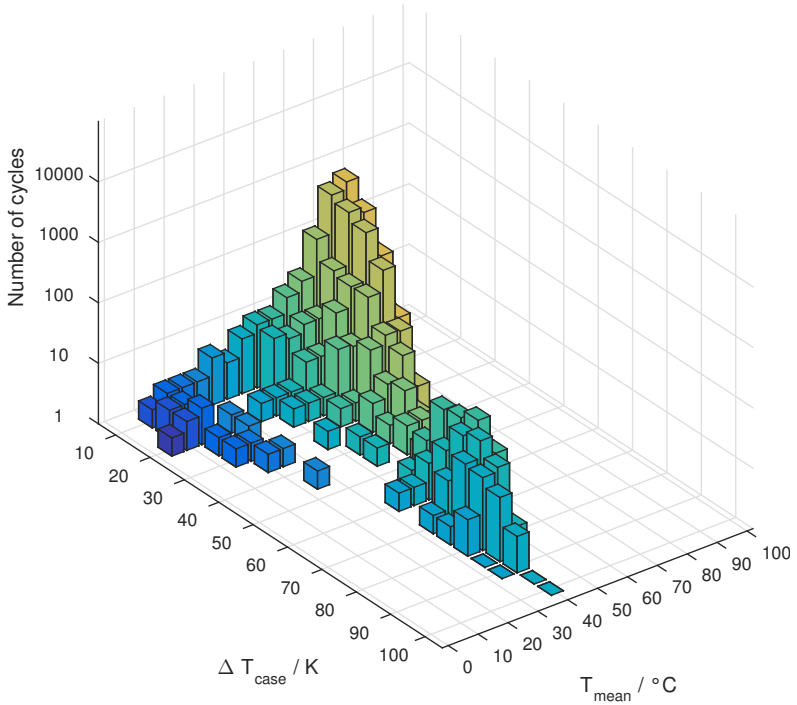


Figure 4.14.: Simulated temperature cycles at the heat-sink of a central inverter operated for one year in Kassel (Germany), size ratio = 1.5, fixed modules.

The temperature cycles extracted from the simulated temperature transients at the high-side IGBT during one year of operation in Kassel (Germany) with a photovoltaic generator with fixed modules and a rated power of 1.5 times the rated power of the inverter are shown in Figure 4.15.

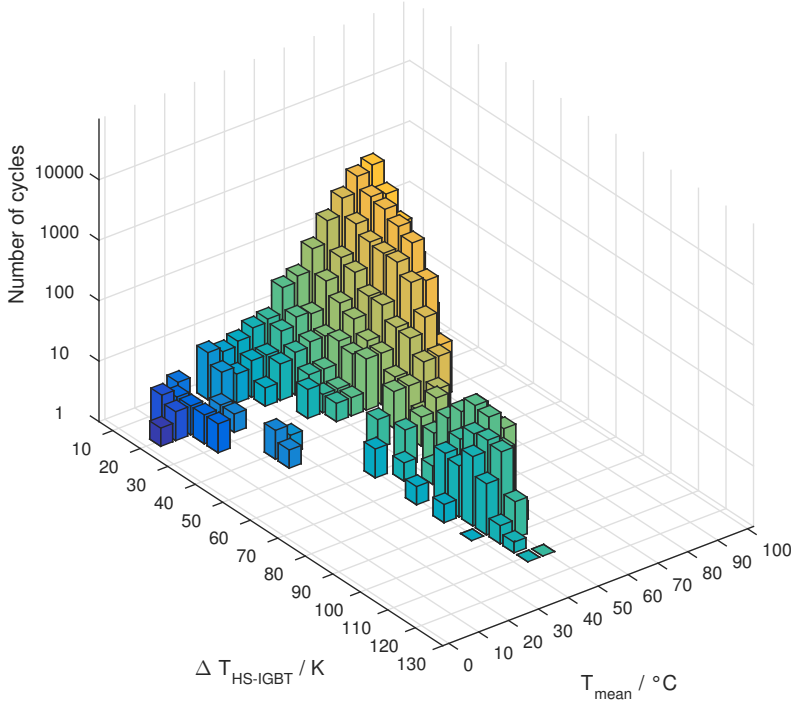
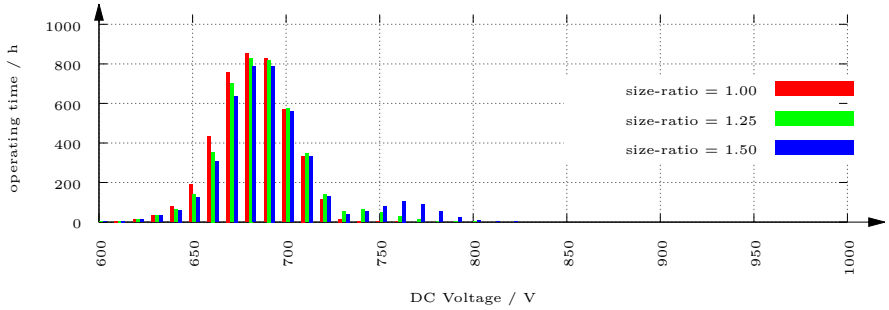


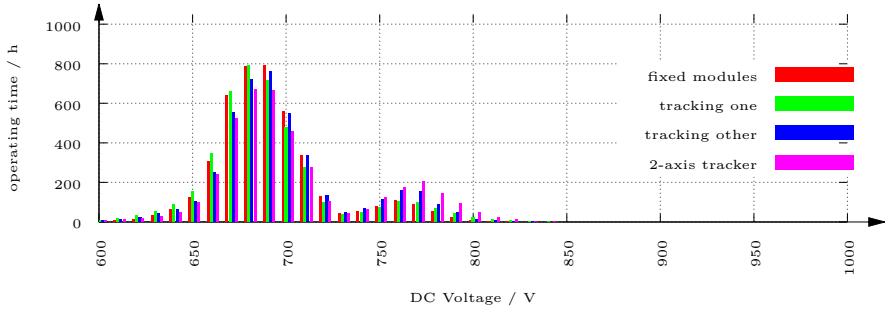
Figure 4.15.: Simulated temperature cycles at the high-side IGBT of a central inverter operated for one year in Kassel (Germany), size ratio = 1.5, fixed modules.

Predicted voltage stress

To analyse the voltage stress on the semiconductors a histogram of the operating times at different DC-link voltages is created from the simulation output. An example of such a histogram is provided in Figure 4.16. It shows the operating hours at different DC voltages for an inverter in Kassel (Germany) over one year for different configurations of photovoltaic generators (sizing ratio and tracking type were varied) under the assumption that the inverter can always operate without external constraints such as output power curtailment.



(a) fixed modules, varying size-ratio



(b) fixed size-ratio = 1.5, different trackers

Figure 4.16.: Predicted distribution of DC voltage over time for a photovoltaic inverter in Kassel (Germany) with different types of photovoltaic generator.

From the diagram it can be seen, that increasing the size-ratio between the photovoltaic generator and the inverter increases the voltage stress. Additionally, the diagram shows that the use of a tracker further increases the voltage stress.

4.2.8. Summary of simulation features

The simulation described in this section allows the temperature cycling and voltage stresses on the IGBT modules in a photovoltaic inverter to be determined. The simulation using a typical one-year long mission profile takes approximately 15 min.

By selecting different photovoltaic generator set-ups and mission profiles various factors that may influence the stresses can be investigated. Additionally, it is possible to change operating parameters of the inverter itself for example by changing the maximum operating voltages or the permissible input current.

To investigate changes to the inverter's hardware design (e.g. use of different semiconductors / alternative cooling system) or the adoption of other modulation strategies slightly more effort is required. Such changes require new look-up-tables of semiconductor losses to be generated and new parameters for the thermal model to be defined.

The simulation framework is modular and could be extended further to obtain data to analyse the stresses on additional components in a photovoltaic central inverter. For example, the stresses on the DC-link capacitors could be obtained if a suitable model for their thermal behaviour was added to the simulation.

4.3. Evaluation of stresses on power semiconductors

4.3.1. Estimation of lifetime limits due to cycling load

In section 2.4.1 the packaging related failure mechanisms of power electronic modules were described. It was highlighted, that the main stress leading to wear-out failures of the power electronic modules is temperature cycling stress. In order to evaluate the expected lifetimes of power electronic modules the cycling stresses in a given application need to be identified and related to the cycling capability of the modules.

Manufacturers of IGBT modules provide cycling capability data for their products that can be used to estimate the lifetime of the IGBT module based on the expected temperature cycles [25]. Such data contains lifetime curves that specify the maximum number of cycles with a given temperature swing and mean temperature $N_f(\Delta T, T_m)$ that a device can be exposed to before the capability limit is reached.

The temperature cycles expected to occur at the semiconductor chips and at the heat-sink were obtained from the simulation (compare Figure 4.14 and Figure 4.15 in Section 4.2.7). To relate the occurring cycling stress to the capability of the power electronic modules the following equation was used.

$$c = \sum_{\Delta T, T_{max}} \frac{N\left(\Delta T, T_{max}\right)}{N_f\left(\Delta T, T_{max}\right)} \cdot 100\% \tag{4.22}$$

In the equation $N\left(\Delta T, T_{max}\right)$ stands for the number of cycles with a given temperature swing ΔT and maximum temperature T_{max} predicted by the simulation and $N_f\left(\Delta T, T_{max}\right)$ stands for the permissible number of cycles at a given temperature swing and maximum temperature.

The value of c in the above equation represents the percentage of the cycling capability that is expended as a consequence of applying a given mission profile. If the value reaches $c = 100\,\%$ the module is considered to have reached its specified cycling capability limit. This means that a mission profile that results in predicted cycles that lead to a value of $c = 2\,\%$ can be applied a maximum of 50 times before the module's cycling capability limit is reached.

4.3.2. Estimation of single-event-burnout failure rate

The failure rate for cosmic radiation induced single-event-burnout depends on the applied voltage and the local neutron flux rate as was shown in Chapter 3. Since the DC voltage applied to the semiconductors varies over time the average failure rate has to be computed by computing the failure rate for each point in time $\lambda(t)$ and integrating over the entire duration of a mission profile.

$$\lambda_{SEB,NYC} = \frac{1}{t_{end}} \int_{t=0}^{t=t_{end}} \lambda(t)\, dt = \frac{1}{t_{end}} \int_{t=0}^{t=t_{end}} \lambda\left(U_{DC}(t)\right)\, dt \tag{4.23}$$

Instead of computing the failure rate for every data point the data for the histogram of the operating time vs. DC-link voltage is used to compute the average failure rate (see e.g. Figure 4.16). For each of the n bins of the histogram the failure rate corresponding to the bin voltage $V_{DC}[n]$ is computed and weighted by the operating time as expressed in the following equation.

$$\lambda_{SEB,NYC} = \frac{\sum_{i=0}^{n} \lambda\left(V_{DC}[i]\right) \cdot T_i}{\sum_{i=0}^{n} T_i} \tag{4.24}$$

Once the average failure rate is computed using the above equation it needs to be adjusted to the local terrestrial neutron flux at a given location. For that purpose the acceleration factors for altitude F_A and location F_B were calculated according to JESD89A [46] under the assumption of average solar activity. Finally, the estimated failure rate at a given location is thus computed as follows.

$$\lambda_{SEB} = F_A \cdot F_B \cdot \lambda_{SEB,NYC} = F_A \cdot F_B \cdot \frac{\sum_{i=0}^{n} \lambda\left(V_{DC}[i]\right) \cdot T_i}{\sum_{i=0}^{n} T_i} \tag{4.25}$$

4.4. Investigated scenarios

The simulation presented in the first section of this chapter was used to determine the stresses on the semiconductor modules in a photovoltaic central inverter for a total of 8 locations in the earth's sunbelt and a reference location in central Europe. The locations are highlighted in the map in Figure 4.17[3] and are also listed in Table 4.3 together with the elevation of the relevant sites. For each location solar irradiance data and temperature data for one year at a time resolution of 60 s was exported from *Meteonorm 7.1* to conduct the simulations.

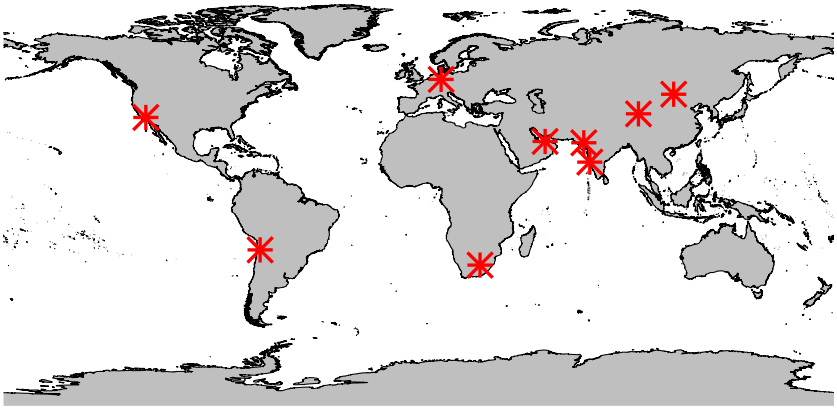


Figure 4.17.: Map showing the locations for PV installations investigated in this study.

For each location a photovoltaic system with a central inverter with a rated power of 1000 kW was considered. The installed nominal power of the photovoltaic generator was varied in two steps between 1000 kW and 1500 kW, which corresponds to sizing ratios of between 1.0 and 1.5. Additionally, four different types of photovoltaic generator set-ups were considered (fixed installation, single axis tracker (azimuth), single axis tracker (elevation) and a two-axis tracker). This leads to a total of 12 scenarios for each location.

[3]Made with Natural Earth. Free vector and raster map data @ `naturalearthdata.com`. Plot created using reshaped data file and script by Hagen Wierstorf from `http://www.gnuplotting.org/plotting-the-world-revisited/` (last visited 19.03.2017)

Table 4.3.: Locations investigated in this study

Place	**Country / Region**	**Latitude**	**Longitude**	**Elevation**
Kassel	Germany	51.30 °N	9.45 °E	233 m
Golmud	China	36.42 °N	94.90 °E	2809 m
Redmond	U.S.A. (CA)	34.83 °N	118.40 °W	790 m
Charanka	India	23.89 °N	71.19 °W	30 m
Goa	India	15.48 °N	73.82 °E	55 m
Calama	Chile (Atacama)	22.50 °S	68.90 °W	2312 m
Abu Dhabi	U.A.E.	24.43 °N	54.47 °E	3 m
Sainshand	Mongolia (Gobi)	44.90 °N	110.12 °E	938 m
Bloemfontain	South Africa	29.10 °S	26.30 °E	1351 m

The key specifications of the considered inverter are summarised in Table 4.4. Above the maximum MPP voltage of 850 V the maximum power processed by the inverter is reduced linearly until it reaches 50 % of the maximum power at the open-circuit voltage.

Table 4.4.: Specifications of assumed photovoltaic central inverter.

$P_{DC(max)}$	1000 kW
$V_{DC(min)}$	530 V
V_{MPP}	645 to 850 V
$V_{DC(max)}$	1000 V
$I_{DC(max)}$	1550 A
$V_{AC(nom)}$	360 V

4.5. Results

4.5.1. Temperature cycling stress on IGBT modules

To evaluate the expected lifetime of the IGBT power modules the temperature cycles occurring at the semiconductor chips as well as the temperature cycles at the module baseplate were compared to the cycling capability data of the modules[4].

Temperature cycles at heat-sink

In Fig 4.18 the damage factor predicted for a one-year mission profile at each of the investigated locations is shown. In this figure data for different sizes of photovoltaic generator is shown. In this case fixed modules were assumed.

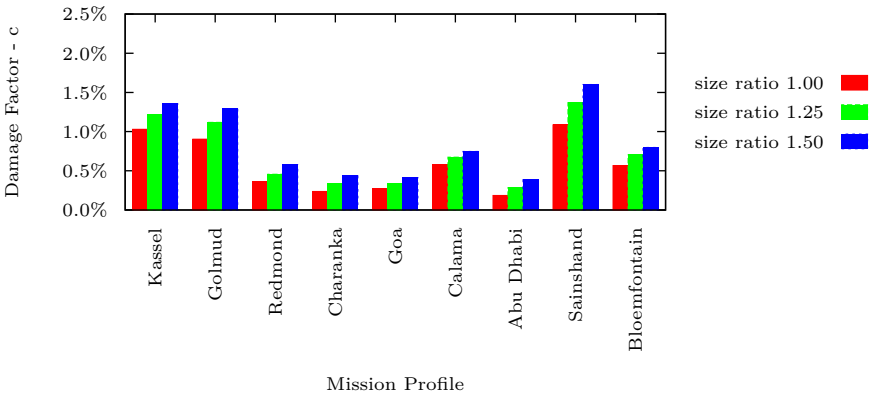


Figure 4.18.: Damage factors for operation of IGBT module in a PV central inverter with a fixed PV generator, one-year mission profiles. T_{case}-cycles applied to thermal cycling capability data.

In Fig 4.19 the predicted damage factors for different photovoltaic generator types are shown. In this case the size of the photovoltaic generator was fixed at 1.5 times the rated inverter power.

[4]Cycling capability provided by the module manufacturer was used. The data was extrapolated where necessary.

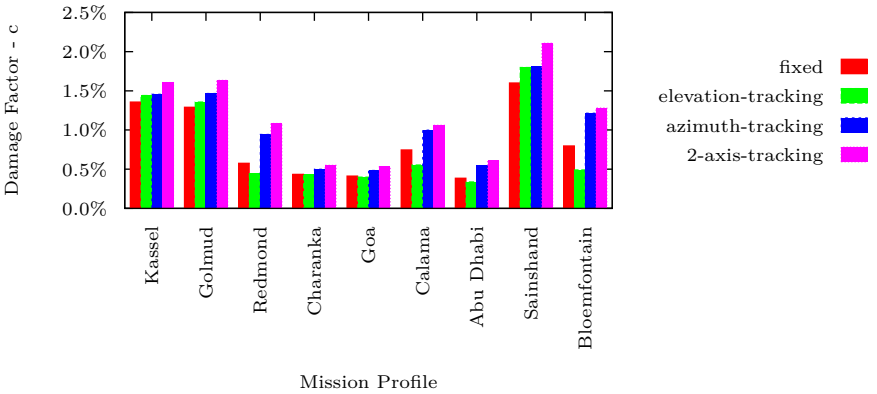


Figure 4.19.: Damage factors for operation of IGBT module in a PV central inverter with a different types of PV generators, fixed size-ratio of 1.5, one-year mission profiles. T_{case}-cycles applied to thermal cycling capability data.

From Fig. 4.18 and Fig. 4.19 it can be seen, that increasing the size-ratio between the nominal power of the photovoltaic generator and the inverter increases the temperature cycling stress on the IGBT modules in all locations. Also, it can be seen that systems with trackers result in slightly higher damage factors.

The results show that in Golmud (China), Sainshand (Mongolia) and Kassel (Germany) the highest temperature cycling stresses are predicted. Each day the heat-sink temperature is allowed to rise to a fixed set-point of e.g. 80 °C by the cooling control system. During the night the system cools down as no losses occur in the semiconductors while the inverter is shut down. The locations in which the highest temperature cycling stress is observed are characterised by relatively low average ambient temperatures. As a consequence of the low ambient temperatures the heat-sink cools down further than in other locations and therefore the daily temperature cycle is particularly large in these locations.

Overall, it can be seen that the damage factors for all investigated locations remain below 2.5 % even if tracking systems are combined with large size-ratios between photovoltaic generators and inverters. While the damage mechanisms is clearly relevant and needs to be taken into consideration when designing the inverter the results show that the desired operating periods in the range of 25 years or more can be achieved. The results also show that most locations will permit significantly longer lifetimes.

Temperature cycles at semiconductor chip

In the following two diagrams the cycling stress at the semiconductor chips is shown. Again the size ratio between inverter and photovoltaic generator was varied (Figure 4.20) as well as the type of generator set-up (Figure 4.21).

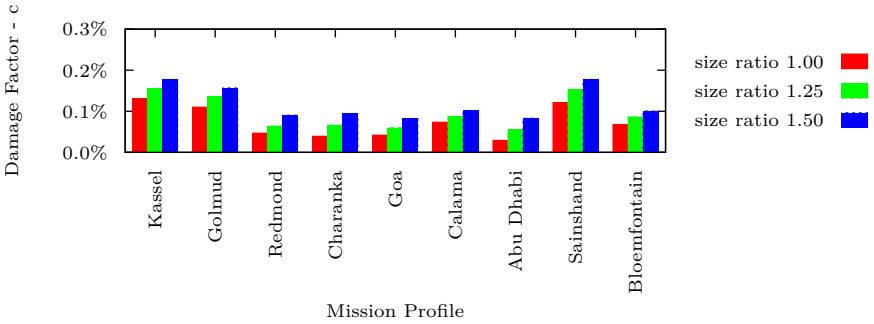


Figure 4.20.: Damage factors due to temperature cycles at high-side IGBT chip. Fixed PV generator, variable size-ratio, one-year mission profile. $T_{j,HS-IGBT}$-cycles applied to power cycling capability data.

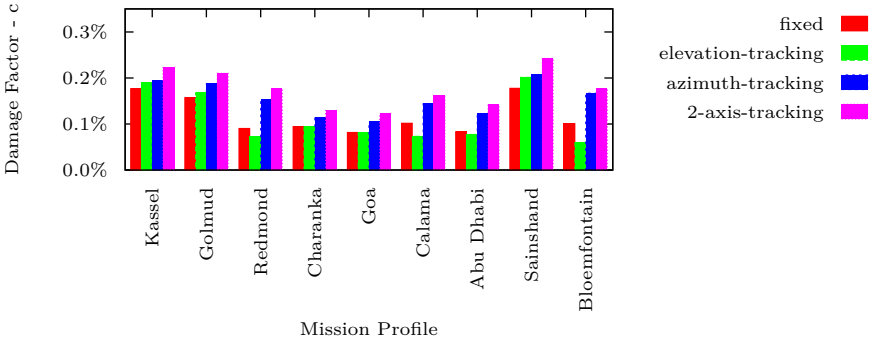


Figure 4.21.: Damage factors due to temperature cycles at high-side IGBT chip. Different types of PV generator trackers, fixed size-ratio of 1.5, one-year mission profile. $T_{j,HS-IGBT}$-cycles applied to power cycling capability data.

The results shown in Figure 4.20 and Figure 4.21 show that for all considered locations and generator set-ups the damage factor remains significantly below 1 %. Therefore, power cycling at the semiconductor chips appears not to limit the lifetime of the semiconductor modules in the application of PV central inverters.

4.5.2. Semiconductor failure rate due to cosmic radiation

The semiconductors that were used to simulate the inverter in this chapter were not included in the measurement campaign to determine their robustness against cosmic radiation induced SEB (see Chapter 3). Therefore, data for Si-IGBT-A was used and scaled to the chip area of the IGBTs in the power electronic module considered in this study. Likewise, data for a typical Si diode from [52] was scaled to the chip area of the diode in the power electronic module.

What failure rate due to cosmic radiation induced SEB is tolerable is a design criteria that needs to be set by the system manufacturer. One approach for finding the tolerable level may be to decide that the failure of a certain percentage of systems during the expected lifetime can be tolerated. A possible criterion could be that no more than 2 % of inverters of a given type should fail within 25 years due to cosmic radiation induced SEB. In that case, a maximum failure rate of 92 FIT could be considered tolerable.

Failure rates under optimal inverter operating conditions

In the following two figures the expected failure rate due to cosmic induced SEB is shown for the investigated locations. It was assumed that the inverter can operate without external constraints.

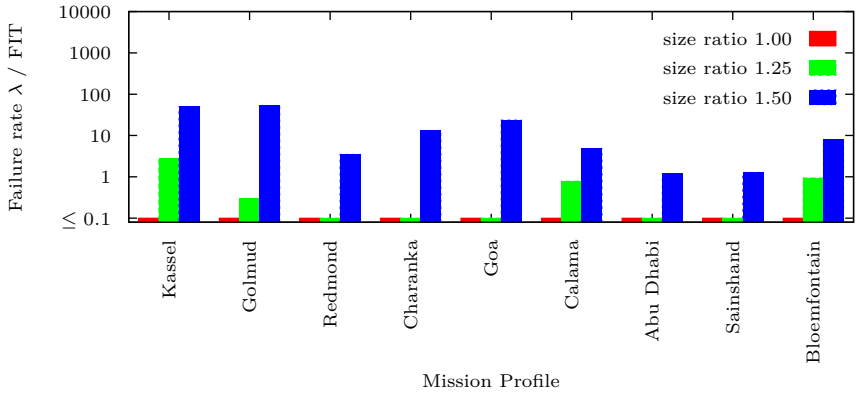


Figure 4.22.: Failure rate due to single-event-burnout. Fixed PV generator, varying size-ratio, one-year mission profile.

The results in Figure 4.22 show that if a fixed tilt PV generator is assumed relevant failure rates are only expected if the photovoltaic generators has a much larger rated power than the inverter. This is in agreement with expectations, as increasing the generator size leads to the occurrence of situations where the available power from the photovoltaic generator exceeds the power processing capability of the inverter. As a consequence the inverter limits the input current and the output voltage of the photovoltaic generator rises.

In the following figures the expected failure rates if trackers are used on photovoltaic generator with a size-ratio of 1.00, 1.25 and 1.50 are shown.

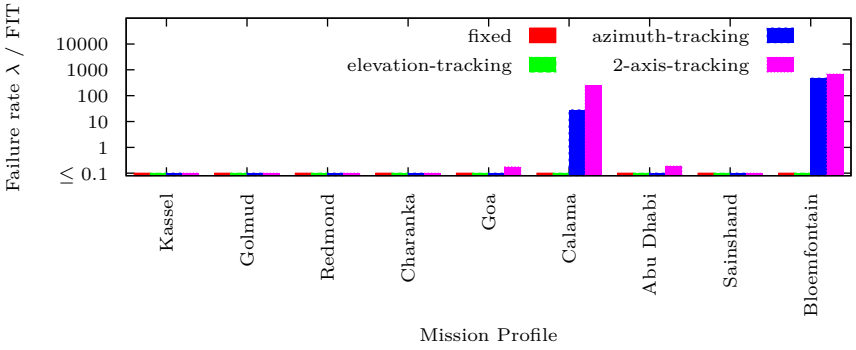


Figure 4.23.: Failure rate due to single-event-burnout. Different types of PV generator, fixed size-ratio of 1.00, one-year mission profile.

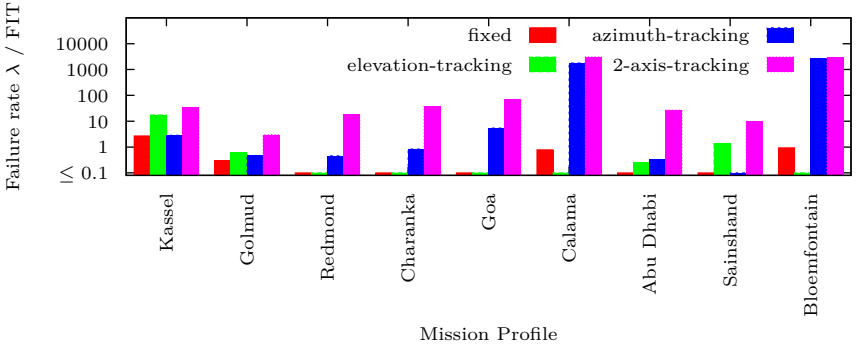


Figure 4.24.: Failure rate due to single-event-burnout. Different types of PV generator, fixed size-ratio of 1.25, one-year mission profile.

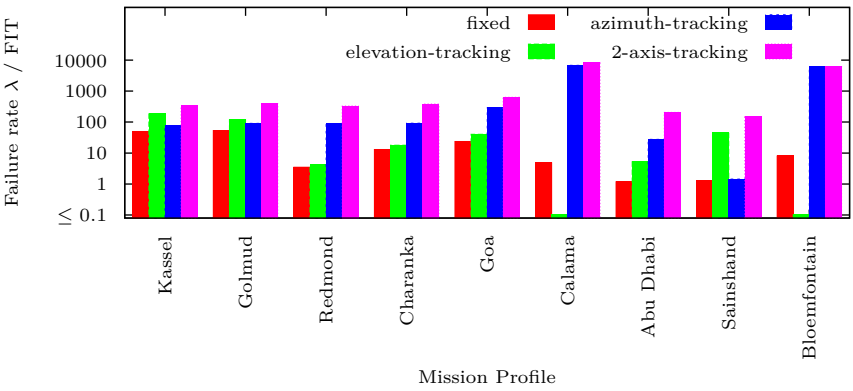


Figure 4.25.: Failure rate due to single-event-burnout. Different types of PV generator, fixed size-ratio of 1.5, one-year mission profile.

As expected, the failure rate due to cosmic radiation induced SEB increases if tracking systems are used in combination with photovoltaic generators with size-ratios of 1.25 or even 1.50. The inverter in these cases will have to operate above the MPP voltage very often to reduce the power from the photovoltaic generator to a level that the it can handle and thus sustain significantly higher voltage stresses. If trackers are combined with over-rated photovoltaic generators the acceptable failure rate is exceeded in may cases.

Failure rates under the assumption of significant output power curtailment

So far it was assumed that the inverter can always operate without external constraints. It has to be expected that in the real application the inverter will be required to operate with reduced active power output for certain periods. These could be situations where large amounts of reactive power need to be provided or periods during which the output power is restricted by the electricity network operator (output power curtailment). In either case the voltage stress increases. It was previously shown in [62] that the increased voltage stress due to output power curtailments significantly increases the failure rate due to SEB.

If it is assumed that the output power of a system with a size-ratio of 1.50 and a fixed tilt photovoltaic generator is curtailed as indicated in Table 4.5 the failure rates due to cosmic radiation induced single event burnout increase as shown

in Figure 4.26. As it is not possible to accurately estimate the expected level of curtailment for a given PV installation the values in Table 4.5 have to be understood as exemplary, as already discussed in [62].

Table 4.5.: Assumed (exemplary) curtailment levels to illustrate effect. (Previously shown in [62])

level of curtailment (permitted output power)	**frequency of occurrence**
no restriction	19 h / 24 h
60 % of P_{max}	4 h / 24 h
30 % of P_{max}	30 min / 24 h
10 % of P_{max}	15 min / 24 h
cease operating	15 min / 24 h

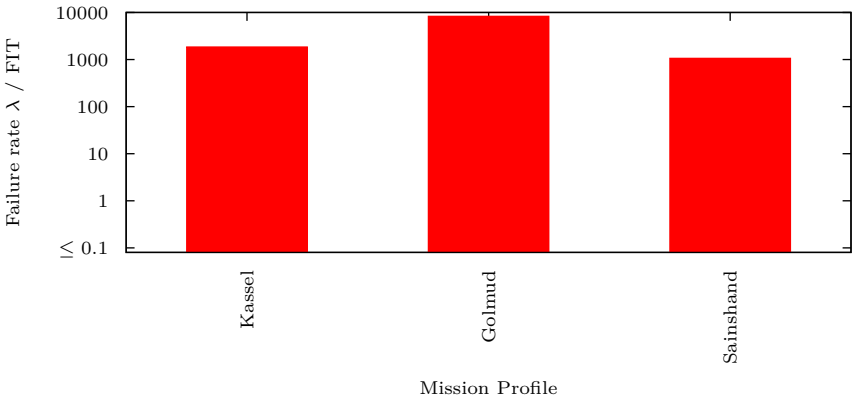


Figure 4.26.: Failure rate due to single-event-burnout. Fixed tilt PV generator, fixed size-ratio of 1.5, one-year mission profile, assumed curtailment as per Table 4.5.

The results show that whereas operation of a 1000 V inverter under ideal operating conditions may be possible with 1200 V semi-conductors the conditions that are to be expected in the application will likely lead to problematic failure rates. As a consequence 1700 V devices may need to be used in inverters for 1000 V systems. This would increase semiconductor losses but would help to avoid failures due to cosmic radiation. Alternatively, multi-level topologies can be used. However, these

also have certain disadvantages such as increased complexity and possibly higher cost and losses. Other alternatives could be the use of more robust semiconductor devices. As was shown in chapter 3, the tested SiC MOSETs are very robust and could be used in place of the Si IGBT. Also, SiC diodes or Si CAL diodes are more robust to cosmic radiation than the diode whose data was used to compute the expected failure rates in this investigation.

Each approach has certain consequences and a design decision has to be made. At this point the only definite conclusion that can be drawn is that it is essential to have accurate knowledge of the cosmic radiation robustness of the power semiconductor devices and of the stresses expected in the application to evaluate if a certain device can meet the requirements. The first point can be addressed by performing measurements such as those described in Chapter 3 or by obtaining data from semiconductor manufacturers. The latter point can be addressed by performing simulations similar to those described in this chapter. To ensure the accuracy of the voltage stress profile obtained from such a simulation it is essential to make sure that the climatic profiles are selected appropriately and that any factors that may influence the voltage stress (e.g reactive power provision or output power curtailments) are taken into consideration.

4.6. Conclusion

A simulation based on *Matlab/Simulink* that allows the stresses on photovoltaic central inverters to be investigated was developed. The simulation models the behaviour of the photovoltaic system to obtain mission profiles for the inverter and in particular the power semiconductors within the inverter from a system mission profile consisting of environmental data.

Using the developed simulation and a set of year-long mission profiles for a total of eight sun-belt locations as well as a reference location in Germany stresses on the power semiconductors in a typical photovoltaic central inverter were investigated. In particular, the temperature cycling stresses as well as the voltage stress on the devices were considered.

The investigation has shown that the thermal cycling stress at the module baseplate (case) will reach the specified limit only after a time of approximately 40 years even in the most critical locations. The most critical locations were identified as those regions with low ambient temperatures and high solar irradiance. In those locations the power electronic modules are exposed to large daily temperature

cycles which lead to a high thermal cycling load. While the predicted stresses allow operational times of up to 25 years even in challenging locations it would be beneficial to reduce this stress. Methods to do so will be investigated in the next chapter.

The results of the simulations suggest that the power cycling stress on the semiconductors in photovoltaic central inverters is not lifetime critical. However, it has to be noted that the simulation does not capture temperature cycles that occur at the semiconductors due to the output current pulsation within the fundamental period of the output current waveform (i.e. 20 ms for a 50 Hz system).

Finally, it was shown that the failure rate expected due to cosmic radiation induced single-event-burnout can exceed tolerable limits if 1200 V semiconductors are used in a 1000 V inverter and effects such as output power curtailment and / or over-sizing of the photovoltaic generator occur. To overcome these problems semiconductors of a higher voltage class or more complex multi-level topologies can be used. Alternatively, devices that are more robust against cosmic radiation induced SEB may be promising alternatives. Either way, it has become clear that it is essential to have accurate knowledge of the cosmic radiation robustness of the power semiconductor devices and of the stresses expected for the system to estimate the failure rate and to decide if the requirements can be met by a certain type of device in a specific converter topology.

5. Cooling system control strategy to reduce temperature cycling

5.1. Introduction

The investigation in the previous chapter has shown that the main cycling stress on the power semiconductor modules is caused by large daily temperature cycles between the maximum heat-sink / case temperature during the day and the minimal temperature at night. In this chapter alternative ways to control the cooling system in order to reduce these daily temperature cycles are investigated. The effectiveness in reducing the temperature cycling stress as well as the influence on the average heat-sink temperature and the extra demand in power for the cooling system of the alternative control strategies are analysed.

The methods to improve the control of the cooling system for photovoltaic central inverters were developed within the project *GigaPV*[1]. The methods were previously evaluated in a paper on the investigation of temperature stress on the power semiconductor modules in photovoltaic central inverters [61]. In addition, patent applications concerning these methods were filed [91, 92]. Here, the methods are again described and evaluated using the extended simulation described in Chapter 4.

[1] Joint research project funded by the German Federal Ministry of Education and Research

5.2. Approach to optimise cooling system control

The cooling system of a typical photovoltaic central inverter is comprised of one or more aluminium heat-sinks onto which the power electronic modules are mounted and which are cooled using forced air-convection. The intensity of the forced air cooling can be varied by changing the fan speed. The cooling system is dimensioned to ensure that at high ambient temperatures (e.g. 50 °C) the heat-sink temperature can be maintained at acceptable levels while the converter operates at nominal power. As a result, the cooling system is not operated at full power if the ambient temperature remains below the maximum specified ambient temperature.

Typically, the cooling system is controlled in order to maintain the heat-sink at a fixed pre-set temperature and to reduce the cooling power if the ambient temperature is below the specified maximum temperature or if the inverter is only partially loaded and the losses in the semiconductors remain below the maximum level. This control strategy has the advantage that only the minimal amount of power is used for the cooling fan at any time but as a consequence the pre-set heat-sink temperature (e.g. 80 °C or 90 °C) is reached even on cold days with little solar irradiance which leads to large temperature cycles for the power semiconductor modules.

Two alternative methods to define the set-point of the cooling system control in order to avoid large temperature cycles on days with low solar irradiance and/or low ambient temperatures were considered.

5.2.1. Option A: Incremental set-point adjustment

For this approach the initial set-point for the cooling system control is set to a value just above the ambient temperature each time the inverter system starts operating. The set-point is then increased incrementally if the control system notices, that the cooling system is fully utilised for a certain period of time.

The simulation results in Figure 5.1 illustrate the strengths and weaknesses of this method. It can be seen that on days with low solar irradiance and hence low losses in the power semiconductors the size of the daily temperature cycle is reduced significantly. On days with high solar irradiance the size of the daily temperature cycle can not be reduced significantly since larger losses are dissipated in the power semiconductors. This shows the main disadvantage of this method. On days with large solar irradiance the incremental increase of the set-point in the first half of the day results in an unnecessary use of energy for the cooling system.

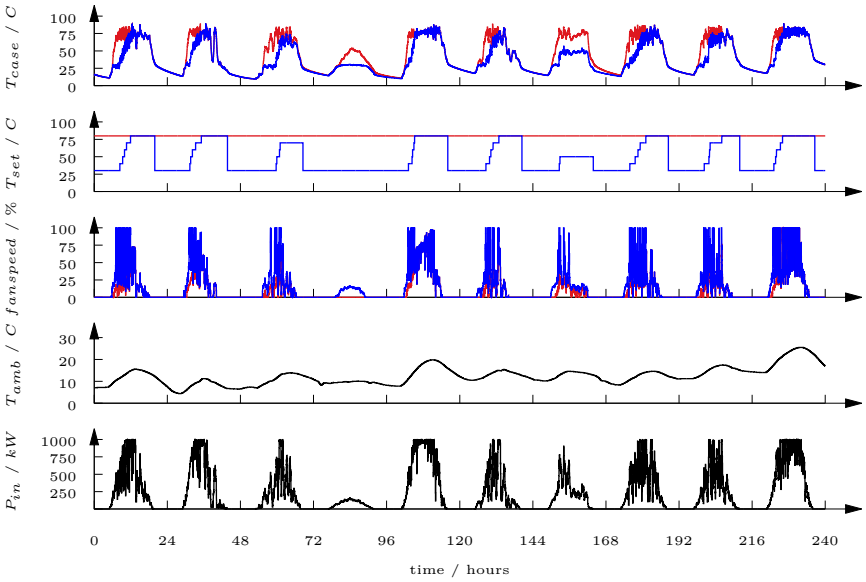


Figure 5.1.: Simulation with incremental set-point adjustment. Red: Control with fixed set-point, Blue: Control with incremental set-point adjustment. Size-ratio 1.5, Kassel, fixed module installation.

5.2.2. Option B: Use of prognosis to determine daily set-point

This second approach can be seen as an extension of the previously discussed incremental set-point adjustment strategy. In order to avoid using large amounts of energy for the cooling system during the first half of the day an initial cooling system set-point temperature can be determined from a prognosis of the expected daily peak energy available from the PV generator. From the prognosis the expected peak losses of the inverter can be estimated and an initial cooling system set-point temperature that is a good compromise between cooling system utilisation and heat-sink temperature can be determined. If the selected initial set-point turns out to be too low and the cooling system is constantly heavily utilised the set-point is incremented as discussed for Option A.

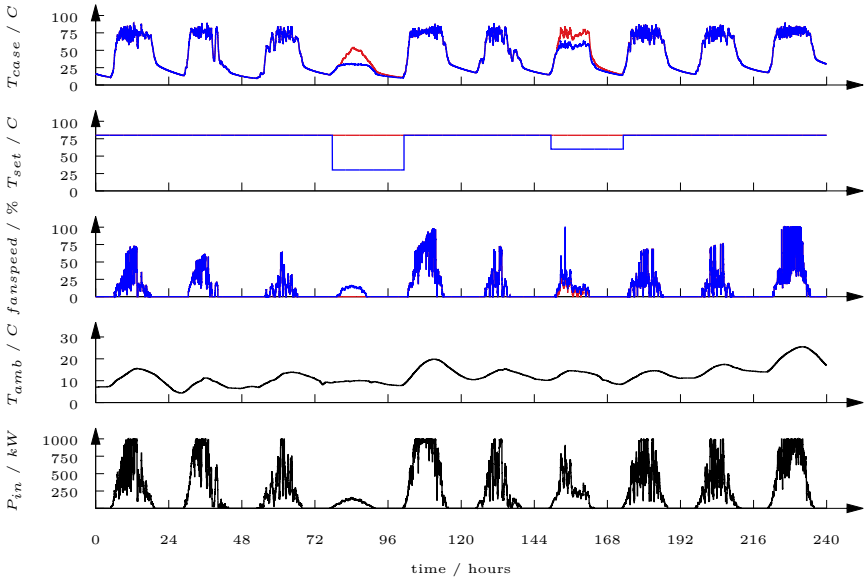


Figure 5.2.: Simulation with incremental set-point adjustment and use of prognosis data for daily initial set-point estimation. Red: Control with fixed set-point, Blue: Control with incremental set-point adjustment. Size-ratio 1.5, Kassel, fixed module installation.

In Figure 5.2 simulation results that make use of this method are shown. To obtain a prognosis for this simulation an initial simulation was run to determine the peak PV power for each day of the simulated time frame. In the application it

is expected that prognosis data for large photovoltaic power systems is available that could be used.

The simulation results in Figure 5.2 show that this approach avoids slowly ramping up the heat-sink temperature set-point during the first half of days with large solar irradiance but still succeeds in reducing the daily temperature cycle for days with low solar irradiance. This method is therefore preferable over Option A, as it provides a reduction of the temperature cycling stress at a minimum of additional energy use.

5.3. Comparison of cooling system control strategies

In the simulation used to investigate the stresses on the semiconductors in photovoltaic central inverters (see Chapter 4) the standard approach was followed and a fixed set-point for the cooling system control of 80 °C was used. As was shown this results in the largest thermal cycling stresses in locations with the lowest ambient temperatures.

The effect of using the two alternative strategies to determine the set-point for the cooling system control proposed above on the temperature cycling stress as well as the average stack temperature and the energy use for the cooling system is investigated. For that purpose the simulations that were described in Chapter 4 for the nine locations were repeated with both proposed strategies of determining the cooling system set-point.

5.3.1. Temperature cycling stress

In Figure 5.3 the temperature cycles occurring for the mission profile for Kassel with a photovoltaic generator with fixed modules and a size-ratio of 1.5 are shown.

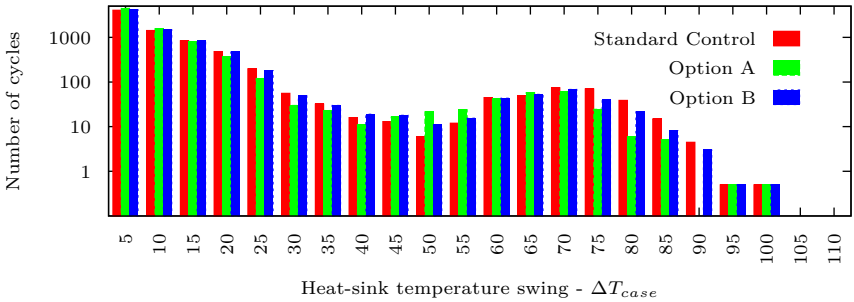


Figure 5.3.: Distribution of temperature cycles for different strategies of selecting the cooling system set-point. Mission Profile: Kassel, PV generator with fixed modules, size-ratio 1.5.

As can be seen the number of cycles larger than 70 K is reduced and more cycles are present in the range of 45 to 55 K if either of the two strategies described above is used. In the diagram in Figure 5.4 the contribution of the cycles with different amplitude to the damage factor is shown.

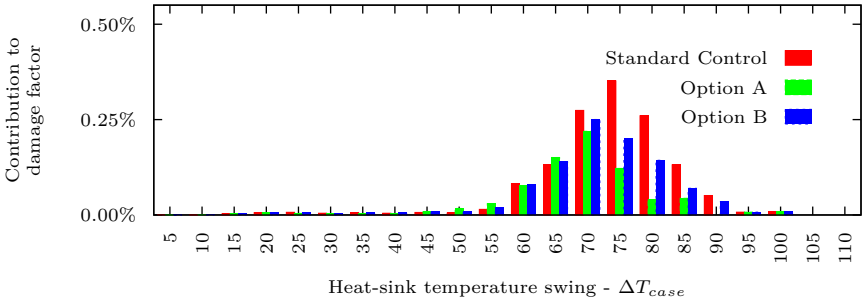


Figure 5.4.: Contribution of temperature cycles to the temperature cycling damage factor for different strategies of selecting the cooling system set-point. Mission Profile: Kassel, PV generator with fixed modules, size-ratio 1.5.

The distribution of damage factor contribution across the temperature swing shown in Figure 5.4 illustrates that the reduction in large temperature cycles leads to a significant reduction in damage factor because the large temperature variations are much more damaging for the module.

The effect on the overall damage factor due to temperature cycling is shown in Figure 5.5 for the locations investigated in Chapter 4. As can be seen the stress in the predicted damage factor reduces significantly in the locations that previously showed the highest values for the damage factor. Both methods are therefore suitable to reduce the stress due to temperature cycling in the regions with the highest stress.

,

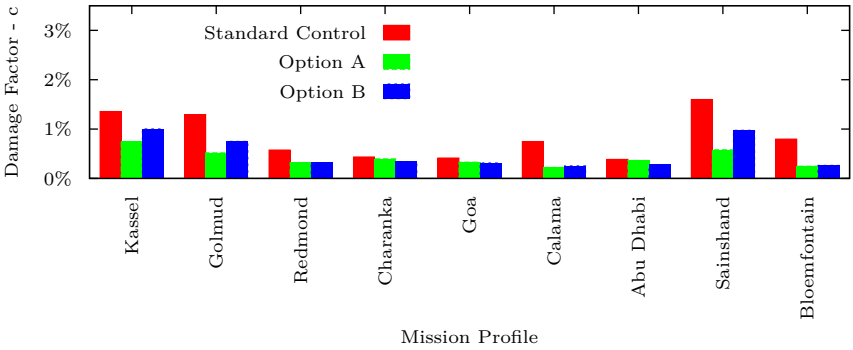


Figure 5.5.: Thermal cycling damage factors for the studied locations using different cooling system control strategies. A photovoltaic generator with size-ratio 1.5 and fixed installation of modules is assumed.

5.3.2. Average stack temperature

In Figure 5.6 the distribution of operating hours over the heat-sink temperature is shown. It can be seen that the adaptive control methods lead to less operating time at high temperatures ($> 70\,\mathrm{K}$). This is beneficial for all components that are exposed to the heat-sink temperature (e.g. the gate-drive subsystem), as many failure mechanisms are accelerated by temperature.

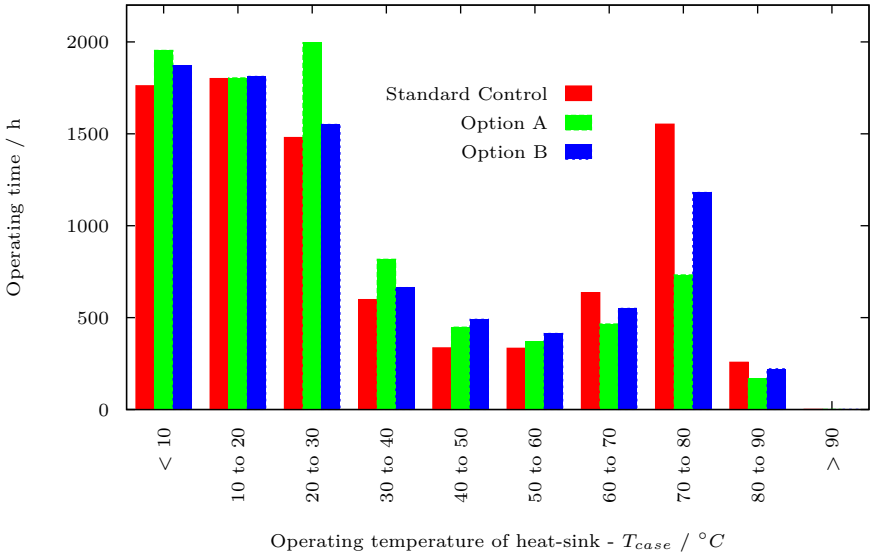


Figure 5.6.: Heat-sink temperature distribution for different cooling system control strategies. Mission profile: Kassel, fixed tilt PV generator, size-ratio 1.5.

The average temperature of the stack in the example shown above decreases by around 6 °C if Option A is used instead of the standard approach. Due to the exponential nature of the Arrhenius equation, which is frequently used to model the temperature dependency of failure mechanisms, even this small reduction in average temperature can lead to a significant reduction in the failure rate of components that are exposed to the stack temperature.

5.3.3. Energy utilisation for cooling system

To estimate the additional energy used by the cooling system if the proposed control strategies are adopted a histogram of the operating time at different fan-speed settings, as shown in Figure 5.7, was created for every location.

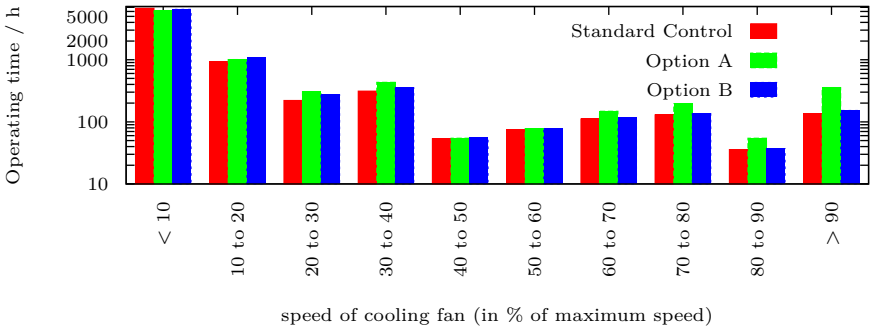


Figure 5.7.: Distribution of operating hours over fan-speed. Mission profile: Kassel, PV generator with fixed modules, size-ratio 1.5.

Using the data in the histogram and information about the power requirement of the cooling fan at different fan-speed settings the overall energy utilised for the cooling system can be estimated. In Figure 5.8 the increase in cooling energy over a one-year mission profile for each location is shown.

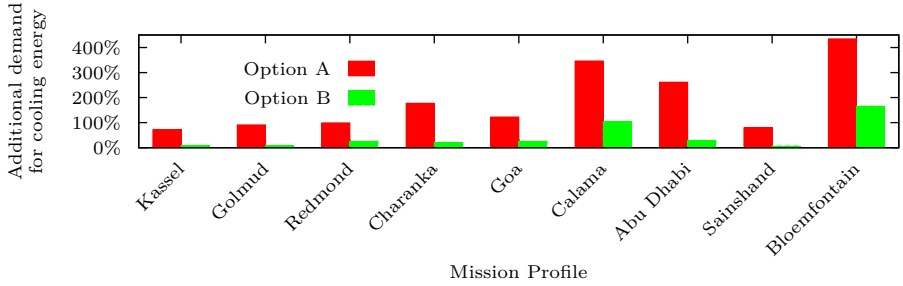


Figure 5.8.: Additional cooling energy required for different cooling system control strategies in the various locations. Compared to default solution. PV generator with fixed modules, size-ratio 1.5.

The results show, that Option B uses significantly less additional energy than Option A in all investigated locations.

5.4. Conclusion

Two alternative methods that can be used to adjust the heat-sink temperature set-point of the cooling system controller for photovoltaic inverters were presented. Instead of using a fixed set-point for the heat-sink temperature during all periods of inverter operation these methods adjust the heat-sink temperature set-point during each day to minimise the daily temperature cycles that the power semiconductor modules are exposed to.

It was shown, that both methods are effective in reducing the temperature cycling stress on the power semiconductors. Additionally, the average temperature of the heat-sink on which the power semiconductor modules are mounted is reduced, which is a further benefit to reliability, as most components' failure rates increase with temperature.

Furthermore, it was shown that the suggested 'Option B', which makes use of prognosis data to find the initial daily set-point, uses very little additional cooling system energy. Implementing this option in large photovoltaic inverters therefore comes at very little additional cost, as it can be assumed that prognosis data will be available for large photovoltaic installations.

6. On-line temperature measurement of IGBTs

6.1. Introduction

Condition monitoring can help to avoid expensive downtimes and reduce the cost of unscheduled maintenance. Information about the state of health of critical components can be used to schedule maintenance before a fault occurs. Such information is particularly useful if energy conversion systems are deployed in inaccessible regions far away from the next support centre or if downtimes may cause high costs e.g. in the case of faults in the energy distribution system.

In power electronic converters there are many components that undergo ageing and that can be monitored. Examples for components that may age are the IGBT modules and energy storage capacitors in the DC link. In this chapter the focus is on temperature monitoring of the IGBTs.

In this chapter a brief comparison of temperature sensitive electrical parameters (TSEPs) of IGBTs regarding their suitability for use in an on-line temperature measurement system is provided. The implementation of a basic IGBT gate-driver circuit that enables on-line temperature monitoring by measuring the turn-off delay is then shown. The functionality of the implemented gate-drive circuit is demonstrated in a scaled laboratory set-up of a three-phase inverter.

The implemented turn-off delay measurement circuit described in this chapter as well as the measurements performed using this circuit in a laboratory set-up of a three-phase inverter were already presented in [93].

The work presented in this chapter was performed as part of the research project *GigaPV*[1]. As a starting point for the work presented in this chapter information from an internal project that focused on indirect temperature sensing of chip temperatures of SiC devices including a comparison of TSEPs was available [94].

[1] Joint research project funded by the German Federal Ministry of Education and Research

6.2. Methods to measure IGBT temperatures

Several methods can be used to measure the temperature of semiconductor chips. As discussed by Blackburn in [95] these approaches can be grouped as *electrical*, *optical* or *physical contact* methods.

An example for a method that relies on *physical contacting* is the attachment of temperature sensors such as thermocouples to the semiconductor chip. While good spatial resolution is achievable if very small sensors are used [95] the main disadvantage is that the probes have to be attached to the device surface. Standard IGBT modules do not contain such sensors and hence this approach would require the modification of IGBT modules which is not desirable. Also, temperature variations during the output waveform period can not be resolved due to the time constant of the sensors as was shown in [96] for the example of K-type thermocouples and also mentioned in [95]. Finally, issues with the electrical signal isolation need to be addressed if sensors are placed in close proximity to the power semiconductors. The use of thermocouples is therefore not suitable for continuous monitoring of chip temperatures in a power converter.

Infra-red thermography is an example for the *optical* methods suggested in [95]. This method has the advantage of providing high spatial resolution and allowing fast temperature transients to be measured. However, chip temperatures of IGBT modules can be measured using infra-red thermography only if the modules are opened, the isolating silicone gel is removed and a suitable surface coating is applied to obtain a good emissivity. While this is a viable method for validation of thermal models in the lab the price of infra-red thermography systems and the requirement to have a clear line of sight to the semiconductor chips rules out this option for implementation as part of a condition monitoring system.

Since both *optical* and *physical* methods are unsuitable for the temperature measurement of IGBTs in standard power modules an *electrical* method that helps to indirectly determine the chip temperature by measuring readily accessible TSEPs needs to be found. While electrical methods based on TSEPs can be applied without making modifications to the semiconductor in their packaging the main disadvantage is that they only provide a single 'lumped' value for the measured temperature while there may be a spatial temperature distribution that can not be determined through these *electrical* methods [95]. Also see [97] for information on the relationship between the single temperature obtained from an electrical measurement (of $V_{CE}(T)$ at a small sense current in this case) and the temperature distribution on the chip.

6.3. Temperature sensitive electrical parameters of power semiconductors

In this section a number of the TSEPs that are discussed in literature [94–110] are briefly compared to assess their suitability for use in an on-line temperature monitoring system.

An ideal TSEP for use during converter operation should provide a high temperature sensitivity to allow an acceptable temperature resolution in the range of e.g. 1 K to be reached without requiring an excessively high measurement resolution. Additionally, it is desirable that the TSEP has a linear temperature dependency and that the sensitivity and absolute value are comparable between devices of the same type to minimise the calibration effort. Furthermore, it is beneficial if few additional parameters that vary during converter operation (e.g. V_{ce}, I_c) influence the TSEP. This is particularly important if these parameters are not already known to the control system typically implemented in a power converter. Finally, it is essential that the TSEP itself can actually be measured without making major modifications to the power converter and without needing to change the way that the power converter is operated.

6.3.1. Collector-emitter saturation voltage

One TSEP of IGBTs that is very frequently discussed in literature [98, 101, 104, 105] is the forward voltage across the device. This TSEP is often used with a small measurement current to characterise the thermal performance or to perform lifetime tests on power semiconductors in the lab [104, 105].

The temperature dependency of the forward voltage can be considered to be linear, if a suitable value for the small measurement current applied to the IGBT is selected. Measurements were conducted on a state of the art IGBT and the results plotted in Figure 6.1 confirm the linearity of this TSEP. The observed sensitivity lies in the range of -1.4 to $-2.4\,\mathrm{mV\,K^{-1}}$ depending on the sense current.

While using a small measurement current is a viable option when characterising a power module (e.g. to measure cooling curves to determine thermal impedances) it is not feasible to apply a small sense current to a device in the on-state during converter operation.

If the forward voltage is to be used as a TSEP during converter operation it will have to be measured while the load current is applied to the device. As can be

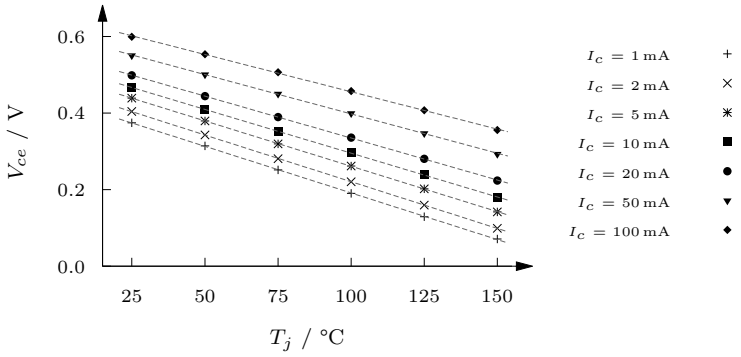


Figure 6.1.: Measured V_{ce} of IKW40N120H3 at small collector currents I_c.

seen from Figure 6.2 the sensitivity of the forward voltage to temperature changes as the load current is varied. For small currents a negative temperature coefficient is expected while for large currents the temperature coefficient is positive.

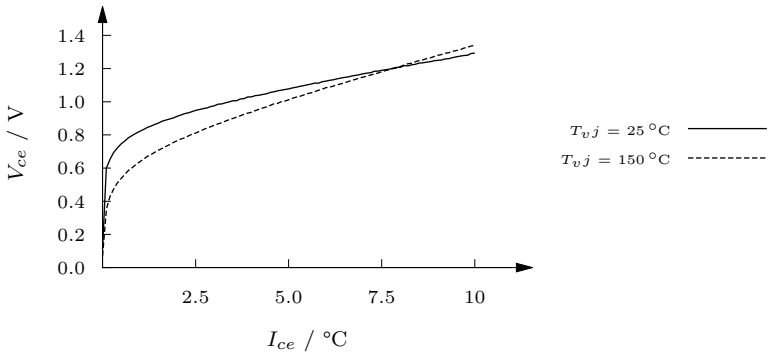


Figure 6.2.: Measured V_{ce} of IKW40N120H3 at larger collector currents I_{ce} for different temperature.

This changing temperature coefficient with current is a consequence of the structure of the IGBT. The forward voltage of the IGBT $V_{F,IGBT}$ is the sum of the voltages across the PN-junction at the collector and the MOS-channel [111, p. 779]. These components have different temperature coefficients. As a result the

overall temperature coefficient depends on the current flowing in the device as well as the design of the IGBT.

The varying sensitivity with output current requires very accurate voltage sensing to implement a temperature measurement system based on this TSEP as well as very accurate current sensing.

In addition to the changing sensitivity with the load current the influence of the temperature dependency of the resistivity of the electrical connections such as the bond wires can not be neglected for high collector currents. The measured temperatures at large collector currents can be inaccurate as the temperature of the electrical connections and hence their resistivity is different during the calibration and the operating condition as discussed by Dupont and Avenas in [105]. In the same paper the authors discuss two approaches for measuring the forward voltage under different conditions to overcome this issue. One approach measures the forward voltage at different gate voltages. The other approach requires measurements at two collector current values.

For this investigation the methods based on the forward voltage of the IGBT were not considered further, as the sensitivity is too current dependent and the methods that require changing gate voltage or collector current were considered too complex.

6.3.2. Internal gate resistance

The use of the internal gate resistance to sense the IGBT chip temperature is discussed by Brekel et. al. in [96] and compared to temperature measurements using a thermocouple, an IR-camera and an IR-sensor.

The authors of [96] were able to perform temperature measurements on a 6.5 kV IGBT chip with good accuracy and high time resolution by measuring the temperature dependent resistivity of the internal gate resistor.

The main downside of this methodology is that contacts to the internal gate resistor need to be accessible in order to implement an on-line temperature measurement system that makes use of this TSEP. Since typical IGBT modules that were considered in this investigation do not provide access to the internal gate resistance this TSEP was not considered further.

6.3.3. Threshold voltage

In literature (e.g. [111]) the threshold voltage is formally defined as the gate voltage at which a strong inversion layer is formed and hence a channel that can conduct significant currents forms. The threshold voltage as a TSEP along with approaches to measure it during converter operation is discussed in [103, 107]. For the purpose of this investigation the threshold voltage was considered as the gate voltage above which a collector-emitter current of 1 mA starts to flow in the IGBT. As the measurement results in Figure 6.3 show the sensitivity of this quasi threshold voltage as a TSEP for the tested device is approximately $-12\,\mathrm{mV\,K^{-1}}$.

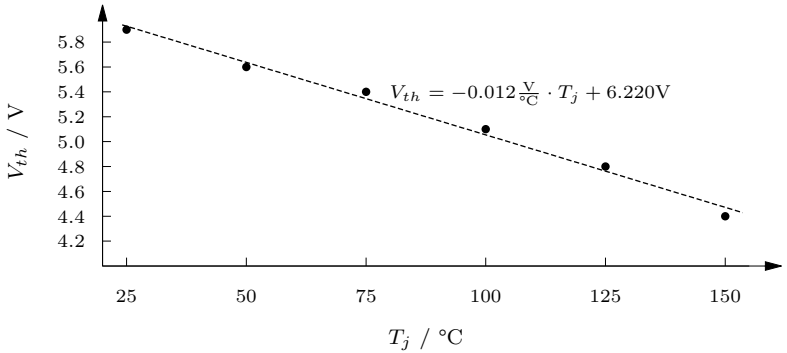


Figure 6.3.: Measured V_{th} of IKW40N120H3 (V_{CE} set to 10 V, increased V_{GE} until I_{DS} of 1 mA flowed.)

The benefit of this TSEP is that it is largely independent of the current [103]. To measure the threshold voltage during converter operation it is necessary to detect the onset of current flow during turn-on of the IGBT and accurately measure the gate-voltage at that point with minimum delay.

6.3.4. Switching delay times

The authors of a number of publications [98, 100, 102, 103, 107] discuss the temperature dependence of both the turn-on delay time $t_{d,on}$ as well as the turn-off delay time $t_{d,off}$ of IGBTs.

The turn-on delay time has the advantage of not being influenced by the switched current, but only the voltage prior to turning-on the device [98, 102]. However, the disadvantage is that very low sensitivities of the turn-on delay time to temperature are reported in some publications [100, 103]. This is also confirmed by looking at datasheets of a typical discrete IGBT and an IGBT module [82, 112]. In these datasheets very low sensitivities to temperature of the turn-on delay are mentioned, while the sensitivity of the turn-off delay $t_{d,off}$ to temperature is in the range of 0.5 to $0.8\,\mathrm{ns\,K^{-1}}$.

The disadvantage of the influence of the switched current on the turn-off delay should not be problematic in most applications of an on-line temperature monitoring system, as the current is known from current measurements that are required for controlling the converter. The turn-off delay time is thus favoured over the turn-on delay time, as higher temperature sensitivities are expected for the devices considered in this investigation.

The switching delay times, in particular at device turn-off, are considered to be a suitable TSEP for building an on-line temperature monitoring solution, since only the time between two events needs to be measured. It is expected that including the necessary components around the gate-drive circuit can be achieved with reasonable effort to permit temperature measurements with a resolution of 1 °C or better.

6.3.5. Switching transients

The switching speed of IGBTs (in particular the di/dt) is dependent on temperature as discussed in [99]. In principle the switching speeds can therefore be used to determine the device temperature.

However, the sensitivity of the rates of change of current and voltage to temperature are expected to be relatively low and also depend on the operating point (switched current and voltage as well as gate voltage). Approaches that could be followed to measure the di/dt and dV/dt are provided in [113]. One approach that makes use of the stray inductance between kelvin-emitter and power terminal to sense the di/dt and hence measure the device temperature is provided in [108].

It is expected that significant effort is required to sense the switching speeds with a sufficient accuracy to measure the device temperature. Also, not in all cases are kelvin-emitters available to use the method described in [108]. Therefore, the switching transients were not considered further as a TSEP in this investigation.

6.3.6. Summary

On the last few pages a number of TSEPs of IGBTs were discussed. A short summary of their advantages and disadvantages in the application of an on-line temperature monitoring system is given in Table 6.1.

Sensing the chip temperature using the collector-emitter voltage $V_{ce,sat}$ with a small measurement current I_C is a good solution for offline applications i.e. while the chip is not operated within a power converter. This is the case if thermal paths are characterised or if power cycling tests are conducted. For online applications this TSEP is not suitable as it is not possible to let a well defined and small measurement current flow in the device while the converter is operating.

For on-line temperature monitoring the most suitable TSEPs are considered to be the threshold voltage V_{th} and the turn-off delay time $t_{d,off}$. In fact, previous implementations of on-line temperature sensing systems based on these TSEPs are mentioned in literature and a few examples are referenced below.

- In [107] and [103] the threshold voltage is used as a TSEP in an on-line temperature monitoring system.
- In a patent application publication published in 2013 [109] a set-up and a methodology to determine the junction temperature of a semiconductor device based on measuring a switching delay time and the device forward voltage in the on-state is described.
- A TSEP not previously discussed here, but closely related to the switching delay times (the width / duration of the miller plateau) is used in [106, 110].

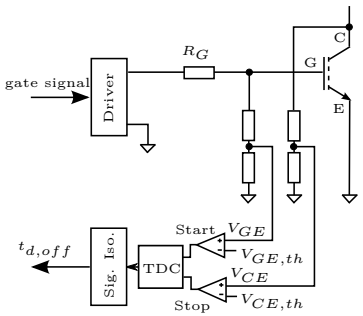
Table 6.1.: Summary of qualitative comparison of IGBT TSEPs

TSEP	**Advantages**	**Disadvantages**	**Suitability for on-line temperature sensing**
$V_{ce,sat}$ (small I_C)	• good linearity • no other influencing parameters	• requires a small sense current in the on-state	not feasible to implement
$V_{ce,sat}$ (large I_C)	• can use load current	• accurate measurement of I_C necessary • sensitivity depends on I_C • influenced by temperature changes of bondwires etc.	high implementation effort
$R_{G,int}$	• good linearity • sufficient sensitivity	• requires access to internal gate resistor	not feasible with standard modules / devices
V_{th}	• good linearity • good sensitivity	• timing for measurement of V_{ge} at the instance I_C starts to flow is critical	promising option
$t_{d,on}$ / $t_{d,off}$	• good linearity • sufficient sensitivity ($t_{d,off}$)	• dependency on I_C and V_{CE} • accurate time measurement required	promising option
switching speed		• high effort to measure di/dt or dV/dt • sensitivity and linearity unclear	if at all possible a high implementation effort is expected

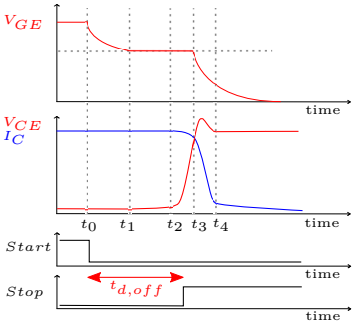
6.4. Gate-drive circuit with turn-off delay measurement

Based on the comparison of various temperature sensitive electrical parameters of IGBTs in the previous section it was decided to implement an on-line temperature monitoring solution based on the turn-off delay time as a TSEP. To realise the on-line temperature monitoring a measurement circuit to sense the turn-off delay with minimum effort in terms of additional components was developed.

In order to measure the turn-off delay of an IGBT two tasks need to be addressed. First of all, the beginning and end of the turn-off delay time need to be detected. This was achieved using a two-channel comparator. The collector-emitter and gate-emitter voltages are compared with constant voltage thresholds corresponding to approximately 50 V and 13 V, respectively. A falling edge on the start signal is thus generated when the gate voltage falls below 13 V and a rising edge on the stop signal is generated when the collector emitter voltage rises above 50 V as illustrated in Fig. 6.4.



(a) Measurement circuit extending IGBT gate-drive circuit.



(b) Start and stop signals generated from voltage transients during IGBT turn-off. IGBT transients are based on those shown in [114, p.564].

Figure 6.4.: Gate-drive circuit with turn-off delay measurement.

Once the *start* and *stop* signal have been generated the delay between both signals needs to be measured. For this measurement a resolution in the region of 0.1 ns is required in order to achieve a temperature resolution in the order of 1 K, as

the expected sensitivity of the measured turn-off delay to temperature lies in the range of 0.5 to 0.8 ns K^{-1} as discussed in the previous section.

To measure time intervals with resolutions in the area of 0.1 ns using a simple counter a clock frequency of 10 GHz would be required and this is not feasible. However, many strategies to accurately measure short time intervals with high resolution exist. Reviews of such techniques can be found in [115–117].

After briefly considering to built a discrete circuit for performing the time measurements such as that presented by Fontanelli et. al. in [118] it was decided to use a commercially available solution for the time measurement to avoid having to characterise and calibrate a sensitive circuit. For the implementation of the IGBT turn-off delay measurement the TDC-GP22 manufactured by acam-messelectronic GmbH which offers a time resolution of 90 ps or better and a range of 3.5 ns to 2.5 µs was used [119].

A block diagram of the measurement circuit which was implemented to measure the IGBT turn-off delay during converter operation is shown in Fig. 6.5. All digital communication signals are isolated to allow the driver-circuit to be used to drive IGBTs at a floating potential.

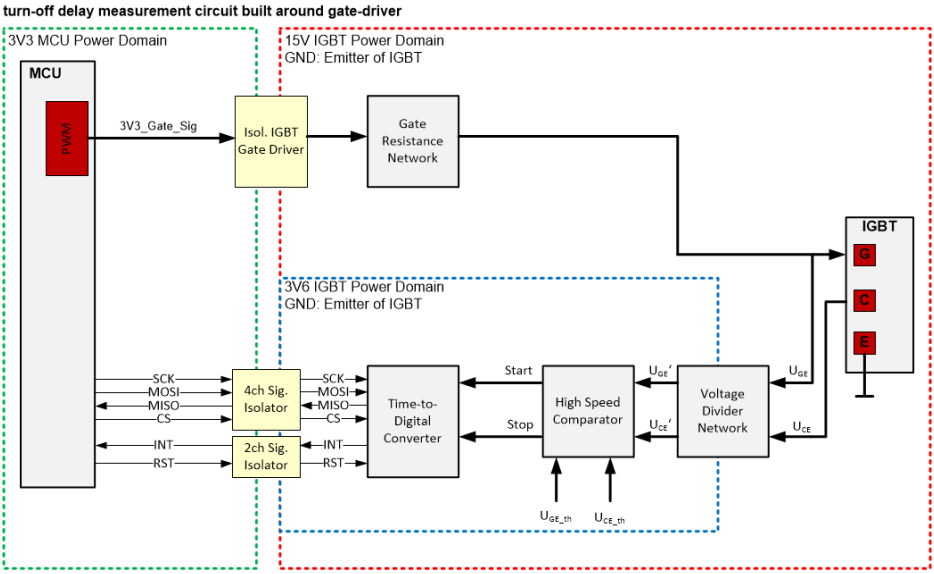


Figure 6.5.: Block diagram of IGBT gate driver with turn-off delay measurement

The time to digital converter (TDC) is configured to measure the time between the falling edge on the *start* signal and the rising edge on the *stop* signal. Completion of the conversion process is indicated by the TDC through an interrupt. Upon receiving the interrupt signal the control system reads the turn-off delay time from the TDC using the SPI bus, which is also used to configure the device.

The gate-driver with the measurement circuit described above was implemented on a small PCB, shown in Fig. 6.6. These gate-driver PCBs were used to conduct the turn-off delay measurements described in the next sections.

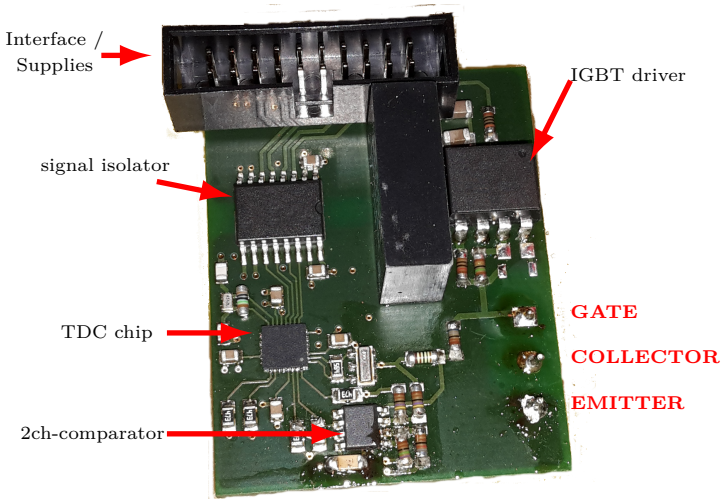


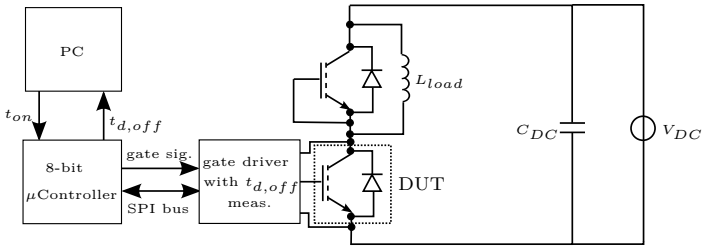
Figure 6.6.: PCB with IGBT driver and circuitry for turn-off delay measurement (further components on bottom side of PCB).

6.5. Experimental investigation of turn-off delay as a TSEP of IGBTs

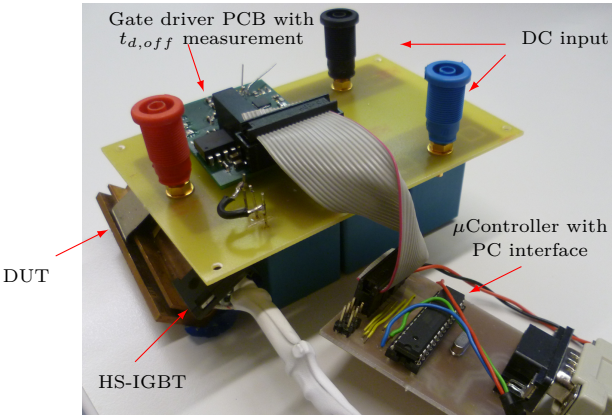
In order to test the gate-drive circuit presented in the previous section and to further investigate the feasibility of using the turn-off delay as a TSEP for on-line temperature monitoring a number of measurements were performed on discrete IGBTs.

6.5.1. Measurement of turn-off delay of a single IGBT

To identify the sensitivity of the turn-off delay measurement with the implemented measurement circuit to temperature and other influencing factors (I_C,V_{DC}) a set of measurements was performed using a typical state-of-the-art discrete IGBT (1200 V,40 A). Single pulses were applied to the device-under-test in a simple set-up as shown in Fig. 6.7.



(a) Principal circuit used to test the turn-off delay measurement and perform measurements on a discrete IGBT. DUT (Low-side IGBT) is placed on a hot plate for measurements at different temperatures.



(b) photo of setup

Figure 6.7.: Experimental set-up used to conduct turn-off delay measurements on a discrete IGBT at different temperatures, switched currents and voltages.

The duration of the pulses was selected to switch off the DUT at different collector currents I_C in the range of 1 to 25 A. The measurements were performed at different temperatures and for different supply voltages V_{DC} of 400 to 800 V.

In Fig. 6.8 the voltage and current transients of a turn-off event at 25 A and a DC voltage of 400 V are shown along with the generated *start* and *stop* signals.

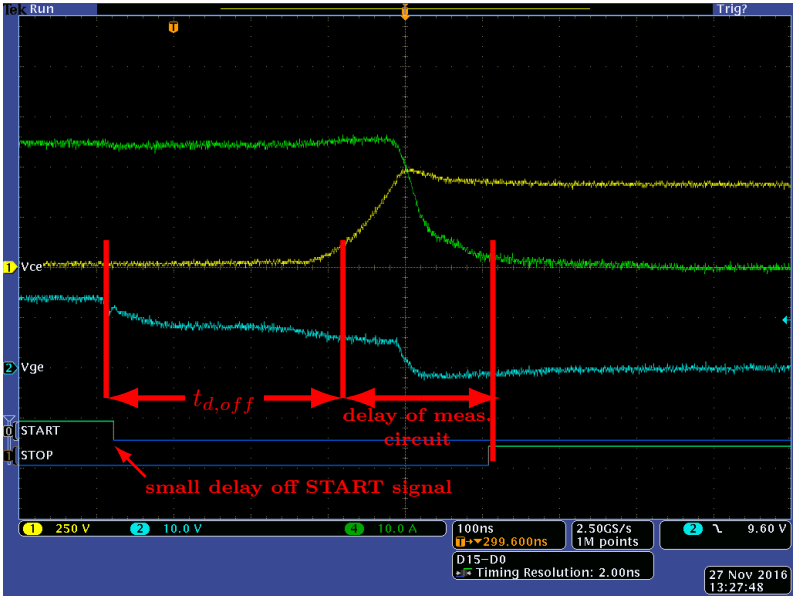


Figure 6.8.: Transient signals for turn-off at 25 A, 400 V, 100 °C, $R_g = 15\,\Omega$.

As can be seen from the plot, the falling edge of the *start* signal marks the time at which the gate voltage V_{GE} starts to fall with only a small additional measurement delay. The rising edge of the *stop* signal lies approximately 180 ns after the collector-emitter voltage V_{CE} rises above the threshold value. The time between the two events is measured by the TDC and communicated to the PC via the micro-controller.

The additional delay between the rise of the collector-emitter voltage and the *stop* signal is attributed to the parasitic capacitances within the voltage divider that reduces the collector-emitter voltage to a level that can be handled by the comparator. The resistances in the voltage divider have to be high enough to limit the current to a value that gives acceptable losses. However, if the resistances are high, the small parasitic capacitances present in the resistive

voltage divider become relevant and introduce an additional delay until the rise in V_{CE} is sensed by the comparator. This has to be considered if the described delay time measurement is to be implemented in a converter system. The circuit either has to be redesigned to minimise the delay of the measurement circuit or the delay has to be taken into account in the calibration of the measurement system.

In Fig. 6.9 the measured turn-off delay is plotted as a function of temperature for different operating points (I_C, V_{DC}). The results confirm, that the turn-off delay times measured using the developed circuit are temperature dependent. The absolute values of the measured turn-off delay times are higher then expected due to the extra delay introduced to the measurement by the voltage divider circuit.

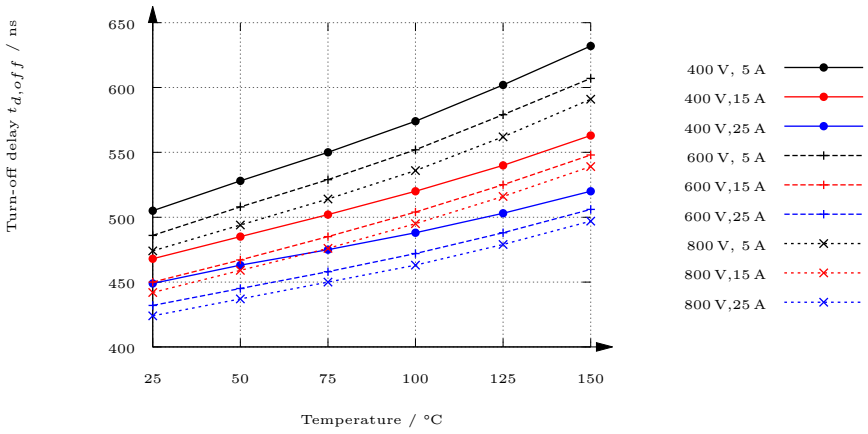
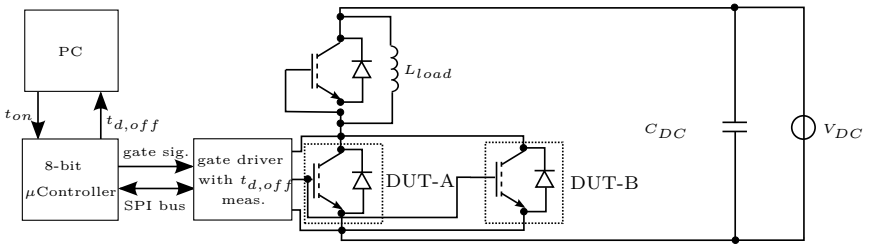


Figure 6.9.: Turn-off delay of an IKW40N120H3 measured with implemented circuit ($R_g = 15\,\Omega$).

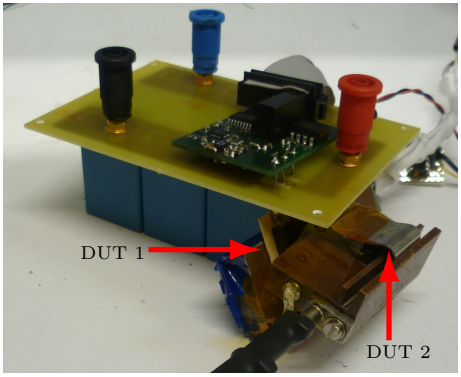
The results also show that the temperature dependency varies between $0.5\,\mathrm{ns\,K^{-1}}$ and $1.0\,\mathrm{ns\,K^{-1}}$ with changing collector current. Additionally, the absolute value of the turn-off delay measured by this measurement circuit depends on the switched current and to a lesser extend on the supply voltage. The dependency on the voltage may have to be attributed to the measurement system. These results suggest that knowledge of the switched current and voltage is required in order to obtain the device temperature from the measured turn-off delay time.

6.5.2. Turn-off delay of parallel IGBTs with different temperatures

In high power applications it is common to place multiple IGBT chips in parallel (e.g. in large IGBT power modules) to achieve the desired power rating. Even though these power modules are optimised by the manufacturers some differences in the chip temperature of paralleled chips can be expected. To investigate how the turn-off delay behaves if multiple IGBTs chips, which may not have the same temperature, are connected in parallel another set of measurements was taken. This time two IGBTs were placed on two independent hot plates to set different operating temperatures, as illustrated in Fig. 6.10.



(a) Principal circuit used to perform measurements on two parallel discrete IGBTs. DUT-A and DUT-B are placed on two hot plates for measurements at different device temperatures.



(b) photo of setup

Figure 6.10.: Experimental set-up to conduct turn-off delay measurements on two DUTs at different temperatures

Figure 6.11 shows the measured turn-off delay for the case in which both IGBTs were heated to the same temperature as solid lines and the measured turn-off delay for the case of one IGBT being kept at around 25 °C while the second IGBT was heated to the indicated temperature as dashed lines.

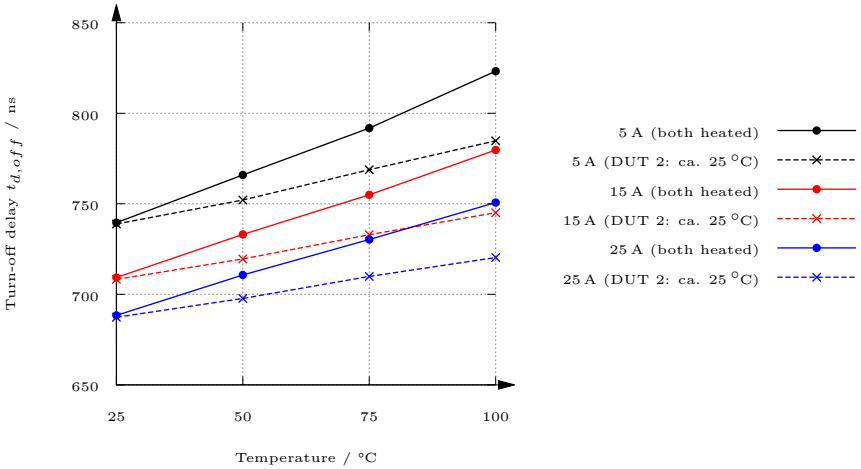


Figure 6.11.: Turn-off delay measurement of parallel devices (one gate resistor $R_g = 15\,\Omega$ for both devices).

It can be seen from the data in Figure 6.11 that the measured turn-off delay time is lower if only one device is heated and the second device remains at approximately 25 °C. This suggests that an average turn-off time is measured. Hence, in the application an average temperature of two devices at different temperatures would be measured. It would be desirable if the temperature of the hottest device were measured, however, depending on the application an average temperature is acceptable.

6.5.3. Turn-off delay of an IGBT in a large power module

In order to show that similar dependencies of the turn-off delay on temperature and the switched voltage and current exist in large power electronic modules a set of measurements was conducted on a power stack in which two 1200 V / 1400 A primepacks (FF1400R12IP4) are installed. The measurement was conducted by warming up the heat-sink to achieve different device temperatures and by applying a number of pulses of varying length to the IGBTs to measure turn-off delays at different turn-off currents. The turn-off delay was measured using an oscilloscope, as the driver circuit shown above can not drive these large power modules.

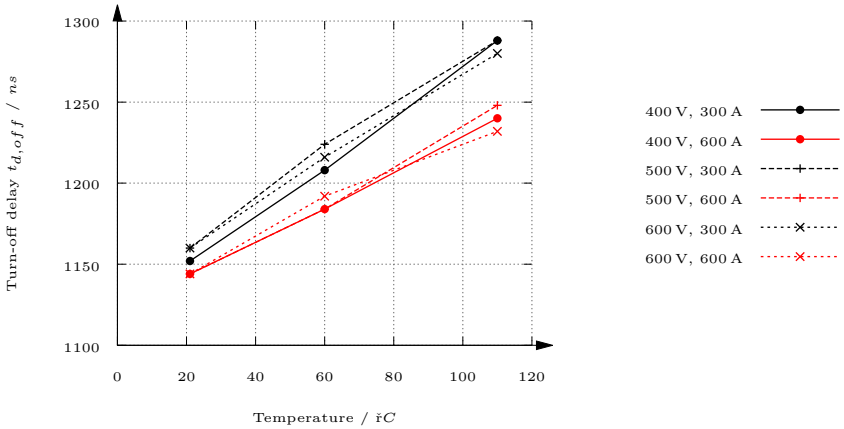


Figure 6.12.: Turn-off delay of PrimePack module

The measurement results shown in Fig. 6.12 illustrate that the temperature dependency of the turn-off delay of the IGBTs in the power module is similar to the temperature dependency observed for a discrete IGBT. The temperature dependency lies in the range of $1.0\,\mathrm{ns\,K^{-1}}$ and $1.5\,\mathrm{ns\,K^{-1}}$ and is therefore higher than for the smaller discrete devices. The result suggests that temperature sensing based on the turn-off delay can be implemented for large IGBT modules as well, if the measurement circuitry is implemented in a driving circuit capable of driving larger modules.

6.6. Implementation of IGBT temperature monitoring in a three-phase inverter

To demonstrate that the described method of on-line temperature measurement can be used during operation of a switching converter a three-phase inverter with a two-level full-bridge topology was set up.

The inverter was built around a 50 A sixpack IGBT module[2] without the usual silicone gel filling in order to enable infrared measurements of the semiconductors to be taken. The open IGBT module can be seen in the picture in Fig. 6.13 along with the sensing circuitry, the DC-link capacitance and the gate-drive circuitry. For one low-side IGBT the driver circuit with the capability to measure the turn-off delay was used.

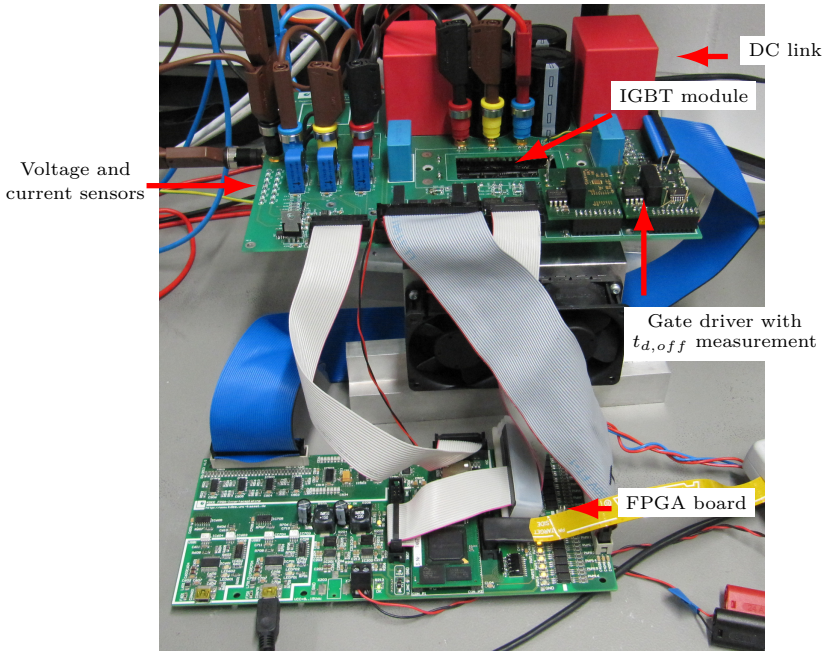


Figure 6.13.: Laboratory set-up of a three-phase inverter built around a 50 A sixpack IGBT module.

[2]Infineon FS50R12KT4_B15

A field-programmable gate array (FPGA) was used to generate the required gate-pulses using space-vector pulse-width modulation (SVPWM). Different switching strategies (as described in e.g. [120, 121]) were implemented and can be selected by sending control signals to the FPGA. The turn-off delay measurement circuitry is controlled by a soft-core micro-controller within the FPGA. The measured turn-off delays are analysed in combination with the measured currents and voltages to estimate the device temperatures. An overview of the functions implemented on the FPGA is provided in Figure 6.14.

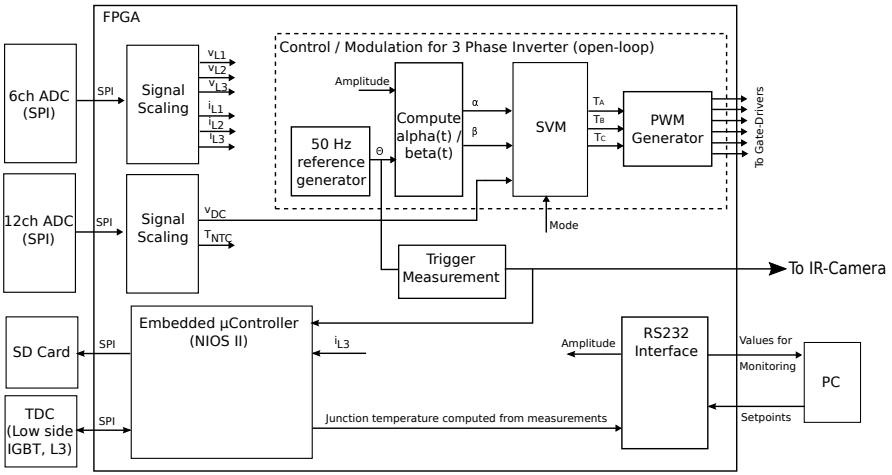
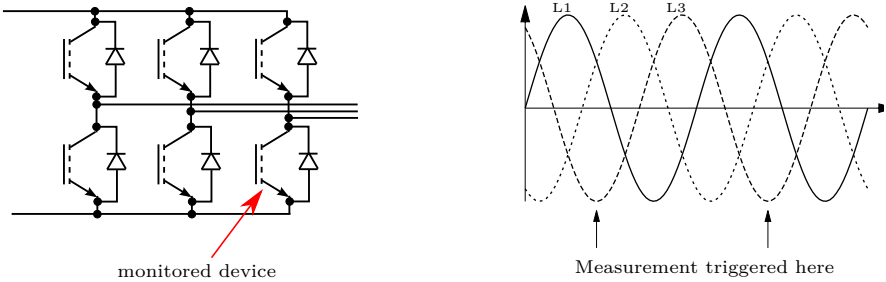


Figure 6.14.: Block diagram of functionality implemented on FPGA to control inverter (open-loop operation) and demonstrate on-line temperature monitoring.

The logic within the FPGA triggers a turn-off delay measurement (via the implemented micro-controller) as well as an IR measurement at a switching event at the peak of the AC output current as illustrated in Fig 6.15.

The micro-controller receives the measured turn-off delay time from the TDC and stores it on an SD-card. Additionally, the current and voltage measured by the ADC just previous to the turn-off delay measurement are recorded alongside the turn-off delay measurement. The actual device temperature was measured using a high-speed infra-red camera. The infra-red measurement was synchronised to the turn-off delay time measurement by a synchronisation pulse sent from the control board.



(a) Monitoring was implemented for one low-side IGBT in the two-level inverter.

(b) Turn-off delay measurement is triggered at peak current in monitored device.

Figure 6.15.: Illustration of the measurement point at the peak current switched by the monitored low-side IGBT.

6.6.1. Calibration measurements and model fitting

As previously discussed, the turn-off delay depends on the temperature of the IGBT as well as the switched current and voltage. A model that links the influencing factors to the measured turn-off delay had to be found to allow the virtual junction temperature T_{vj} to be obtained from the measured turn-off delay, the switched current and the DC-link voltage during converter operation.

To obtain data for finding such a model a number of measurements at different operating points of the inverter were conducted. The measured turn-off delay at different temperatures and six different inverter operating points is shown in Fig. 6.16.

As can be seen from the data in Fig 6.16 some outliers are obtained in the measurement. To improve the results data points that clearly contained invalid data were removed from the dataset and averaging over a number of measurement points was introduced. The resulting data is replotted in Figure 6.17.

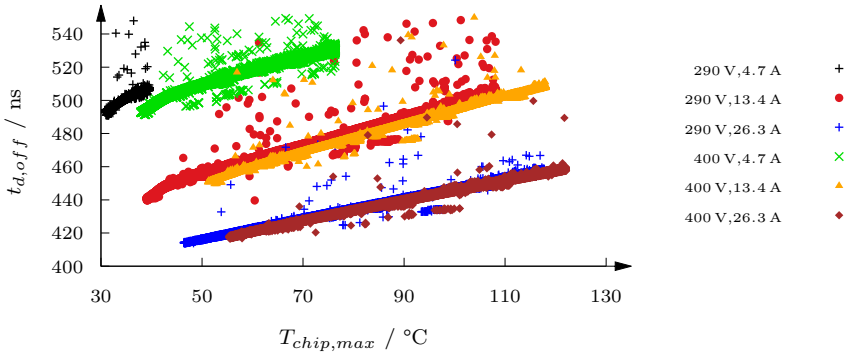


Figure 6.16.: Measured turn-off delay at various operating points. No filtering.

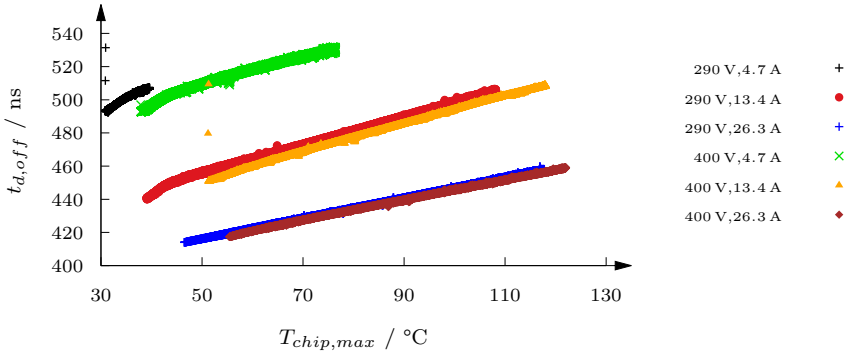


Figure 6.17.: Measured turn-off delay at various operating points. Implausible values removed and filtered by averaging. Data previously shown in [93]

The data in Fig 6.17 shows that at each individual operating point the temperature and turn-off delay are linearly related. However, the gradient and y-intercept of the linear relationship vary between the different operating points. The following set of equations was used to describe the relationship between the measured quantities:

$$t_{d,off}\left(T_{vj}, I_C, V_{DC}\right) = m\left(I_C\right) \cdot T_{vj} + b\left(V_{DC}, I_C\right) \tag{6.1}$$

$$m\left(I_C\right) = m_2 \cdot I_C^2 + m_1 \cdot I_C + m_0 \tag{6.2}$$

$$b\left(V_{DC}, I_C\right) = \left(b_3 \cdot V_{DC} + b_2\right) \cdot ln\left(I_C\right) + b_1 \cdot V_{DC} + b_0 \tag{6.3}$$

The coefficients m_2 to m_0 and b_3 to b_0 were found by fitting the model to the measured data. The resulting coefficients are provided in Table 6.2. Additionally, the fitted lines are shown as an overlay to the measured data points in Fig 6.18.

Table 6.2.: Parameters found by fitting

m_2	-6.048×10^{-5}
m_1	-1.079×10^{-2}
m_0	9.763×10^{-1}
b_3	1.972×10^{-2}
b_2	-5.520×10^{1}
b_1	-8.326×10^{-2}
b_0	5.682×10^{2}

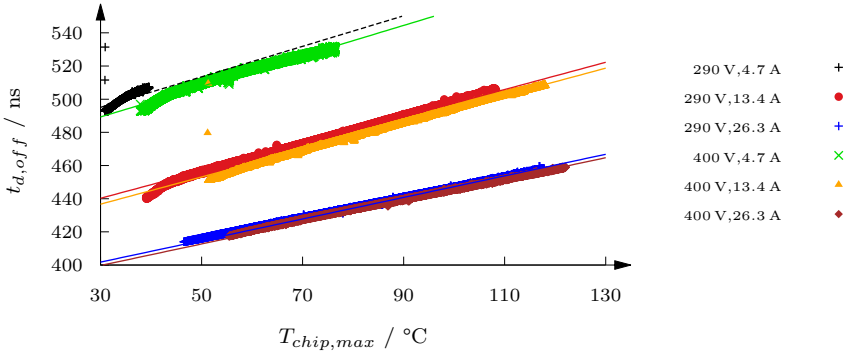


Figure 6.18.: Model of turn-off delay with fitted parameters compared to measured values

One can see that with this simple model the dependency between the chip temperature, the DC-link voltage and the switched current can be modelled.

6.6.2. On-line temperature measurement during converter operation

To show the capability of the measurement system to monitor the chip temperature during converter operation two further measurement runs were conducted. The model relating the measured turn-off delay to the chip temperature was implemented in the micro-controller (within the FPGA) to enable direct conversion of the measurement result to a temperature.

The measured temperatures were stored on an SD card along with the measured voltages and currents. Synchronised to the on-line measurements infra-red were taken to evaluate the performance of the on-line measurement solution. The measured temperatures and operating conditions are plotted below.

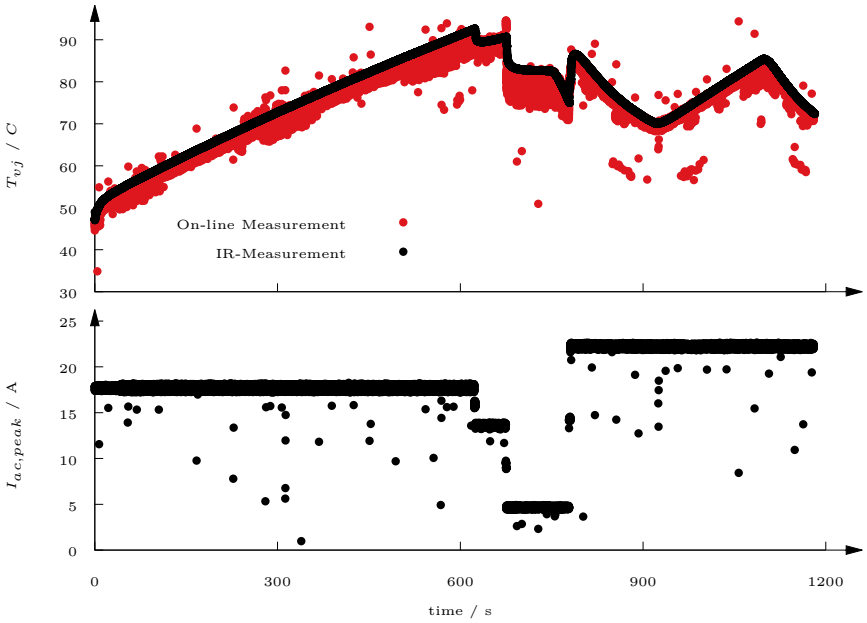


Figure 6.19.: Comparison of on-line temperature measurement with IR measurement. (V_{DC} constant at 290 V, f_{sw} = 16 kHz)

As can be seen from the plots in Figure 6.19 the temperatures measured by the IR-camera and the on-line system are in good agreement, however, some noise is seen on the temperatures measured by the on-line system as well as on the current

measurements. The data was post-processed by removing implausible values and filtering (averaging over multiple measurements) and the post-processed data is replotted in Figure 6.20.

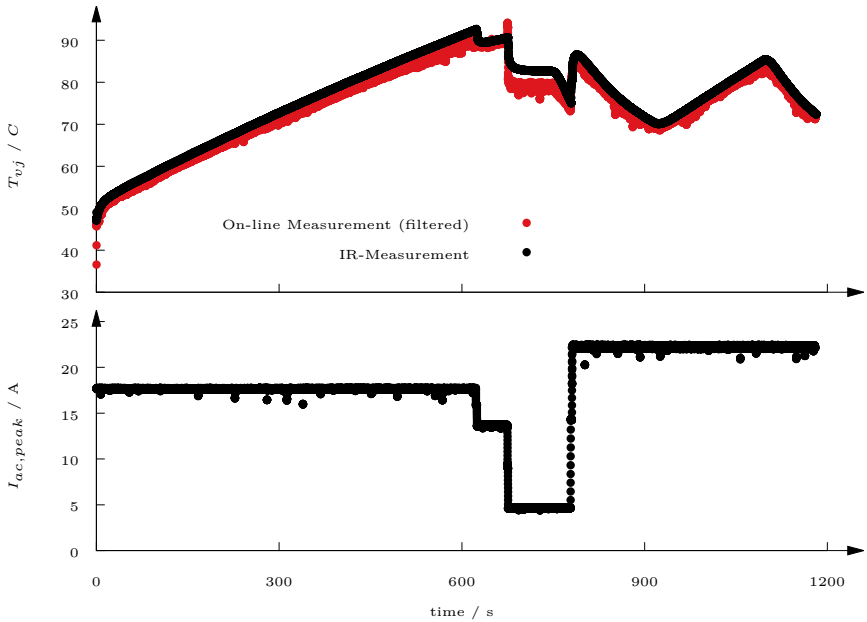


Figure 6.20.: Comparison of on-line temperature measurement with IR measurement. (V_{DC} constant at 290 V, $f_{sw} = 16$ kHz) Implausible values removed, filtered by averaging. Previously published at [93]

As can be seen from Figure 6.20 the post-processing has significantly improved the quality of the temperature measurements. Instead of post-processing the results as was done here it is also possible to implement the plausibility checks for the measurements ($t_{d,off}$, I_C, V_{DC}) as well as the filtering on the micro-controller.

To illustrate that the method also works for varying DC-link voltages V_{DC} a second test run was performed. The measurements obtained in this test run are plotted in Figure 6.21 (after post-processing as previously described).

The results show, that the implemented on-line measurement of the chip temperature yields good results over a range of DC-link voltages and output currents.

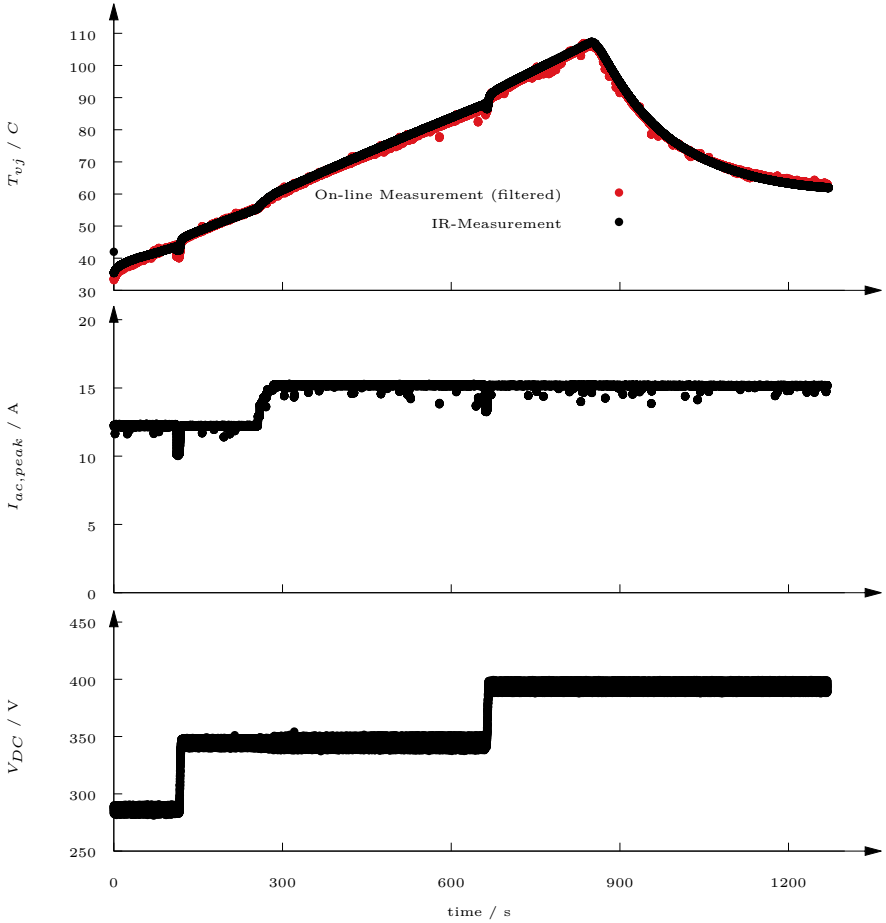


Figure 6.21.: Comparison of on-line temperature measurement with IR measurement. (f_{sw} = 16 kHz) Implausible values removed, filtered by averaging. Previously published at [93]

6.7. Conclusion

In this chapter an implementation of a measurement circuit which enables indirect measurements of the temperature of the IGBT chip during operation of a power converter was presented. The method itself is very similar to the method described in [109] and makes use of the well known sensitivity of the IGBT turn-off delay $t_{d,off}$ to temperature.

With the help of a scaled three-phase inverter laboratory set-up it was shown that the implemented measurement circuit allows on-line temperature measurements to be taken during converter operation.

Before the presented methodology can be considered for application in a product it would be essential to further investigate ways to minimise the required calibration effort. To do so the component to component variation of the turn-off delay of IGBTs of the same type needs to be explored. Also, it would be important to investigate the variability in the sensitivity of the turn-off delay between different types and generations of IGBTs.

The measurement system itself also needs to be optimised. The resistive voltage divider to measure the rise in V_{CE} needs to be improved to minimise its time delay and the stability of the measurement system itself needs to be analysed to identify possible drifts with temperature or other changing factors. Maybe, alternative methods of sensing time dependent durations at device turn-off, such as that presented in [106], should be considered to avoid high voltage divider ratios that are required to sense the collector-emitter voltage.

Additionally, further investigation of the behaviour of the turn-off delay of multiple IGBT chips connected in parallel is necessary to decide whether the turn-off delay time is suitable as a TSEP for temperature measurement in larger multi-chip modules. The preliminary investigations that were conducted on two parallel IGBTs suggest that an average temperature is sensed if devices with different temperatures are paralleled.

Overall, the results presented in this chapter show that measuring the chip temperature of IGBTs during converter operation is possible with sufficient accuracy and acceptable effort in terms of additional components by sensing the turn-off delay.

In [122] Musallam et.al. presented a method to perform on-line rainflow computations to perform on-line estimations of the remaining lifetime of power modules. While a temperature monitoring system as presented here can not measure the

temperatures of all parts of a power module (e.g. system solder, chip solder, etc.) it could be used to supplement compact thermal models (see e.g. [123] for such a real-time model) that are used to estimate the temperatures within the power module during converter operation.

Alternatively, the temperatures measured by the on-line measurement system could directly be applied to an on-line rainflow counting algorithm if only the temperature cycles at the chips are to be analysed. In that case the history of temperature cycles imposed on the IGBT module can be related to the cycling capability to estimate the remaining life of the module.

7. Summary and Conclusion

In this work a number of aspects related to the reliability of power semiconductors with a focus on photovoltaic central inverters for sun-belt regions were investigated.

On the device level an investigation into the cosmic radiation robustness of a number of Si and SiC semiconductor devices with rated voltages between 600 V and 1700 V was undertaken. Samples of the different devices were irradiated with a neutron beam with a spectrum that approximates that of the terrestrial neutron flux to measure the voltage dependent failure rate of the components.

The results of the measurements show that the tested SiC MOSFETs are more robust than the tested Si IGBTs and Si SJ MOSFETs against cosmic radiation induced single-event-burnout. However, it was also observed that part of the robustness apparently has to be attributed to the high breakdown voltage that the tested devices have when compared to their rated voltage. Nevertheless, it was seen that two of the tested SiC MOSFETs show higher robustness than the Si devices if the results are normalised to the measured breakdown voltage.

Additionally, the results show that the tested SiC Schottky diode is more robust than a state of the art Si diode tested by other authors [52], while the tested Si CAL diodes are even more robust against cosmic radiation induced single-event-burnout.

In summary, the results show that the tested SiC devices are more robust against cosmic radiation induced SEB than the tested Si devices with the exception of the Si CAL diode. Nevertheless, it is essential to note that this has to be evaluated for every new device as changes in the design can impact the robustness. Particularly, reductions in the ratio between the breakdown voltage and nominal voltage of the SiC MOSFETs could lead to a reduction of their SEB robustness.

On the system level a simulation to estimate the stresses on the power semiconductor modules in photovoltaic central inverters operated in sun-belt regions was developed. The simulation takes information about a photovoltaic system and climatic data as inputs and estimates the temperature cycles occurring at the heat-sink / IGBT module baseplate and at the semiconductor chips as well as the voltage stress. From these stresses the lifetime (limited by temperature cycling) and reliability (failure due to cosmic radiation induced SEB) of the IGBT modules were estimated.

Based on simulations conducted for a total of nine locations it was seen that power cycling is apparently not critical for photovoltaic central inverters. However, the performed simulation did not capture temperature cycles that occur at the semiconductors due to the output current pulsation within the fundamental period of the output current waveform. These also need to be taken into consideration when designing a converter. The thermal cycling stress is at a higher level than the power cycling stress and certainly has to be taken into consideration when sizing an inverter. Overall, the stresses predicted by the simulation suggest that it is possible to reach lifetimes exceeding 25 years with appropriate designs.

The thermal cycling stress was found to be most critical in locations that are characterised by the frequent occurrence of low ambient temperatures. At low ambient temperatures large daily temperature cycles between the cooling system's set-point temperature and the nightly ambient temperature were observed.

Alternative approaches to determine the set-point for the cooling system controller were suggested and their effectiveness in reducing the thermal cycling stress was analysed. It was shown that the thermal cycling stress can be reduced significantly without requiring any hardware changes and that the impact on the power demand for cooling of the converter can be minimised if prognosis data is used.

In addition to the temperature cycling stress the voltage stress on the semiconductors in a photovoltaic central inverter was investigated. The investigation has shown that output power curtailment of the photovoltaic inverter leads to increased voltage stress. This voltage stress was compared with the measured voltage dependent failure rate of 1200 V power semiconductors (silicon IGBT / diode) and it was seen that failure rates significantly exceeding tolerable limits may be observed if 1200 V silicon power semiconductors are used in 1000 V inverters. The use of more robust semiconductors (e.g. SiC MOSFETs or silicon CAL diodes) or the use of devices from a higher voltage class are options to achieve acceptable failure rates. Alternatively, multi-level topologies with lower voltage stress on the semiconductors can be considered. No matter which approach is selected it is important to accurately estimate the voltage stress in the application and compare

it with the voltage dependent failure rate of the considered semiconductors to evaluate if a design meets the requirements.

Finally, an implementation of an on-line temperature monitoring system for IGBTs within a power converter was shown. The implemented temperature monitoring solution makes use of the temperature dependency of the IGBT's turn-off delay. Using a small laboratory set-up of a three phase inverter it was shown that the temperature can be measured during operation of the inverter. The temperature measurements were validated using a high speed infra-red measurement system.

A. Perez model for diffuse irradiance on a tilted surface

According to the Perez model in the version presented in [73] and discussed by Quaschning in [66, 67] the diffuse irradiation can be calculated as

$$E_{diff,gen} = E_{diff,hor} \cdot \left(\frac{(1 - F_1) \cdot (1 + cos\beta_{gen})}{2} + F_1 \cdot \frac{a}{b} + F_2 \cdot sin\beta_{gen} \right) \quad \text{(A.1)}$$

where

$$a = max(0; cos\theta_{gen}) \quad \text{(A.2)}$$

$$b = max(0.087; sin\gamma_s) \quad \text{(A.3)}$$

and F_1 and F_2 are coefficients describing the anisotropy around the sun and the horizon [73]. The values for F_1 and F_2 are computed by first computing the index for the sky clearance ,ϵ, and the sky's brightness, Δ.

$$\epsilon = \frac{\frac{E_{diff,hor} + \frac{E_{dir,hor}}{sin\gamma_s}}{E_{diff,hor}} + k \cdot {\theta_s}^3}{1 + k \cdot {\theta_s}^3} \quad \text{(A.4)}$$

$$\Delta = E_{diff,hor} \cdot \frac{m}{E_0} \quad \text{(A.5)}$$

θ_s	angle between sun and zenith / rad	
k	constant	$k = 1.041$
m	relative air mass [67, p.103]	$\frac{1}{sin\gamma_s}$

Based on the value of the sky clearance index the coefficients from Table A.1 are selected and used to compute F_1 and F_2 according to the following equations.

$$F_1 = F_{11} + F_{12} \cdot \Delta + F_{13} \cdot \theta_s \tag{A.6}$$

$$F_2 = F_{21} + F_{22} \cdot \Delta + F_{23} \cdot \theta_s \tag{A.7}$$

Table A.1.: Coefficients for the irradiance model by Perez et.al. [73]

ϵ	F_{11}	F_{12}	F_{13}	F_{21}	F_{22}	F_{23}
1 ... 1.065	-0.008	0.588	-0.062	-0.060	0.072	-0.022
1.065 ... 1.230	0.130	0.683	-0.151	-0.019	0.066	-0.029
1.230 ... 1.500	0.330	0.487	-0.221	0.055	-0.064	-0.026
1.500 ... 1.950	0.568	0.187	-0.295	0.109	-0.152	-0.014
1.950 ... 2.800	0.873	-0.392	-0.362	0.226	-0.462	0.001
2.800 ... 4.500	1.132	-1.237	-0.412	0.288	-0.823	0.056
4.500 ... 6.200	1.060	-1.600	-0.359	0.264	-1.127	0.131
6.200 ... –	0.678	-0.327	-0.250	0.156	-1.377	0.251

B. Details of thermal model of power electronic stack

Table B.1.: Parameters of Foster type thermal model. Values for $Z_{th}JC$ taken from [82]

Z_{th}JC (Diode)					
i:		1	2	3	4
r_i / (K/kW):		3.0	8.5	23.8	0.7
τ_i / s:		0.0008	0.013	0.05	0.6
Z_{th}JC (IGBT)					
i:		1	2	3	4
r_i / (K/kW):		0.8	4.0	13.2	1.5
τ_i / s:		0.0008	0.013	0.05	0.6
Z_{th}CA (for different fan speeds)					
i:		1	2	3	4
r_i / (K/kW):	FAN: 0 %	1.88	53.77	99.98	8.27
	FAN: 20 %	6.90	19.01	11.15	2.19
	FAN: 40 %	7.97	10.99	1.66	1.60
	FAN: 60 %	7.50	8.25	2.96	1.92
	FAN: 80 %	8.67	6.81	1.19	1.99
	FAN: 100 %	8.63	5.91	1.61	1.95
c_i / (J/K):		826	13086	28827	2594904

Table B.2.: Parameters of the Cauer type thermal model. Obtained by transforming Foster model (see Table B.1) to Cauer model.

Z_{th}JC (Diode)						
i:			1	2	3	4
r_i / (K/kW):			5.02	19.98	10.77	0.22
c_i / (J/K):			0.0512	0.1892	0.7877	69.6627
Z_{th}JC (IGBT)						
i:			1	2	3	4
r_i / (K/kW):			1.94	10.65	6.05	0.86
c_i / (J/K):			0.1585	0.3120	1.3597	52.4494
Z_{th}CA (for different fan speeds)						
i:		0	1	2	3	4
r_i / (K/kW):	FAN: 0 %	2.29	0.83	102.59	53.11	5.78
	FAN: 20 %	2.29	6.14	28.49	0.63	1.75
	FAN: 40 %	2.29	7.31	8.81	2.38	1.45
	FAN: 60 %	2.29	6.79	9.64	0.19	1.76
	FAN: 80 %	2.29	8.06	5.39	1.03	1.89
	FAN: 100 %	2.29	8.03	5.59	0.35	1.85
c_i / (J/K):			551	9817	290573	2566237

Table B.3.: Cooling curves obtained from project partner and simulated model responses (Part 1).

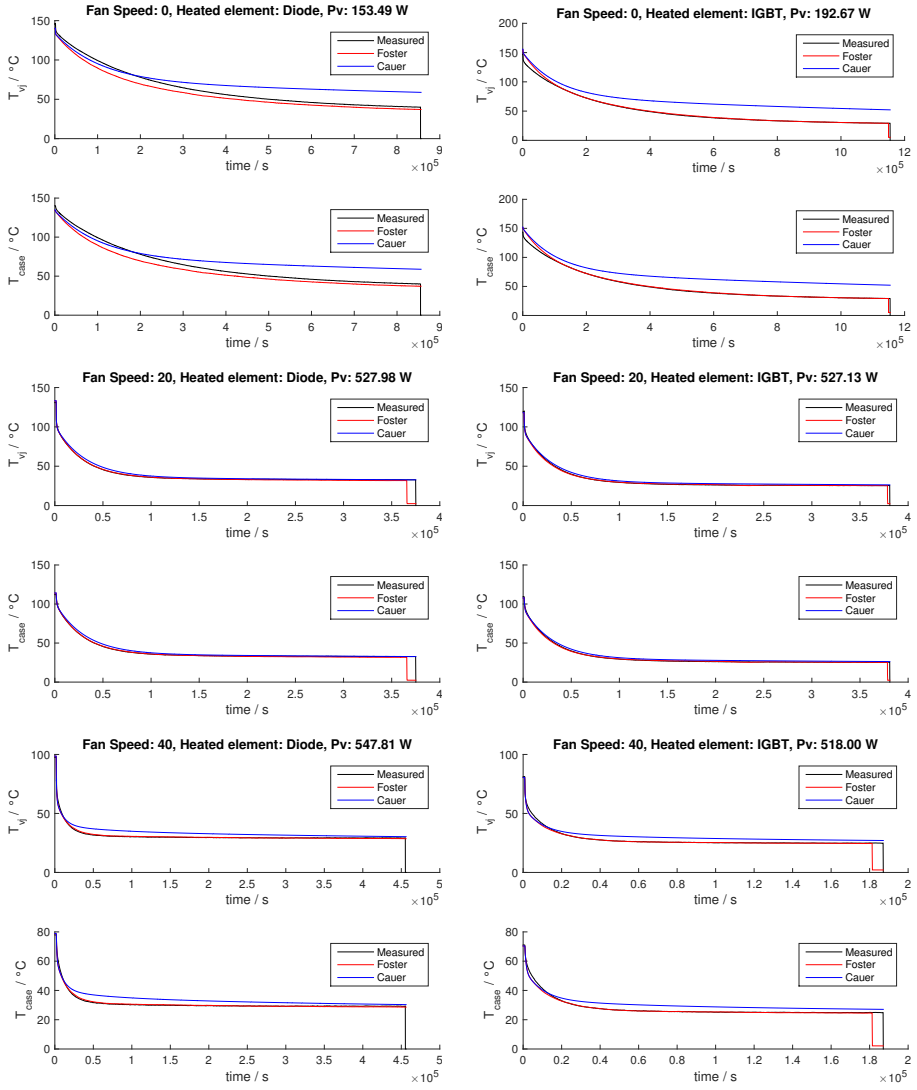
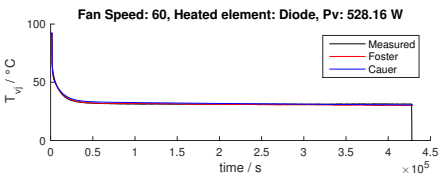
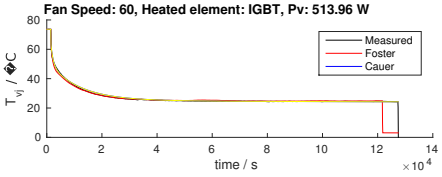
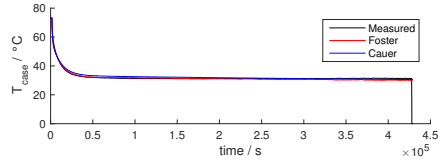
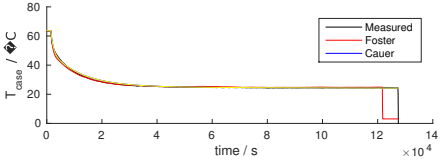


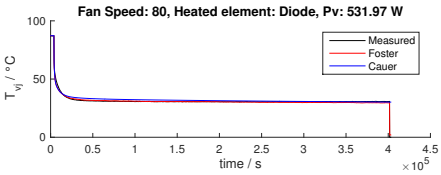
Table B.4.: Cooling curves obtained from project partner and simulated model responses (Part 2).

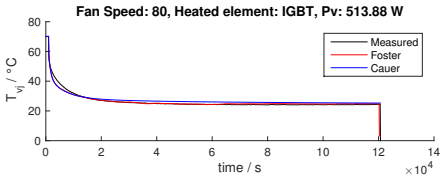


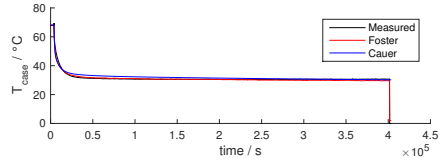


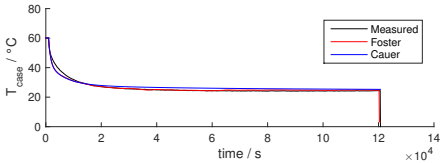


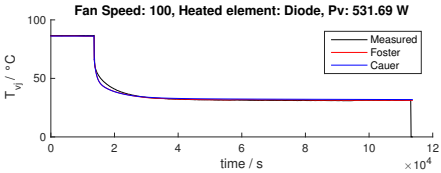


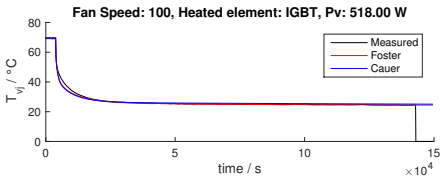


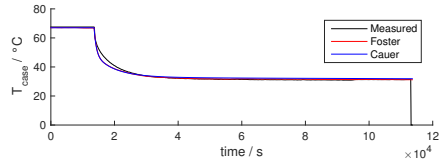


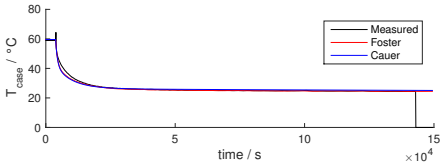












C. Simulation results using different thermal model structures

As discussed in chapter 4 the Cauer type structure shown in Figure 4.9 was used to model the thermal behaviour of the IGBT modules of one phase arm. To identify if the Foster type model that was directly fitted to the available cooling curves gives significantly different results a few of scenarios investigated in this chapter were also simulated using the Foster model. A comparison of the thermal cycling and power cycling predicted using both thermal models with otherwise unchanged simulation conditions is shown in Figure C.1 and Figure C.2.

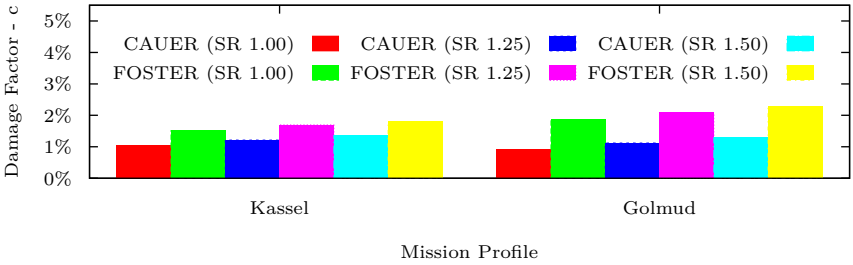


Figure C.1.: Comparison of thermal cycling damage factors obtained using different thermal models in otherwise identical simulation conditions.

The comparison shows that higher damage factors are obtained if the Foster type model is used instead of the Cauer type model. The damage factors obtained from the simulation using the Foster type model are between 33 % and 107 % higher than those obtained using the Cauer model.

To investigate the reasons for these differences further analysis of the simulation results was performed. In Figure C.3 the distribution of temperature cycles at

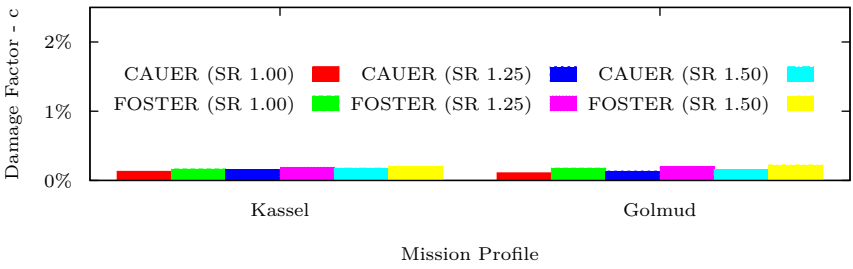


Figure C.2.: Comparison of power cycling damage factors obtained using different thermal models in otherwise identical simulation conditions.

the heatsink(case) predicted for the mission profile "Kassel" by both the Foster and the Cauer model are compared.

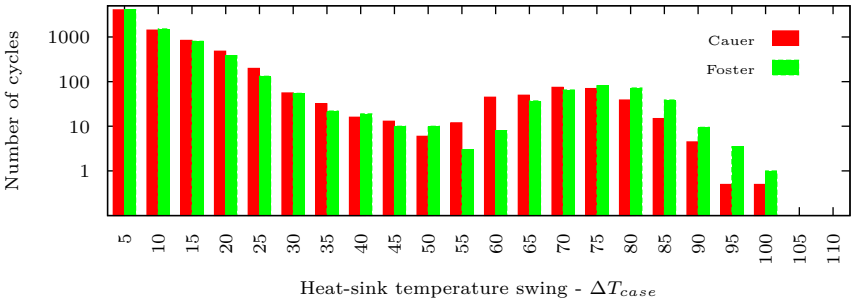


Figure C.3.: Comparison of temperature cycles at heat-sink using different thermal models in otherwise identical simulation conditions, Kassel, size-ratio 1.5, fixed PV generator.

From the data in Figure C.3 one can see that overall the size of temperature cycles predicted by the Foster model is larger than the size of cycles predicted by the Cauer model.

The damage caused by the cycles of different size is illustrated in Figure C.4. It can be seen that the slightly larger cycles predicted by the Foster model result in larger damage factors. This is as expected, as the larger cycles are more critical for the modules than the smaller cycles. Overall the damage factor predicted

when the Cauer model is used is 1.35 % whereas it is 1.80 % if the Foster model is used.

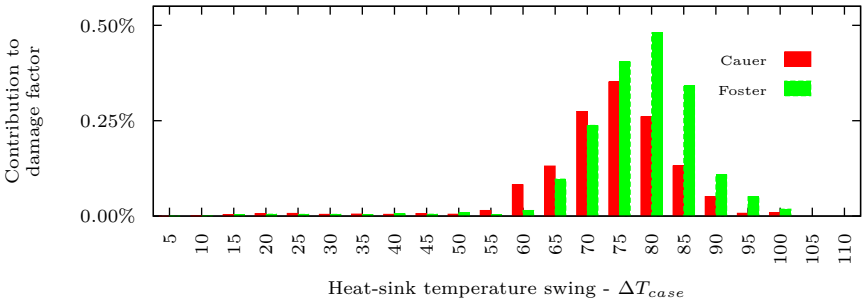


Figure C.4.: Comparison of damage factors caused by temperature cycles at heat-sink using different thermal models in otherwise identical simulation conditions, Kassel, size-ratio 1.5, fixed PV generator.

The reason for the higher damage factor predicted when using the Foster model is thus that the cycles are larger than the cycles predicted using the Cauer model. It remains to be seen why the cycles predicted are of different size when the two different thermal models are used.

One known limitation of the Foster type models is that variations in the ambient temperature are immediately observed across the entire model. To investigate whether this is the reason for the difference in temperature cycles predicted by the two models another simulation in which the ambient temperature was set constant to the average annual temperature was performed.

In Figure C.5 the temperature cycles at the heat-sink are plotted for four simulations of the same conditions. The thermal model has been varied (Foster vs. Cauer structure) and the ambient temperature was set to a constant value for two of the simulations whereas data from the mission profile was used for the other two simulations (fixed T_{amb}).

From Figure C.5 and the damage factors in Table C.1 one can see that if the Cauer model is used the variations in ambient temperature only have a small effect on the temperature cycles at the heat-sink (T_{case}).

If the Foster model is used the effect of the ambient temperature variations on the temperature cycles is much stronger. Due to the way the model is structured

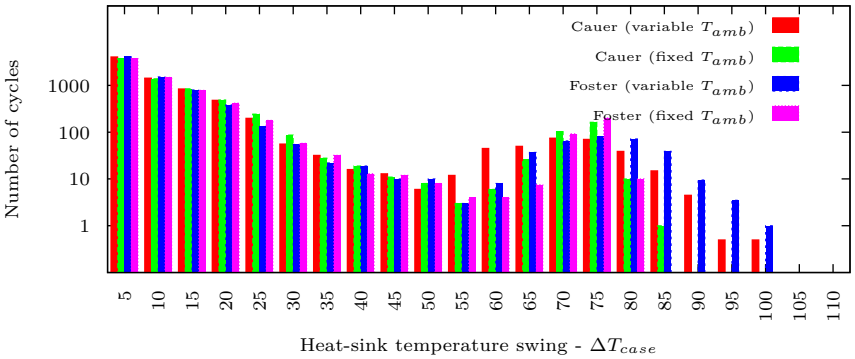


Figure C.5.: Comparison of temperature cycles at heat-sink using different thermal models and with variable and fixed ambient temperatures. Other simulation conditions are identical, Kassel, size-ratio 1.5, fixed PV generator.

the ambient temperature changes directly affect the temperature at all points in the model, whereas they are dampened in the case of the Cauer model.

Table C.1.: Damage factors due to temperature cycling - T_{case} for different thermal models and the influence of ambient temperature variation.

Thermal Model	T_{amb}	Damage Factor Thermal Cycling	Damage Factor Power Cycling
Cauer	variable (from mission profile)	1.55 %	0.22 %
Cauer	constant	1.53 %	0.20 %
Foster	variable (from mission profile)	2.05 %	0.25 %
Foster	constant	1.60 %	0.20 %

The behaviour of the Foster model when the ambient temperature changes is not realistic, as it will take some time for the heat-sink temperature to change as a consequence of a change in ambient temperature. For the purpose of this investigation it was decided to use the Cauer model structure as it more realistically describes the behaviour of the heat-sink as the ambient temperature is varied.

D. Simulation results using different sets of climatic data

In order to investigate the effect of selecting different historical datasets or datasets based on future climate change scenarios within Meteonorm the simulation described in chapter 4 was repeated for three locations using different input datasets.

In chapter 4 the most up to date period of historical datasets was used to generate the dataset of solar irradiance and temperature within Meteonorm. Here, the oldest available dataset and a dataset based on the IPCC A1B scenario for 2030 were additionally selected (see [124] for information about IPCC scenarios). The simulations were carried out for each dataset with otherwise identical settings. In Figure D.1 the damage factor due to thermal cycling for each of the three datasets for three locations is shown.

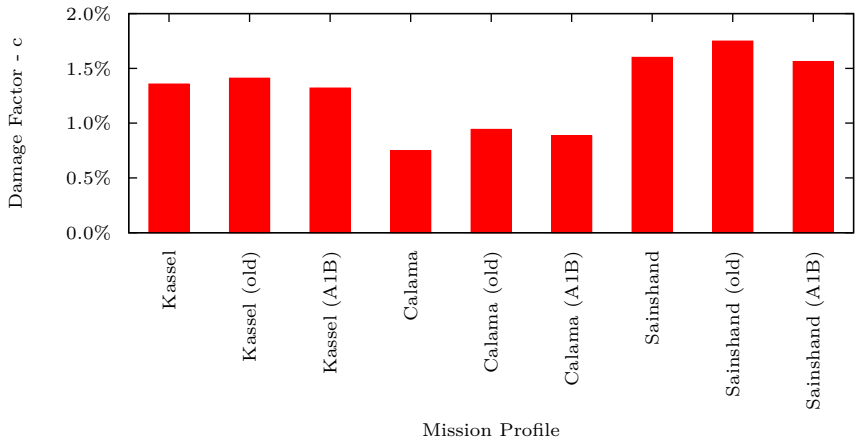


Figure D.1.: Comparison of thermal cycling damage factors obtained using different sets of climatic data in otherwise identical simulation conditions (size ratio 1.5).

As can be seen the impact of selecting datasets from different time periods for each of the locations is quite small. The difference between the locations is certainly more significant than the differences resulting from using different datasets generated within Meteonorm.

In Figure D.2 the power cycling damage factors for each of the three datasets for the investigated locations is shown. The results show very little difference in the predicted power cycling damage factors for the different datasets.

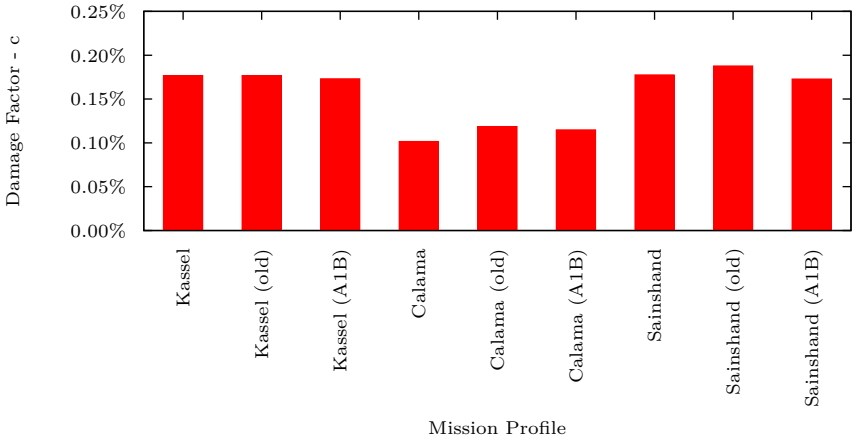


Figure D.2.: Comparison of power cycling damage factors obtained using different sets of climatic data in otherwise identical simulation conditions (size ratio 1.5).

Overall, the comparison of results using different climatic datasets for these locations suggests that the impact of changing climate on the results of the lifetime estimation of the power semiconductor modules in the investigated PV central inverter is very low.

Bibliography

[1] Volker U. Hoffmann. 'DAMALS WAR'S - Ein Rückblick auf die Entwicklung der Photovoltaik in Deutschland'. In: *SONNENENERGIE* 6 (2008), pp. 38–39. URL: http://www.sonnenenergie.de/sonnenenergie-redaktion/SE-2008-06/Layout-fertig/PDF/Einzelartikel/SE-2008-06-s038-Photovoltaik-PV-Historie.pdf (visited on 27/11/2015).

[2] *Gesamtausgabe der Energiedaten - Datensammlung des BMWi.* Bundesministerium für Wirtschaft und Energie. Jan. 2016. URL: http://bmwi.de/BMWi/Redaktion/Binaer/energie-daten-gesamt,property=blob,bereich=bmwi2012,sprache=de,rwb=true.xls (visited on 01/05/2016).

[3] *Photovoltaik-Preisindex.* URL: http://www.photovoltaik-guide.de/pv-preisindex (visited on 28/10/2015).

[4] Lars Döring. *Wirtschaftlichkeit von Photovoltaik-Großkraftwerken in ausgewählten Regionen des globalen Sonnengürtels.* BSc-Thesis, University of Kassel. 2013.

[5] Panos Konstantin. *Praxisbuch Energiewirtschaft.* 2nd ed. Springer Berlin Heidelberg, 2009. DOI: 10.1007/978-3-540-78592-7.

[6] Christian Felgemacher, Wolfram Kruschel, Lars Döring and Peter Zacharias. 'Herausforderungen für Zuverlässigkeit und Lebensdauer leistungselektronischer Systeme in der Energieversorgung'. In: *Konferenz für Nachhaltige Energieversorgung und Integration von Speichern (NEIS).* 2013.

[7] Huai Wang, M. Liserre and F. Blaabjerg. 'Toward Reliable Power Electronics: Challenges, Design Tools, and Opportunities'. In: *IEEE Industrial Electronics Magazine* 7.2 (2013), pp. 17–26. ISSN: 1932-4529. DOI: 10.1109/MIE.2013.2252958.

[8] *Electropedia: The World's Online Electrotechnical Vocabulary - Section 192-01 - Reliability.* IEC. Feb. 2015. URL: http://www.electropedia.org/iev/iev.nsf/display?openform&ievref=192-01-24 (visited on 19/02/2017).

[9] Arno Meyna and Bernhard Pauli. *Zuverlässigkeitstechnik Qualitative Bewertungsverfahren*. 2nd ed. Carl Hanser Verlag, 2010.

[10] H. Wang, K. Ma and F. Blaabjerg. 'Design for reliability of power electronic systems'. In: *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*. Oct. 2012, pp. 33–44. DOI: 10.1109/IECON.2012.6388833.

[11] Christian Nöding. 'PV-Stromrichter höherer Leistung für 1.500 V Systemspannung Bewertung, Vergleich, Realisierung'. PhD thesis. Universität Kassel, 2016.

[12] Shaoyong Yang, Angus Bryant, Philip Mawby, Dawei Xiang, Li Ran and Peter Tavner. 'An Industry-Based Survey of Reliability in Power Electronic Converters'. In: *IEEE Transactions on Industry Applications* 47.3 (May 2011), pp. 1441–1451. DOI: 10.1109/TIA.2011.2124436.

[13] Josef Lutz. 'Packaging and Reliability of Power Modules'. In: *8th International Conference on Integrated Power Systems (CIPS)*. Feb. 2014.

[14] Hyunseok Oh, Bongtae Han, P. McCluskey, Changwoon Han and B.D. Youn. 'Physics-of-Failure, Condition Monitoring, and Prognostics of Insulated Gate Bipolar Transistor Modules: A Review'. In: *IEEE Transactions on Power Electronics* 30.5 (May 2015), pp. 2413–2426. ISSN: 0885-8993. DOI: 10.1109/TPEL.2014.2346485.

[15] Mauro Ciappa. 'Selected failure mechanisms of modern power modules'. In: *Microelectronics Reliability* 42.4–5 (2002), pp. 653–667. ISSN: 0026-2714. DOI: 10.1016/S0026-2714(02)00042-2.

[16] Jack Flicker, Robert Kaplar, Benjamin Yang, Matthew Marinella and Jennifer Granata. 'Insulated gate bipolar transistor reliability testing protocol for PV inverter applications'. In: *Progress in Photovoltaics: Research and Applications* 22.9 (2014), pp. 970–983. ISSN: 1099-159X. DOI: 10.1002/pip.2351.

[17] Rui Wu, F. Blaabjerg, Huai Wang, M. Liserre and F. Iannuzzo. 'Catastrophic failure and fault-tolerant design of IGBT power electronic converters - an overview'. In: *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*. Nov. 2013, pp. 507–513. DOI: 10.1109/IECON.2013.6699187.

[18] Josef Lutz, Heinrich Schlangenotto, Uwe Scheuermann and Rik De Doncker. *Semiconductor Power Devices Physics, Characteristics, Reliability*. Springer, 2011. DOI: 10.1007/978-3-642-11125-9.

[19] V. Smet, F. Forest, J. Huselstein, F. Richardeau, Z. Khatir, S. Lefebvre and M. Berkani. 'Ageing and Failure Modes of IGBT Modules in High-Temperature Power Cycling'. In: *IEEE Transactions on Industrial Electronics* 58.10 (Oct. 2011), pp. 4931–4941. ISSN: 0278-0046. DOI: 10.1109/TIE.2011.2114313.

[20] C. Bailey, H. Lu and T. Tilford. 'Predicting the Reliability of Power Electronic Modules'. In: *ICEPT 2007. 8th International Conference on Electronic Packaging Technology*. Aug. 2007. DOI: 10.1109/ICEPT.2007.4441543.

[21] K. Guth et al. 'End-of-life investigation on the .XT interconnect technology'. In: *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. May 2015.

[22] U. Scheuermann. 'Reliability of Planar SKiN Interconnect Technology'. In: *7th International Conference on Integrated Power Electronics Systems (CIPS)*. Mar. 2012.

[23] M. Held, P. Jacob, G. Nicoletti, P. Scacco and M.-H. Poech. 'Fast power cycling test of IGBT modules in traction application'. In: *International Conference on Power Electronics and Drive Systems, Proceedings.* May 1997, pp. 425–430. DOI: 10.1109/PEDS.1997.618742.

[24] Reinhold Bayerer, Tobias Herrmann, Thomas Licht, Josef Lutz and Marco Feller. 'Model for Power Cycling lifetime of IGBT Modules - various factors influencing lifetime'. In: *5th International Conference on Integrated Power Systems (CIPS)*. 2008.

[25] *AN2010-02 V1.0, Technical Information, IGBT modules, Use of Power Cycling Curves for IGBT4*. Infineon Technologies AG. 2010.

[26] H. Kabza, H.-J. Schulze, Y. Gerstenmaier, P. Voss, J. Wilhelmi, W. Schmid, F. Pfirsch and K. Platzöder. 'Cosmic radiation as a cause for power device failure and possible countermeasures'. In: *Proceedings of the 6th International Symposium on Power Semiconductor Devices and ICs (ISPSD '94)*. May 1994, pp. 9–12. DOI: 10.1109/ISPSD.1994.583620.

[27] H. Matsuda, T. Fujiwara, M. Hiyoshi, K. Nishitani, A Kuwako and T. Ikehara. 'Analysis of GTO failure mode during DC voltage blocking'. In: *Proceedings of the 6th International Symposium on Power Semiconductor Devices and ICs (ISPSD '94)*. May 1994, pp. 221–225. DOI: 10.1109/ISPSD.1994.583727.

[28] H.R. Zeller. 'Cosmic ray induced breakdown in high voltage semiconductor devices, microscopic model and phenomenological lifetime prediction'. In: *Proceedings of the 6th International Symposium on Power Semiconductor Devices and ICs (ISPSD '94)*. May 1994, pp. 339–340. DOI: 10.1109/ISPSD.1994.583762.

[29] H. R. Zeller. 'Cosmic Ray Induced Failures in High Power Semiconductor Devices'. In: *Solid State Electronics* 38.12 (1995), pp. 2041–2046.

[30] Nando Kaminski and Arnost Kopta. *ABB Switzerland Ltd., Semiconductors, Failure Rates of HiPak Modules Due to Cosmic Rays - Application Note 5SYA 2042-04*. Mar. 2011.

[31] *ABB Switzerland Ltd., Semiconductors, Application Note 5SYA 2061-00: Failure Rates of Fast Recovery Diodes Due to Cosmic Rays*. Jan. 2012.

[32] Jörg Walter. 'Simulationsbasierte Zuverlässigkeitsanalyse in der modernen Leistungselektronik'. PhD thesis. RWTH Aachen, 2004.

[33] *MIL-HDBK-217F (Notice 2): Reliability Prediction of Electronic Equipment*. United States Department of Defense. 1995.

[34] Christian Felgemacher, Wolfram Kruschel, Christian Nöding and Peter Zacharias. 'Reliability Aspects of a Power Electronic Voltage Regulator for Active Low-Voltage Distribution Networks'. In: *IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*. June 2015. DOI: 10.1109/PEDG.2015.7223018.

[35] O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez and R. Teodorescu. 'Electro-thermal modeling for junction temperature cycling-based lifetime prediction of a press-pack IGBT 3L-NPC-VSC applied to large wind turbines'. In: *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*. 2011, pp. 568–575.

[36] Ke Ma, Marco Liserre, Frede Blaabjerg and Tamas Kerekes. 'Thermal Loading and Lifetime Estimation for Power Device Considering Mission Profiles in Wind Power Converter'. In: *IEEE Transactions on Power Electronics* 30.2 (Feb. 2015), pp. 590–602. ISSN: 0885-8993. DOI: 10.1109/TPEL.2014.2312335.

[37] Nicolae-Cristian. Sintamarean, Frede Blaabjerg, Huai Wang and Yongheng Yang. 'Real Field Mission Profile Oriented Design of a SiC-Based PV-Inverter Application'. In: *IEEE Transactions on Industry Applications* 50.6 (Nov. 2014), pp. 4082–4089. ISSN: 0093-9994. DOI: 10.1109/TIA.2014.2312545.

[38] Christian Felgemacher, Samuel Araújo, Peter Zacharias, Karl Nesemann and Artjom Gruber. 'Cosmic Radiation Ruggedness of Si and SiC Power Semiconductors'. In: *28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. 2016, pp. 51–54. DOI: 10.1109/ISPSD.2016.7520775.

[39] Johannes Blümer. 'Partikel in der Pampa'. In: *Physik Journal* 9.6 (2010), pp. 31–36. URL: http://www.pro-physik.de/details/articlePdf/1102467/issue.html.

[40] Hans Blümer and Karl-Heinz Kampert. 'Die Suche nach den Quellen der kosmischen Strahlung: Antworten versprechen die Luftschauerexperimente KASCADE und AUGER'. In: *Physik Journal (Physikalische Blätter)* 56.3 (2000), pp. 39–45. ISSN: 1521-3722. DOI: 10.1002/phbl.20000560311.

[41] S.P. Swordy. 'The Energy Spectra and Anisotropies of Cosmic Rays'. English. In: *The Astrophysics of Galactic Cosmic Rays*. Ed. by Roland Diehl, Etienne Parizot, Reinald Kallenbach and Rudolf Von Steiger. Vol. 13. Space Sciences Series of ISSI. Springer Netherlands, 2001, pp. 85–94. ISBN: 978-90-481-5862-1. DOI: 10.1007/978-94-017-3239-0_8.

[42] Norbert Lossau. *Urknall-Experiment glückt ohne Weltuntergang*. 2010. URL: http://www.welt.de/wissenschaft/urknallexperiment/article6990263/Urknall-Experiment-glueckt-ohne-Weltuntergang.html (visited on 28/10/2015).

[43] Winfried Kaindl. 'Modellierung höhenstrahlungsinduzierter Ausfälle in Halbleiterleistungsbauelementen'. PhD thesis. Technische Universität München, 2005. URL: http://nbn-resolving.de/urn/resolver.pl?urn:nbn:de:bvb:91-diss20051202-1805269629.

[44] Christoph Weiß. 'Höhenstrahlungsresistenz von Silizium-Hochleistungsbauelementen'. PhD thesis. Technische Universität München, 2015. URL: http://nbn-resolving.de/urn/resolver.pl?urn:nbn:de:bvb:91-diss-20150129-1130763-0-6.

[45] J. F. Ziegler. 'Terrestrial cosmic rays'. In: *IBM Journal of Research and Development* 40.1 (Jan. 1996), pp. 19–39. ISSN: 0018-8646. DOI: 10.1147/rd.401.0019.

[46] *JEDEC Standard JESD89A: Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices*. JEDEC, Oct. 2006.

[47] *Cosmic Ray Database of the Cosmic Ray Station of the University of Oulu / Sodankyla Geophysical Observatory*. URL: http://cosmicrays.oulu.fi/.

[48] *Global 30 Arc-Second Elevation (GTOPO30), Data available from the U. S. Geological Survey.* URL: https://lta.cr.usgs.gov/GTOPO30.

[49] Hiroaki Asai, Kenji Sugimoto, Isamu Nashiyama, Yoshiya Iide, Kensuke Shiba, Mieko Matsuda and Yoshio Miyazaki. 'Terrestrial Neutron-Induced Single-Event Burnout in SiC Power Diodes'. In: *IEEE Transactions on Nuclear Science* 59.4 (2012), pp. 880–885. ISSN: 0018-9499. DOI: 10.1109/TNS.2012.2203145.

[50] Hiroaki Asai et al. 'Tolerance Against Terrestrial Neutron-Induced Single-Event Burnout in SiC MOSFETs'. In: *IEEE Transactions on Nuclear Science* 61.6 (Dec. 2014), pp. 3109–3114. ISSN: 0018-9499. DOI: 10.1109/TNS.2014.2371892.

[51] Shuichi Nishida, Tomoyuki Shoji, Toyokazu Ohnishi, Touma Fujikawa, Noboru Nose, Masayasu Ishiko and Kimimori Hamada. 'Cosmic ray ruggedness of IGBTs for hybrid vehicles'. In: *22nd International Symposium on Power Semiconductor Devices IC's (ISPSD)*. June 2010, pp. 129–132.

[52] Uwe Scheuermann and Uwe Schilling. 'Cosmic Ray Failures of Power Modules - The Diode Makes the Difference'. In: *PCIM Europe 2015, 19 - 21 May*. 2015.

[53] Gerhard Soelkner, Winfried Kaindl, Michael Treu and Dethard Peters. 'Reliability of SiC Power Devices Against Cosmic Radiation-Induced Failure'. In: *Materials Science Forum*. Vol. 556-557. 2007, pp. 851–856. DOI: 10.4028/www.scientific.net/MSF.556-557.851.

[54] G. Soelkner, W. Kaindl, H.-J. Schulze and G. Wachutka. 'Reliability of power electronic devices against cosmic radiation-induced failure'. In: *Microelectronics Reliability* 44.9-11 (2004). 15th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, pp. 1399–1406. ISSN: 0026-2714. DOI: 10.1016/j.microrel.2004.07.024.

[55] Alexander V. Prokofiev, Jan Blomgren, Mitja Majerle, Ralf Nolte, Stefan Röttger, Simon P. Platt, Cai Xiao Xiao and Andrey N. Smirnov. 'Characterization of the ANITA Neutron Source for Accelerated SEE Testing at the Svedberg Laboratory'. In: *2009 IEEE Radiation Effects Data Workshop*. July 2009, pp. 166–173. DOI: 10.1109/REDW.2009.5336295.

[56] *MIL-STD-750F (Change 1): Test Method Standard - Test Methods for Semiconductor Devices*. United States Department of Defense. Apr. 2013.

[57] Alessio Griffoni et al. 'Neutron-Induced Failure in Silicon IGBTs, Silicon Super-Junction and SiC MOSFETs'. In: *IEEE Transactions on Nuclear Science* 59.4 (2012), pp. 866–871. ISSN: 0018-9499. DOI: 10.1109/TNS.2011.2180924.

[58] Jeffrey L. Titus. 'An Updated Perspective of Single Event Gate Rupture and Single Event Burnout in Power MOSFETs'. In: *IEEE Transactions on Nuclear Science* 60.3 (2013), pp. 1912–1928. ISSN: 0018-9499. DOI: 10.1109/TNS.2013.2252194.

[59] G. Consentino, M. Laudani, G. Privitera, C. Pace, C. Giordano, J. Hernandez and M. Mazzeo. 'Effects on power transistors of Terrestrial Cosmic Rays: Study, experimental results and analysis'. In: *Twenty-Ninth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*. Mar. 2014, pp. 2582–2587. DOI: 10.1109/APEC.2014.6803667.

[60] Sandra Liu et al. 'Evaluation on Protective Single Event Burnout Test Method for Power DMOSFETs'. In: *IEEE Transactions on Nuclear Science* 59.4 (Aug. 2012), pp. 1125–1129. ISSN: 0018-9499. DOI: 10.1109/TNS.2011.2177863.

[61] Christian Felgemacher, Samuel Araújo, Christian Nöding, Peter Zacharias, Alexander Ehrlich and Martin Schidleja. 'Evaluation of Temperature Cycling Stress imposed on Power Electronic Modules in Photovoltaic Central Inverters in Sunbelt Regions'. In: *CIPS 2016 - 9th International Conference on Integrated Power Electronic Systems*. 2016.

[62] Christian Felgemacher, Samuel Araújo and Peter Zacharias. 'Benefits of increased cosmic radiation robustness of SiC semiconductors in large power-converters'. In: *PCIM Europe 2016*. 2016.

[63] Ben Willis. *PV Talk: Why 1,500V is set to dominate utility PV*. PV-Tech Solar Media Ltd. Jan. 2016. URL: http://www.pv-tech.org/interviews/pv-talk-why-1500v-is-set-to-dominate-utility-pv (visited on 12/11/2016).

[64] Charles W. Thurston. *Higher voltage, lower cost*. Sept. 2015. URL: http://www.pv-magazine.com/archive/articles/beitrag/higher-voltage--lower-cost-_100020830/630/#axzz4N3Fayqvu (visited on 12/11/2016).

[65] *WHITEPAPER 1500 V: TRUE 1500 V TECHNOLOGY FOR THE NEW GENERATION OF PV POWER PLANTS*. SMA Solar Technology AG. URL: http://www.sma.de/fileadmin/content/global/specials/1500V/Whitepap1500V-AEN1639.pdf (visited on 12/11/2016).

[66] Volker Quaschning. *Regenerative Energiesysteme*. 8th ed. Carl Hanser Verlag GmbH & Co. KG, Jan. 2013. ISBN: 978-3446435261.

[67] Volker Quaschning. 'Simulation der Abschattungsverluste bei solarelektrischen Systemen'. PhD thesis. Technische Universität Berlin, 1996. ISBN: 3-89574-191-4.

[68] D. T. Reindl, W. A. Beckmann and J. A. Duffie. 'Diffuse Fraction Correlations'. In: *ISES Solar World Conference*. 1989, pp. 2082–2086.

[69] *DIN 5034: Tageslicht in Innenräumen, Teil 2: Grundlagen*. Feb. 1985.

[70] Yong Sheng Khoo, André Nobre, Raghav Malhotra, Dazhi Yang, Ricardo Rüther, Thomas Reindl and Armin G. Aberle. 'Optimal Orientation and Tilt Angle for Maximizing in-Plane Solar Irradiation for PV Applications in Singapore'. In: *IEEE Journal of Photovoltaics* 4.2 (Mar. 2014), pp. 647–653. ISSN: 2156-3381. DOI: 10.1109/JPHOTOV.2013.2292743.

[71] Richard Perez and Ronald Stewart. 'Solar irradiance conversion models'. In: *Solar Cells* 18.3-4 (Oct. 1986), pp. 213–222. DOI: 10.1016/0379-6787(86)90120-1.

[72] Richard Perez, Robert Seals, Pierre Ineichen, Ronald Stewart and David Menicucci. 'A new simplified version of the perez diffuse irradiance model for tilted surfaces'. In: *Solar Energy* 39.3 (1987), pp. 221–231. DOI: 10.1016/S0038-092X(87)80031-2.

[73] Richard Perez, Pierre Ineichen, Robert Seals, Joseph Michalsky and Ronald Stewart. 'Modeling daylight availability and irradiance components from direct and global irradiance'. In: *Solar Energy* 44.5 (1990), pp. 271–289. ISSN: 0038-092X. DOI: 10.1016/0038-092X(90)90055-H.

[74] Christian Märtel. *Vor- und Nachteile verschiedener Nachführsysteme im Vergleich*. URL: http://www.photovoltaik-web.de/photovoltaik/dacheignung/solar-tracker-nachfuehrung-nachfuehrsysteme.html (visited on 18/12/2015).

[75] M. Mattei, G. Notton, C. Cristofari, M. Muselli and P. Poggi. 'Calculation of the polycrystalline PV module temperature using a simple method of energy balance'. In: *Renewable Energy* 31.4 (Apr. 2006), pp. 553–567. ISSN: 0960-1481. DOI: 10.1016/j.renene.2005.03.010.

[76] W. Marańda and M. Piotrowicz. 'Extraction of thermal model parameters for field-installed photovoltaic module'. In: *27th International Conference on Microelectronics (MIEL), Proceedings*. May 2010, pp. 153–156. DOI: 10.1109/MIEL.2010.5490512.

[77] A.D. Jones and C.P. Underwood. 'A thermal model for photovoltaic systems'. In: *Solar Energy* 70.4 (2001), pp. 349–359. ISSN: 0038-092X. DOI: 10.1016/S0038-092X(00)00149-3.

[78] Ayedh H. Alqahtani, Muthanna S. Abuhamdeh and Yazan M. Alsmadi. 'A simplified and comprehensive approach to characterize photovoltaic system performance'. In: *2012 IEEE Energytech*. 2012, pp. 1–6. DOI: 10.1109/EnergyTech.2012.6304628.

[79] *Datasheet: Sunmodule Plus SW 280 - 290 mono, SolarWorld AG*. URL: http://www.solarworld.de/fileadmin/downloads_new/produkt/sunmodule/datenblaetter/de/mono/mono_280-290_de.pdf (visited on 17/11/2015).

[80] *Datasheet: Sunmodule Plus SW 250 - 260 poly, SolarWorld AG*. URL: http://www.solarworld.de/fileadmin/downloads_new/produkt/sunmodule/datenblaetter/de/poly/poly_250-260_de.pdf (visited on 17/11/2015).

[81] Uwe Drofenik, Ivana Kovacevic, Roland Schmidt and Johann W. Kolar. 'Multi-Domain Simulation of Transient Junction Temperatures and Resulting Stress-Strain Behavior of Power Switches for Long-Term Mission Profiles'. In: *Proc. 11th Workshop Control and Modeling for Power Electronics (COMPEL 2008)*. 2008. DOI: 10.1109/COMPEL.2008.4634691.

[82] Infineon. *Datasheet: FF1400R12IP4, Rev. 2.4*. 2013. URL: http://www.infineon.com/dgdl/Infineon-FF1400R12IP4-DS-v02_04-en_de.pdf?fileId=db3a30431f848401011feb7645573e9f (visited on 16/01/2016).

[83] Y.C. Gerstenmaier, W. Kiffe and G. Wachutka. 'Combination of thermal subsystems modeled by rapid circuit transformation'. In: *13th International Workshop on Thermal Investigation of ICs and Systems (THERMINIC 2007)*. Sept. 2007, pp. 115–120. DOI: 10.1109/THERMINIC.2007.4451758.

[84] T. Gradinger and G. Riedel. 'Thermal Networks for Time-Variant Cooling Systems: Modeling Approach and Accuracy Requirements for Lifetime Prediction'. In: *Proc. 7th International Conference on Integrated Power Electronics Systems (CIPS)*. 2012.

[85] H. Müller. 'Beziehungen zwischen dem praktisch verwendeten und dem physikalisch sinnvollen Wärmeersatzschaltbild von Dioden und Thyristoren'. In: *Electrical Engineering (Archiv für Elektrotechnik)* 54 (3 1971), pp. 170–176. ISSN: 0948-7921. DOI: 10.1007/BF01624089.

[86] Bartlomiej Ufnalski. *Foster and Cauer equivalent networks*. Oct. 2014. URL: http://www.mathworks.com/matlabcentral/fileexchange/48042 (visited on 12/03/2016).

[87] Martin März and Paul Nance. *Thermal Modeling of Power-electronic Systems*. URL: http://www.iisb.fraunhofer.de/content/dam/iisb2014/en/Documents/Research-Areas/Energy_Electronics/publications_patents_downloads/Publications/Therm_Modelling_2000_IISB.pdf (visited on 12/02/2017).

[88] *ASTM E1049-85(2011): Standard Practices for Cycle Counting in Fatigue Analysis*. ASTM, 2011.

[89] Adam Nieslony. *Rainflow Counting Algorithm*. Apr. 2010. URL: http://www.mathworks.com/matlabcentral/fileexchange/3026 (visited on 19/05/2015).

[90] Krzysztof Mainka, Markus Thoben and Oliver Schilling. 'Counting Methods for Lifetime Calculation of Power Modules'. In: *Power Electronics Europe* 6 / 2011 (Sept. 2011), pp. 35–38. URL: http://www.power-mag.com/pdf/issuearchive/48.pdf (visited on 12/02/2016).

[91] Christian Jochen Felgemacher, Christian Nöding, Samuel Vasconcelos Araújo and Peter Zacharias. 'Verfahren zur Steuerung einer Kühlvorrichtung zur Lebensdauererhöhung Abwärme erzeugender Komponenten und Kühlvorrichtung'. Offenlegungsschrift DE 10 2014 112 458 A1.

[92] Christian Jochen Felgemacher, Christian Nöding, Peter Zacharias and Samuel Vasconcelos Araújo. 'Method for Controlling a Cooling Device for Increasing the Lifetime of Components Generating Waste Heat, and Cooling Device'. Patent Application Publication US 2016/0065126 A1.

[93] Christian Felgemacher, Benjamin Dombert, Christian Nöding and Peter Zacharias. 'IGBT Online-Temperature Monitoring using Turn-Off Delay as a Temperature Sensitive Electrical Parameter'. In: *CIPS 2016 - 9th International Conference on Integrated Power Electronic Systems*. 2016.

[94] Benjamin Dombert. *Indirekte Messungen der Chiptemperatur ("Piggyback")*. Internal KDEE report (confidential). Feb. 2012.

[95] David L. Blackburn. 'Temperature measurements of semiconductor devices - a review'. In: *Twentieth Annual IEEE Semiconductor Thermal Measurement and Management Symposium*. Mar. 2004, pp. 70–80. DOI: 10.1109/STHERM.2004.1291304.

[96] Waleri Brekel, Thomas Duetemeyer, Gunnar Puk and Oliver Schilling. 'Time Resolved In Situ Tvj Measurements of 6.5kV IGBTs during Inverter Operation'. In: *Proceedings PCIM Europe Conference*. 2009, pp. 808–813.

[97] Ralf Schmidt and Uwe Scheuermann. 'Using the chip as a temperature sensor - The influence of steep lateral temperature gradients on the Vce(T)-measurement'. In: *13th European Conference on Power Electronics and Applications. EPE '09.* Sept. 2009.

[98] Yvan Avenas, Laurent Dupont and Zoubir Khatir. 'Temperature Measurement of Power Semiconductor Devices by Thermo-Sensitive Electrical Parameters - A Review'. In: *IEEE Transactions on Power Electronics* 27.6 (June 2012), pp. 3081–3092. DOI: 10.1109/TPEL.2011.2178433.

[99] D. Barlini, M. Ciappa, A. Castellazzi, M. Mermet-Guyennet and W. Fichtner. 'New technique for the measurement of the static and of the transient junction temperature in IGBT devices under operating conditions'. In: *Microelectronics Reliability* 46.9–11 (2006). Proceedings of the 17th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis. Wuppertal, Germany 3rd–6th October 2006, pp. 1772–1777. ISSN: 0026-2714. DOI: 10.1016/j.microrel.2006.07.058.

[100] D. Barlini, M. Ciappa, M. Mermet-Guyennet and W. Fichtner. 'Measurement of the transient junction temperature in MOSFET devices under operating conditions'. In: *Microelectronics Reliability* 47.9–11 (2007). 18th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, pp. 1707–1712. ISSN: 0026-2714. DOI: 10.1016/j.microrel.2007.07.008.

[101] Yong-Seok Kim and Seung-Ki Sul. 'On-line estimation of IGBT junction temperature using on-state voltage drop'. In: *The 1998 IEEE Industry Applications Conference. Thirty-Third IAS Annual Meeting.* Vol. 2. 1998, 853–859 vol.2. DOI: 10.1109/IAS.1998.730245.

[102] Harald Kuhn and Axel Mertens. 'On-line junction temperature measurement of IGBTs based on temperature sensitive electrical parameters'. In: *13th European Conference on Power Electronics and Applications. EPE '09.* 2009.

[103] Jimmy Alexander Butron Ccoa, Bastian Strauss, Gerhard Mitic and Andreas Lindemann. 'Investigation of Temperature Sensitive Electrical Parameters for Power Semiconductors (IGBT) in Real-Time Applications'. In: *Proceedings of PCIM Europe Conference*. May 2014.

[104] Laurent Dupont, Yvan Avenas and Pierre-Olivier Jeannin. 'Comparison of Junction Temperature Evaluations in a Power IGBT Module Using an IR Camera and Three Thermosensitive Electrical Parameters'. In: *IEEE Transactions on Industry Applications* 49.4 (July 2013), pp. 1599–1608. ISSN: 0093-9994. DOI: 10.1109/TIA.2013.2255852.

[105] Laurent Dupont and Yvan Avenas. 'Evaluation of Thermo-Sensitive Electrical Parameters Based on the Forward Voltage for On-line Chip Temperature Measurements of IGBT Devices'. In: *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*. Sept. 2014, pp. 4028–4035. DOI: 10.1109/ECCE.2014.6953950.

[106] V. Sundaramoorthy, E. Bianda, R. Bloch, I. Nistor, G. Knapp and A. Heinemann. 'Online estimation of IGBT junction temperature (Tj) using gate-emitter voltage (Vge) at turn-off'. In: *15th European Conference on Power Electronics and Applications (EPE)*. Sept. 2013, pp. 1–10. DOI: 10.1109/EPE.2013.6634444.

[107] Ivan Bahun, Neven Čobanov and Željko Jakopović. 'Real-Time Measurement of IGBT's Operating Temperature'. In: *Automatika - Journal for Control, Measurement, Electronics, Computing and Communications* 52.4 (2011), pp. 295–305. URL: https://automatika.korema.hr/index.php/automatika/article/view/104/.

[108] Vinoth Kumar Sundaramoorthy, Enea Bianda, Richard Bloch and Franz Zurfluh. 'Simultaneous online estimation of junction temperature and current of IGBTs using emitter-auxiliary emitter parasitic inductance'. In: *Proceedings of PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. May 2014, pp. 1–8.

[109] 'Verfahren und Vorrichtung zur Bestimmung einer Sperrschichttemperatur eines Halbleiterbauelements'. German. Offenlegungsschrift DE 10 2012 006 009 A1. 26th Sept. 2013.

[110] 'System and method for monitoring in real time the operating state of an IGBT device'. European patent specification EP 2 615 467 B1. 18th June 2014.

[111] B. Jayant Baliga. *Fundamentals of Power Semiconductor Devices*. Springer, 2008. DOI: 10.1007/978-0-387-47314-7.

[112] Infineon. *Datasheet: IKW40N120H3, Rev. 2.1*. 2014. URL: http://www.infineon.com/dgdl/Infineon-IKW40N120H3-DS-v02_01-EN.pdf?fileId=db3a304325305e6d012591d4832f7032 (visited on 19/02/2017).

[113] Yanick Lobsiger and Johann W. Kolar. 'Voltage, Current and Temperature Measurement Concepts Enabling Intelligent Gate Drives'. In: *ECPE Workshop "Electronics around the Power Switch: Gate Drivers, Sensors and Control", Munich, Germany, June 29-30*. 2011. URL: https://www.pes.ee.ethz.ch/uploads/tx_ethpublications/Lobsiger_Measurement_Concepts_ECPE_WS_2011.pdf (visited on 26/11/2016).

[114] Dierk Schröder. *Leistungselektronische Bauelemente*. 2nd ed. Springer, 2006.

[115] Józef Kalisz. 'Review of methods for time interval measurements with picosecond resolution'. In: *Metrologia* 41 (2004), pp. 17–32. DOI: 10.1088/0026-1394/41/1/004.

[116] Dan I Porat. 'Review of Sub-Nanosecond Time-Interval Measurements'. In: *IEEE Transactions on Nuclear Science* 20.5 (Oct. 1973), pp. 36–51. ISSN: 0018-9499. DOI: 10.1109/TNS.1973.4327349.

[117] M. A Abas, G. Russell and D.J. Kinniment. 'Embedded high-resolution delay measurement system using time amplification'. In: *Computers Digital Techniques, IET* 1.2 (Mar. 2007), pp. 77–86. ISSN: 1751-8601. DOI: 10.1049/iet-cdt:20060099.

[118] F. Fontanelli, L. Repetto and R. Chittofrati. 'A simple instrument for measuring time intervals with subnanosecond resolution'. In: *American Journal of Physics* 70 (2002), pp. 1234–1236.

[119] *Datasheet: TDC-GP22 Universal 2-Channel Time-to-Digital Converters Dedicated to Ultrasonic Heat & Water Meters*. acam-messelectronic gmbh. Mar. 2014. URL: http://www.acam.de/fileadmin/Download/pdf/TDC/English/DB_GP22_en.pdf (visited on 12/02/2017).

[120] Dorin O. Neacsu. 'Space Vector Modulation - An Introduction'. In: *Tutorial at the 27th Annual IEEE Industrial Electronics Society Conference*. 2001, pp. 1583–1592.

[121] Zeng Cong, Liu Dichen, Liao Qingfen and Huang Yong. 'Research and realization of a Pulse Width Modulation technique based on voltage space vectors'. In: *Proc. Int. Conf. Electrical Machines and Systems ICEMS 2008*. 2008, pp. 2178–2182.

[122] Mahera Musallam, C. Mark Johnson, Chunyan Yin, Chris Bailey and Michel Mermet-Guyennet. 'Real-time life consumption power modules prognosis using on-line rainflow algorithm in metro applications'. In: *2010 IEEE Energy Conversion Congress and Exposition (ECCE)*. Sept. 2010, pp. 970–977. DOI: 10.1109/ECCE.2010.5617883.

[123] Mahera Musallam and C. Mark Johnson. 'Real-Time Compact Thermal Models for Health Management of Power Electronics'. In: *IEEE Transactions on Power Electronics* 25.6 (June 2010), pp. 1416–1425. ISSN: 0885-8993. DOI: 10.1109/TPEL.2010.2040634.

[124] *IPCC Special Report Emission Scenarios - Summary for Policymakers*. 2000. URL: https://www.ipcc.ch/pdf/special-reports/spm/sres-en.pdf (visited on 27/01/2017).

Acronyms

CAL	controlled axial lifetime
CTE	coefficient of thermal expansion
DCB	direct copper bonded
DfR	design for reliability
DUT	device under test
EEG	Erneuerbare-Energien-Gesetz
FPGA	field-programmable gate array
FTA	fault tree analysis
IGBT	insulated gate bipolar transistor
LCOE	levelised cost of electricity
LUT	look up table
MOSFET	motal oxide field effect transistor
MPP	maximum power point
MTTF	mean time to failure
NOCT	normal operating cell temperature
O&M	operation and maintenance
PCB	printed circuit board
PV	photovoltaic
SEB	single event burnout
SEGR	single event gate rupture
Si	silicon
SiC	silicon carbide
SVPWM	space-vector pulse-width modulation
TDC	time to digital converter
TSEP	temperature sensitive electrical parameter

List of symbols

A	Albedo coefficient.
A_t	Operating cost during period t.
c	Damage factor as proportion of used up lifetime.
$E_{0,hor}$	Solar constant - 1367 $\mathrm{W/m^2}$.
$E_{diff,gen}$	Diffuse solar irradiance on a titled plane.
$E_{diff,hor}$	Diffuse solar irradiance on a horizontal plane.
$E_{dir,gen}$	Direct solar irradiance on a tilted plane.
$E_{dir,hor}$	Direct solar irradiance on a horizontal plane.
$E_{G,gen}$	Total (global) solar irradiance on a tilted plane.
$E_{G,hor}$	Total (global) solar irradiance on a horizontal plane.
$E_{refl,gen}$	Reflected solar irradiance on a titled plane.
F_A	Neutron flux scaling factor due to altitude [46].
F_B	Neutron flux scaling factor due to geomagnetic location and solar modulation [46].
I_C	Collector current.
I_{mpp}	MPP current of photovoltaic module.
I_{sc}	Short circuit current of photovoltaic module.
k	Number of devices that failed in one neutron irradiation measurement.
t_i	Time during a neutron irradiation measurement when i-th device failed.
K_0	Initial investment cost.
K_I	Temperature coefficient of MPP current.
K_V	Temperature coefficient of MPP voltage.
n	Number of devices at the beginning of a neutron irradiation measurement.
N_f	Cycles to failure.
N_{pp}	Number of strings of PV modules connected in parallel.
N_s	Number of cells in series in photovoltaic module.

N_{ss}	Number of PV modules connected in series.
$R*$	Value of current sense resistor.
$R_{G,int}$	Internal gate resistance.
R_{meas}	Value of resistor used to detect state of fuses.
$R_{th,req}$	Required thermal resistance to achieve a desired heat-sink temperature at a known level of losses.
T_{amb}	Ambient temperature.
$t_{d,off}$	Turn-off delay time.
$t_{d,on}$	Turn-on delay time.
$T_{hs,set}$	Setpoint of heat sink temperature.
T_m	Mean temperature.
t_k	Time after which a neutron irradiation measurement is stopped.
$t_{k,eq}$	Time it would take under non-accelerated conditions for the recorded neutron dose to pass through the test set-up.
T_{NOCT}	Normal operating cell temperature of photovoltaic module.
T_{vj}	Virtual junction temperature.
V_{CE}	Collector-emitter voltage.
$V_{ce,sat}$	Collector-emitter saturation voltage.
V_{DC}	DC-Link voltage.
V_{DUT}	Voltage applied to DUT.
$V_{F,IGBT}$	IGBT forward voltage drop.
V_{GE}	Gate-emitter voltage.
V_{meas}	Measured voltage at datalogger input.
V_{mpp}	MPP voltage of photovoltaic module.
V_{oc}	Open circuit voltage of photovoltaic module.
V_T	Thermal voltage.
V_{th}	Threshold voltage.
Y_t	Energy output during period t.
α_{gen}	Azimuth of photovoltaic modules.
α_s	Azimuth of sun.
β_{gen}	Inclination of photovoltaic modules.
η_{MPP}	Photovoltaic module efficiency at maximum power point.
γ_s	Elevation of sun above horizon.
ΔT_j	Junction temperature swing.
θ_{gen}	Angle of incidence of sunlight on photovoltaic module.

List of Figures

1.1. Influence of system lifetime on LCOE for very large scale PV power plants in selected sunbelt locations. Re-plot of figure previously published in [6]. 2
1.2. Influence of inverter replacement periods on LCOE (Thailand, overall system lifetime 30 years). Re-plot of figure previously published in [6]. 3
1.3. Influence of different levels of O&M cost on LCOE (Thailand, overall system lifetime 30 years). Re-plot of figure previously published in [6]. 4

2.1. Typical bathtub shape of a plot of the failure rate of a population of items over time. (also see [9, p.111],[10]) 6
2.2. Failure rates (dashed lines) and survivability (solid lines) of two products. (Blue: Product A, Red: Product B) 7
2.3. Overview of structure of a photovoltaic central inverter. Subsystems such as auxiliary supplies, DC and AC contactors, gate-drives, etc. are not shown for clarity. 8
2.4. Cross section of standard power module - also see [13, 14] 9
2.5. Flowchart for the reliability prediction of power electronic systems. Similar illustration previously published in [34] 14
2.6. Combining failure rates to estimate system the system failure rate. 15

3.1. Reference neutron flux for New York City. (Source of data: [46]) 19
3.2. Altitude dependent acceleration factor for terrestrial neutron flux. (for underlying equation see: [46]) 19
3.3. Monthly averages of recorded neutron count rate at Oulu Neutron Monitor for a period of 51 years. (Source of data: [47]) 20
3.4. Relative neutron flux rate based on location (scaling factor $F_A \cdot F_B$) at average solar activity. Calculated using the method and rigidity cut-off data from [46] in combination with global elevation data from [48]. 20

3.5. Scaling factor for terrestrial neutron flux in sunbelt locations with potential for large scale photovoltaic installations. 21
3.6. Exemplary failure rates for Si (blue) and SiC (red) power semiconductors. (Source of data: [49, 50, 52]) 24
3.7. Spectral neutron flux at ANITA facility computed from spectral neutron fluence per incident proton given in [55] multiplied by beam current compared to the reference terrestrial neutron flux given in [46] scaled by 3×10^8. 26
3.8. Circuit to detect device failures for SEB failure rate measurement. Exemplary drawing for a group of three DUTs. In the experimental set-up each group had space for either 12 or 14 DUTs. (Principle circuit previously shown in [38]) 27
3.9. Main printed-circuit-board for SEB testing. A maximum of 52 DUTs can be connected using two smaller PCBs that are plugged into the main-board. 28
3.10. Overview of experimental set-up. 29
3.11. Measured failure rates for 600 V semiconductor switches at sea level and room temperature, normalised to chip area. (data previously shown: [38]) 32
3.12. Measured failure rates for 1200 V semiconductor switches at sea level and room temperature, normalised to chip area. (data previously shown: [38]) 32
3.13. Measured failure rates for 650 V and 1200 V semiconductor switches at sea level and room temperature, normalised to chip area and actual breakdown voltage of the devices. (data previously shown: [38]) 33
3.14. Measured failure rates for 1700 V semiconductor switches at sea level and room temperature, normalised to chip area. (data previously shown: [38]) 34
3.15. Measured failure rates for 1700 V semiconductor switches at sea level and room temperature, normalised to chip area and actual breakdown voltage of the devices. (data previously shown: [38]) . 34
3.16. Measured failure rates for 1200 V diodes at sea level and room temperature, normalised to chip area. Failure rates for a standard Si diode from [52] is shown for reference. (data previously shown: [38]) 35
3.17. Measured failure rates for 1700 V diodes at sea level and room temperature, normalised to chip area. Failure rates for a standard Si diode from [52] is shown for reference. (data previously shown: [38]) 36

3.18. Experimental set-up within a purpose built thermal chamber that was used to heat the DUTs to 100 °C while placed in the beam-line. 36
3.19. Measured failure rates for Si-IGBT-A at room temperature and at 100 °C at sea level, normalised to chip area (measurement at 100 °C not recalibrated to account for shielding of thermal chamber). 37
3.20. Measured failure rates for Si-IGBT-A at room temperature and at 100 °C at sea level, normalised to chip area and normalised to the measured breakdown voltage at the different temperatures (V_{bd} @ room temp = 1361 V, V_{bd} @ 100 °C = 1491 V, measurement at 100 °C not recalibrated to account for shielding of thermal chamber). 37
3.21. Measured failure rates for diodes compared to data from [50] and [52] (comparison of data previously shown: [38]) 38
3.22. Comparison of failure rates observed failures during long-term experiment and measurements at ANITA facility at V_{DC} = 1100 V. The measurement data of the accelerated measurement was originally discarded because failures occurred too fast for accurate measurement. Overall duration of long-term measurement: 4572.1 h. 41

4.1. Overview of the photovoltaic system considered in this investigation. 46
4.2. Overview of the photovoltaic system simulation. 47
4.3. Description of sun position according to DIN 5043 [69], also see [66, 67]. 50
4.4. Photovoltaic module orientation. (see [67, p.98][66], α_{gen} defined differently) 51
4.5. Modelled IV-characteristic (lines) vs. points taken from IV-characteristics in the data-sheets of the two PV modules [79, 80]. (T_{module} = 25 °C) 56
4.6. Possible operating ranges for the inverter (similar illustration previously published in [62]). 57
4.7. Exemplary look-up-table of semiconductor losses for a single IGBT module (two are connected in parallel for each phase) with V_{ac} = 360 V, T_j = 150 °C and $cos\phi = 1$. 60
4.8. Structure of Foster type thermal model for one phase-arm of B6 inverter. 61
4.9. Structure of Cauer type thermal model for one phase-arm of B6 inverter. 63
4.10. Exemplary simulation inputs (Kassel, days 135 to 139) 65
4.11. Exemplary transient photovoltaic generator irradiance and module temperature (Kassel, days 135 to 139, fixed tilt modules) 66

4.12. Exemplary inverter input transients (Kassel, days 135 to 139, size-ratio 1.5, fixed tilt modules) 66
4.13. Exemplary transients of semiconductor losses (total in one IGBT module), temperatures of high-side IGBT and heat-sink and simulated fan speed (Kassel, days 135 to 139, size-ratio 1.5, fixed tilt modules) 67
4.14. Simulated temperature cycles at the heat-sink of a central inverter operated for one year in Kassel (Germany), size ratio = 1.5, fixed modules. 68
4.15. Simulated temperature cycles at the high-side IGBT of a central inverter operated for one year in Kassel (Germany), size ratio = 1.5, fixed modules. 69
4.16. Predicted distribution of DC voltage over time for a photovoltaic inverter in Kassel (Germany) with different types of photovoltaic generator. 70
4.17. Map showing the locations for PV installations investigated in this study. 74
4.18. Damage factors for operation of IGBT module in a PV central inverter with a fixed PV generator, one-year mission profiles. T_{case}-cycles applied to thermal cycling capability data. 76
4.19. Damage factors for operation of IGBT module in a PV central inverter with a different types of PV generators, fixed size-ratio of 1.5, one-year mission profiles. T_{case}-cycles applied to thermal cycling capability data. 77
4.20. Damage factors due to temperature cycles at high-side IGBT chip. Fixed PV generator, variable size-ratio, one-year mission profile. $T_{j,HS-IGBT}$-cycles applied to power cycling capability data. . . . 78
4.21. Damage factors due to temperature cycles at high-side IGBT chip. Different types of PV generator trackers, fixed size-ratio of 1.5, one-year mission profile. $T_{j,HS-IGBT}$-cycles applied to power cycling capability data. 78
4.22. Failure rate due to single-event-burnout. Fixed PV generator, varying size-ratio, one-year mission profile. 79
4.23. Failure rate due to single-event-burnout. Different types of PV generator, fixed size-ratio of 1.00, one-year mission profile. 80
4.24. Failure rate due to single-event-burnout. Different types of PV generator, fixed size-ratio of 1.25, one-year mission profile. 80
4.25. Failure rate due to single-event-burnout. Different types of PV generator, fixed size-ratio of 1.5, one-year mission profile. 81

4.26. Failure rate due to single-event-burnout. Fixed tilt PV generator, fixed size-ratio of 1.5, one-year mission profile, assumed curtailment as per Table 4.5. 82

5.1. Simulation with incremental set-point adjustment. Red: Control with fixed set-point, Blue: Control with incremental set-point adjustment. Size-ratio 1.5, Kassel, fixed module installation. . . . 87
5.2. Simulation with incremental set-point adjustment and use of prognosis data for daily initial set-point estimation. Red: Control with fixed set-point, Blue: Control with incremental set-point adjustment. Size-ratio 1.5, Kassel, fixed module installation. . . . 88
5.3. Distribution of temperature cycles for different strategies of selecting the cooling system set-point. Mission Profile: Kassel, PV generator with fixed modules, size-ratio 1.5. 90
5.4. Contribution of temperature cycles to the temperature cycling damage factor for different strategies of selecting the cooling system set-point. Mission Profile: Kassel, PV generator with fixed modules, size-ratio 1.5. 90
5.5. Thermal cycling damage factors for the studied locations using different cooling system control strategies. A photovoltaic generator with size-ratio 1.5 and fixed installation of modules is assumed. . 91
5.6. Heat-sink temperature distribution for different cooling system control strategies. Mission profile: Kassel, fixed tilt PV generator, size-ratio 1.5. 92
5.7. Distribution of operating hours over fan-speed. Mission profile: Kassel, PV generator with fixed modules, size-ratio 1.5. 93
5.8. Additional cooling energy required for different cooling system control strategies in the various locations. Compared to default solution. PV generator with fixed modules, size-ratio 1.5. 93

6.1. Measured V_{ce} of IKW40N120H3 at small collector currents I_c. . . 98
6.2. Measured V_{ce} of IKW40N120H3 at larger collector currents I_{ce} for different temperature. 98
6.3. Measured V_{th} of IKW40N120H3 (V_{CE} set to 10 V, increased V_{GE} until I_{DS} of 1 mA flowed.) 100
6.4. Gate-drive circuit with turn-off delay measurement. 104
6.5. Block diagram of IGBT gate driver with turn-off delay measurement 105
6.6. PCB with IGBT driver and circuitry for turn-off delay measurement (further components on bottom side of PCB). 106

6.7. Experimental set-up used to conduct turn-off delay measurements on a discrete IGBT at different temperatures, switched currents and voltages. 107
6.8. Transient signals for turn-off at 25 A, 400 V, 100 °C, $R_g = 15\,\Omega$. . 108
6.9. Turn-off delay of an IKW40N120H3 measured with implemented circuit ($R_g = 15\,\Omega$). 109
6.10. Experimental set-up to conduct turn-off delay measurements on two DUTs at different temperatures 110
6.11. Turn-off delay measurement of parallel devices (one gate resistor $R_g = 15\,\Omega$ for both devices). 111
6.12. Turn-off delay of PrimePack module 112
6.13. Laboratory set-up of a three-phase inverter built around a 50 A sixpack IGBT module. 113
6.14. Block diagram of functionality implemented on FPGA to control inverter (open-loop operation) and demonstrate on-line temperature monitoring. 114
6.15. Illustration of the measurement point at the peak current switched by the monitored low-side IGBT. 115
6.16. Measured turn-off delay at various operating points. No filtering. 116
6.17. Measured turn-off delay at various operating points. Implausible values removed and filtered by averaging. Data previously shown in [93] 116
6.18. Model of turn-off delay with fitted parameters compared to measured values 117
6.19. Comparison of on-line temperature measurement with IR measurement. (V_{DC} constant at 290 V, $f_{sw} = 16\,\text{kHz}$) 118
6.20. Comparison of on-line temperature measurement with IR measurement. (V_{DC} constant at 290 V, $f_{sw} = 16\,\text{kHz}$) Implausible values removed, filtered by averaging. Previously published at [93] . . . 119
6.21. Comparison of on-line temperature measurement with IR measurement. ($f_{sw} = 16\,\text{kHz}$) Implausible values removed, filtered by averaging. Previously published at [93] 120

C.1. Comparison of thermal cycling damage factors obtained using different thermal models in otherwise identical simulation conditions. 133
C.2. Comparison of power cycling damage factors obtained using different thermal models in otherwise identical simulation conditions. . 134
C.3. Comparison of temperature cycles at heat-sink using different thermal models in otherwise identical simulation conditions, Kassel, size-ratio 1.5, fixed PV generator. 134

C.4. Comparison of damage factors caused by temperature cycles at heat-sink using different thermal models in otherwise identical simulation conditions, Kassel, size-ratio 1.5, fixed PV generator. . 135
C.5. Comparison of temperature cycles at heat-sink using different thermal models and with variable and fixed ambient temperatures. Other simulation conditions are identical, Kassel, size-ratio 1.5, fixed PV generator. 136

D.1. Comparison of thermal cycling damage factors obtained using different sets of climatic data in otherwise identical simulation conditions (size ratio 1.5). 137
D.2. Comparison of power cycling damage factors obtained using different sets of climatic data in otherwise identical simulation conditions (size ratio 1.5). 138

List of Tables

3.1. Important metrics of the semiconductors tested in this study. . . 31
3.2. Observed failures during long-term experiment. Applied DC voltage: 1100 V, overall experiment duration: 4572.1 h. 40

4.1. Parameters for simulation of photovoltaic system 48
4.2. Constants and parameters for model of PV module 56
4.3. Locations investigated in this study 75
4.4. Specifications of assumed photovoltaic central inverter. 75
4.5. Assumed (exemplary) curtailment levels to illustrate effect. (Previously shown in [62]) 82

6.1. Summary of qualitative comparison of IGBT TSEPs 103
6.2. Parameters found by fitting 117

A.1. Coefficients for the irradiance model by Perez et.al. [73] 128

B.1. Parameters of Foster type thermal model. Values for $Z_{th}JC$ taken from [82] 129
B.2. Parameters of the Cauer type thermal model. Obtained by transforming Foster model (see Table B.1) to Cauer model. 130
B.3. Cooling curves obtained from project partner and simulated model responses (Part 1). 131
B.4. Cooling curves obtained from project partner and simulated model responses (Part 2). 132

C.1. Damage factors due to temperature cycling - T_{case} for different thermal models and the influence of ambient temperature variation. 136

Schriftenverzeichnis Elektrische Energiesysteme

Herausgegeben von / Edited by
Kompetenzzentrum für Dezentrale Elektrische Energieversorgungstechnik

---

Band 1: Wechselrichtersysteme mit Stromzwischenkreis zur Netzanbindung von Photovoltaik-Generatoren, Kassel 2010, ISBN 978-3-89958-912-2
Benjamin Sahan

Band 2: Methode zur Evaluation leistungselektronischer Schaltungstopologien für die Anwendung in dezentralen Netzeinspeisern kleiner Leistung, Kassel 2011, ISBN 978-3-86219-094-2
Thorsten Bülo

Band 3: On the Perspectives of Wide-Band Gap Power Devices in Electronic-Based Power Conversion for Renewable Systems, Kassel 2013, ISBN 978-3-86219-486-5
Samuel Vasconcelos Araújo

Band 4: Development of Brushless Self-excited and Self-regulated Synchronous Generating System for Wind and Hydro Generators, Kassel 2014, ISBN 978-3-86219-018-8
Likaa Fahmi Ahmed Izzat

Band 5: Untersuchung eines Ringgenerators für Windenergieanlagen der 10 MW-Klasse auf Basis statischer Versuchsmodelle und numerischer Simulationen, Kassel 2014, ISBN 978-3-86219-732-3
Anna Katharina Messoll

Band 6: Modellierung der parasitären passiven Elemente in IGBT-Hoch-leistungsmodulen, Kassel 2014, ISBN 978-3-86219-752-1
Michael Heeb

Band 7: Permanentmagnetische Vormagnetisierung von Speicherdrosseln in Stromrichtern, Kassel 2014, ISBN 978-3-86219-820-7
Jens Friebe

Band 8: Analysis and Comparison of Power Electronic Converters with Electronic Isolation, Kassel 2015, ISBN 978-3-86219-822-1
Mehmet Kazanbas

Band 9: Optimierung von PV-Wechselrichtern im Netzparallelbetrieb mithilfe analytischer Verhaltens- und Verlustleistungsmodelle, Kassel 2015, ISBN 978-3-86219-924-2
Julia Pinne

Band 10: Auswirkungen der Netzintegration von Windkraftanlagen auf die Spannungsstabilität im Nördlichen Verbundsystem Chiles, Kassel 2015, ISBN 978-3-86219-986-0
Darío Lafferte

Band 11: Untersuchung des Betriebsverhaltens einer Windkraftanlage mit permanenterregten Synchrongeneratoren für den Einsatz im Offshore-Bereich, Kassel 2015, ISBN 978-3-86219-966-2
Adil Ezzahraoui

Band 12: PV-Stromrichter höherer Leistung für 1.500 V Systemspannung. Bewertung, Vergleich, Realisierung, Kassel 2016, ISBN 978-3-7376-0118-4
Christian Nöding

Band 13: Investigation on Performance Advantage of Functionally Integrated Magnetic Components in Decentralised Power Electronic Applications, Kassel 2017, ISBN 978-3-7376-0226-6
Thiemo Kleeb

Band 14: Discrete time sliding mode control strategies applied to a multiphase brushless DC machine, Kassel 2017, ISBN 978-3-7376-0318-8
Milena Sabrina Godoi Dias

Band 15: Investigation of Reliability Aspects of Power Semiconductors in Photovoltaic Central Inverters for Sunbelt Regions, Kassel 2018, ISBN 978-3-7376-0494-9
Christian Jochen Felgemacher

High reliability and system lifetimes in the range of 30 years are essential for renewable energy systems such as photovoltaic power plants to minimise costs for the generated electric energy. At the same time such systems are used in regions with high solar irradiance and also harsh environmental conditions. Therefore, designs for photovoltaic inverters need to meet not only the key design criteria of high conversion efficiency but also need to be very robust and at the same time meet challenging cost targets.

In this dissertation aspects concerning the lifetime and reliability of power semiconductors in photovoltaic central inverters are investigated. On key topic of the dissertation is the measurement of the voltage dependent failure rate due to cosmic radiation induced single-event-burnout of SiC and Si power semiconductors. The second topic is the development of a system level simulation to quantify the stress on the power semiconductors in a PV central inverters in various regions of the world. Further topics are the investigation of improved control concepts for the cooling system of PV central inverters and the monitoring of IGBT temperatures during converter operation.

ISBN 978-3-7376-0494-9

