

Device Characterization and Modeling of Large-Size GaN HEMTs

Jaime Alberto Zamudio Flores



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List of Symbols

Symbol	Description	Unit
A_{p+b_d}	Summed horizontal areas of the drain contacting pad and bus-bar	m^2
A_{p+b_g}	Summed horizontal areas of the gate contacting pad and bus-bar	m^2
BV_{gd}	Value of gate-drain off-state breakdown voltage	V
C_{ch}	Capacitance of the conduction channel impedance	F
C_{ds}	Drain-source capacitance of the intrinsic transistor	F
C_{ds0}	Total capacitance of the drain-source branch in <i>cold pinch-off</i> conditions	F
C_{dsi}	Drain-source inter-electrode parasitic capacitance	F
C_{dsi1}	Electrode-to-electrode component of the drain-source inter-electrode parasitic capacitance	F
C_{dsi2}	Electrode-to-ground component of the drain-source inter-electrode parasitic capacitance	F
C_{gd}	Gate-drain capacitance of the intrinsic transistor	F
C_{gd0}	Total capacitance of the gate-drain branch in <i>cold pinch-off</i> conditions	F
C_{gdi}	Gate-drain inter-electrode parasitic capacitance	F
C_{gg}	Capacitance of the Schottky-gate impedance	F
C_{gs}	Gate-source capacitance of the intrinsic transistor	F
C_{gs0}	Total capacitance of the gate-source branch in <i>cold pinch-off</i> conditions	F
C_{gsi}	Inter-electrode parasitic gate-source capacitance	F
C_{pds}	Drain-source parasitic capacitance related to contacting-pad, bus-bar and air-bridge effects	F
C_{pdg}	Parasitic capacitance between the drain contacting pad or bus-bar and the gate electrode	F
C_{pgd}	Parasitic capacitance between the gate contacting pad or bus-bar and the drain electrode	F
C_{pgs}	Parasitic capacitance related to the contacting pad, bus-bar and air bridges of the gate	F
C_{th}	Thermal capacitance	$s \cdot W / ^\circ C$
d_{dsi}	Metal-to-metal separation between lateral surfaces of contiguous drain and source electrodes	μm
d_{gdi}	Metal-to-metal separation between lateral surfaces of contiguous gate and drain electrodes	μm
d_{gsi}	Metal-to-metal separation between lateral surfaces of contiguous gate and source electrodes	μm
d_{pdg}	Metal-to-metal separation between the drain contacting pad or bus-bar and the gate electrode	μm
d_{pgd}	Metal-to-metal separation between the gate contacting pad or bus-bar and the drain electrode	μm

Symbol	Description	Unit
e	Electron charge ($e = 1.602176565 \times 10^{-19}$ C)	C
E_c	Critical electric field	V/cm
E_g	Energy bandgap of semiconductor materials	eV
E_{Net}	Net electric field due to the polarization dipole	V/cm
E^P	<i>Cold-pinch-off</i> -oriented error function to compare modeled and measured S-parameters	-
$E_{S,rel}$	General relative-error function to compare modeled and measured S-parameters	%
f_D	I_{ds} -model parameter for charge-trapping related to the drain voltage	S
f_G	I_{ds} -model parameter for charge-trapping related to the gate voltage	S
f_P	I_{ds} -model parameter for self-heating effects for unknown thermal resistance	A/W
f_{th}	I_{ds} -model parameter for self-heating effects for known thermal resistance	A/°C
G_P	Device power gain	dB
g_M	Device transconductance at the extrinsic device ports	dB
G_{ME}	Maximally-efficient gain	dB
G_{gdf}	Differential gate-drain diode conductance of the intrinsic transistor	S
G_{gsf}	Differential gate-source diode conductance of the intrinsic transistor	S
G_m	Device transconductance of the intrinsic transistor	S
G_{ds}	Drain-source conductance of the intrinsic transistor	S
I_{DC}	Static-DC current	A
i_{DS}	Drain current signal at the extrinsic device ports	A
I_{DS}	Static-DC drain current at the extrinsic device ports	A
I_{ds}	Drain current source of the device equivalent circuits	A
I_{ds}^{Iso}	I_{ds} -model parameter related to ideal isothermal IV characteristics	A
I_{DSS}	Static-DC drain current value in the saturation region for zero gate voltage	A
I_{gd}	Gate-drain current source of the large-signal model	A
I_{GS}	Static-DC gate current at the extrinsic device ports	A
I_{gs}	Gate-source current source of the large-signal model	A
$I_{th}(t)$	Component of transient drain current attributed to self-heating effects	A
$I_{trap}(t)$	Component of transient drain current attributed to charge trapping effects	A
k	Thermal conductivity of a material	W/m·°C
L_d	Drain parasitic inductance	H
L_g	Gate parasitic inductance	H

Symbol	Description	Unit
l_d	Length of the drain electrodes or drain fingers	μm
l_g	Length of the gate electrodes or gate fingers	μm
L_s	Source parasitic inductance	H
n	Electron density in the device conduction channel	cm^{-3}
N	Number of frequency points measured in S-parameters characterization	-
n_{fd}	Number of drain electrodes or drain fingers	-
n_{fg}	Number of gate electrodes or gate fingers	-
P_{DC}	Static-DC power	W
p_{ds}	Drain power signal at the intrinsic device ports	W
P_{ds}	Average value of the drain power at the intrinsic device ports	W
P_{DS}	Static-DC drain power at the extrinsic device ports	W
P_{DSmax}^{SOA}	Limit value of P_{DS} from the device safe-operation-area, normalized to the total gate periphery in mm	W/mm
P_{in}	Net input power signal	W
P_{out}	Net output power signal	W
$P_{piezoelectric}$	Piezoelectric field of the polarization dipole	V/cm
$P_{spontaneous}$	Spontaneous field of the polarization dipole	V/cm
Q_{gd}	Gate-drain charge source of the large-signal model	C
Q_{gs}	Gate-source charge source of the large-signal model	C
R_{ch}	Resistance of the conduction channel impedance	Ω
R_d	Drain parasitic resistance	Ω
R_{ds}	Drain-source resistance of the intrinsic transistor	Ω
$R_{DT} \cdot C_{DT}$	Time constant of V_{DS} -related charge trapping	s
R_g	Gate parasitic resistance	Ω
R_{gd}	Gate-drain resistance of the intrinsic transistor	Ω
R_{gg}	Resistance component of the impedance of the gate Schottky contact	Ω
$R_{GT} \cdot C_{GT}$	Time constant of V_{GS} -related charge trapping	s
R_i	Gate-source resistance of the intrinsic transistor	Ω
R_s	Source parasitic resistance	Ω
R_{th}	Thermal resistance	$^{\circ}\text{C}/\text{W}$
T_C	Case temperature of the device under test	$^{\circ}\text{C}$
T_{ch0}	Average value of the channel temperature	$^{\circ}\text{C}$
t_{fd}	Thickness of the lateral metal surface of the drain electrode	mm
t_{fg}	Thickness of the lateral metal surface of the gate electrode	mm
t_{lay}	Thickness of the device layer structure	nm
V_{br}	Value of drain-source off-state breakdown voltage	V

Symbol	Description	Unit
v_{DS}	Drain voltage signal at the extrinsic device ports	V
v_{ds}	Drain voltage signal at the intrinsic device ports	V
V_{ds}	Static-DC drain voltage at the intrinsic device ports	V
V_{DS}	Static-DC drain voltage at the extrinsic device ports	V
v_{GD}	Gate-drain voltage signal at the extrinsic device ports	V
v_{gd}	Gate-drain voltage signal at the intrinsic device ports	V
V_{gd}	Static-DC gate-drain voltage at the intrinsic ports	V
V_{GD}	Static-DC gate-drain voltage at the extrinsic ports	V
v_{GS}	Gate voltage signal at the extrinsic device ports	V
v_{gs}	Gate voltage signal at the intrinsic device ports	V
V_{gs}	Static-DC gate voltage at the intrinsic device ports	V
V_{GS}	Static-DC gate voltage at the extrinsic device ports	V
V_k	Knee voltage value	V
$V_{\text{Pinch-off}}$	Gate voltage value for <i>cold pinch-off</i> S-parameters	V
v_{sat}	Saturation velocity	cm/s
V_{th}	Threshold voltage value	V
w_{fd}	Unit width of the drain electrodes or drain fingers	mm
w_{fg}	Unit width of the gate electrodes or gate fingers	mm
Y_{ds}	Drain-source admittance of the intrinsic transistor	S
Y_{gd}	Date-drain admittance of the intrinsic transistor	S
Y_{gm}	Transconductance admittance of the intrinsic transistor	S
Y_{gs}	Gate-source admittance of the intrinsic transistor	S
Z_0	Characteristic impedance of transmission-line systems	Ω
Z_{ch}	Impedance of the conduction channel	Ω
Z_{gg}	Impedance of the gate Schottky contact	Ω
Z_{th}	Thermal impedance	$^{\circ}\text{C}/\text{W}$
ΔS	Determinant of the S-parameters matrix	-
ΔT	Change in average channel temperature	$^{\circ}\text{C}$
α	Partitioning parameter of the channel impedance corresponding to the gate-length region	-
β	Partitioning parameter of the channel impedance corresponding to the gate-source region	-
ϵ_{air}	Dielectric constant of air	F/m
ϵ_{gdi}	Dielectric constant of the region between contiguous gate and drain electrodes	F/m
ϵ_{gsi}	Dielectric constant of the region between contiguous gate and source electrodes	F/m
ϵ_{lay}	Dielectric constant of the device layer structure	F/m
ϵ_0	Dielectric constant of vacuum ($\approx 8.85 \times 10^{-12}$ F/m)	F/m

Symbol	Description	Unit
η_D	Drain efficiency	%
μ	Electron mobility	$\text{cm}^2/\text{V}\cdot\text{s}$
σ	Conductivity in the device conduction channel	S/m
τ	Transconductance delay due to propagation time	s
τ_{th}	Time constant of self-heating effects	s
τ_{trap}	Time constant of charge trapping effects	s
$[Y^{CR}]$	Y-parameter matrix of the device in <i>cold reverse</i> conditions	S
$[Y^{Int}]$	Y-parameter matrix of the intrinsic transistor	
$[Y^P]$	Y-parameter matrix at the extrinsic device ports in <i>cold pinch-off</i> conditions	S
$[Y^{Total}]$	Y-parameter matrix at the extrinsic device ports	S
$[Z^{RCold}]$	Z-parameter matrix of the device in <i>cold</i> conditions after subtraction of extrinsic reactive effects	Ω

List of Abbreviations and Acronyms

2DEG	Two-dimensional electron gas
3D	Three-dimensional
3G	Third generation
4G	Fourth generation
6D	Six-dimensional
AC	Alternating current
ACPR	Adjacent-channel power ratio
ADS [®]	Advanced design system [®]
ANN	Artificial neural networks
BS	Base station
CAD	Computer-aided design
CMOS FETs	Complementary metal-oxide-semiconductor field-effect transistors
CW	Continuous wave
DAC	Data-access component
DC	Direct current
DiVA [®]	Dynamic current-voltage analyzer [®]
DSP	Digital signal processing
DSSS	Direct-sequence spread-spectrum
FBH	Ferdinand-Braun Institute for Highest-Frequency Engineering (German: <i>Ferdinand-Braun-Institut für Höchstfrequenztechnik, Berlin, Germany</i>)
FDD	Frequency-division duplexing
FET	Field-effect transistor
FG	Department (German: <i>Fachgebiet</i>)
IAF	Fraunhofer Institute for Applied Solid-State Physics (German: <i>Fraunhofer Institut für Angewandte Festkörperphysik, Freiburg im Breisgau, Germany</i>)
FP	Field plate
GPB	General purpose interface bus
HBT	Heterojunction bipolar transistor
HEMT	High-electron mobility transistor
HFET	Heterojunction field-effect transistor
HFT	High-frequency technique (German: <i>Hochfrequenztechnik</i>)
IEMN	Institute of electronics, microelectronics and nanotechnology (French: <i>Institut d'électronique de microélectronique et de nanotechnologie, Lille, France</i>)
IMD	Intermodulation distortion
IMD3	Third-order intermodulation distortion
ITU	International Telecommunications Union
IV	Current-voltage
LDMOS	Laterally diffused metal-oxide-semiconductor

LTE	Long term evolution
MESFET	Metal-semiconductor field-effect transistor
PAE	Power-added efficiency
RC	Resistive-capacitive
RF	Radio frequency
SEM	Scanning electron microscope
SDD	Symbolically defined device
S-c FP	Source-connected field plate
SOA	Safe-operation area
SOLT	Short-open-load-through
UMTS	Universal mobile telecommunications system
VNA	Vector signal network analyzer
WCDMA	Wideband code-division multiple access
WiMAX	Worldwide-interoperability-for-microwave access (Based on the IEEE 802.16 Standard)

Abstract

Material properties of wide-bandgap semiconductors, like SiC and GaN, are ideal to build transistors for highly-linear highly-efficient power amplifiers. AlGaIn/GaN HEMTs represent the most promising type of wide-bandgap devices, because they combine the material properties of GaN with the operation principle of HEMTs.

This dissertation presents a large-signal modeling strategy for power AlGaIn/GaN HEMTs that is oriented to the computer-aided design of power amplifiers for the UMTS technologies of the 3G and 4G standards of cellular communications.

The modeling strategy is formulated to account for the key effects observed in advanced large-size GaN transistors, such as complex parasitic effects and low-frequency dispersion induced by charge-trapping and self-heating effects. At the same time, the formulation maintains a clear physical interpretation of the model parameters, allowing a meaningful insight in the device physics.

The models developed in this thesis work represent the device with electrical equivalent circuits and are empirical, so that parameter calculation is performed on the basis of electrical device characterization. Initially, a small-signal model is developed based on S-parameter measurements. The small-signal parameter extraction starts finding the extrinsic capacitance values, continues with the extrinsic inductance and resistance values and then calculates voltage-dependent values of the intrinsic parameters. The small-signal model is the foundation for the later development of the large-signal model. For the latter model, pulsed-DC IV measurements are used as database for a dispersive- I_{DS} model.

Unstable operation was observed during pulsed-DC IV measurements on large-size (large-transconductance) devices at bias points with non-negligible dissipated power. This was overcome with the successful application of a stabilization technique, removing the related constraints to quality and size of the achievable database.

A comprehensive equivalent circuit is adopted for the small-signal model that contains 10 bias-dependent intrinsic and 12 bias-independent extrinsic elements, with six extrinsic capacitance parameters.

Relationships between those six capacitance parameters and device capacitive effects are exposed in detail, leading to original closed expressions for those parameters in terms of physical features of the device structure. These novel expressions are not evaluated directly, instead of this, they are used to formulate capacitance ratios.

An extraction algorithm for the comprehensive 22-element equivalent circuit has been reported before by other authors, using capacitance ratio values and S-parameter measurements. However, the basic assumptions of such algorithm are perfected in this thesis work in the following two ways:

A) The required capacitance ratios are evaluated combining capacitance parameter expressions related to physical device features with top-view photographs of the finger layout. This gives ratios that are usable with high generality.

B) The influences of finger layout features of advanced large-size HEMTs, i.e. field plates and source air bridges, on the capacitance ratio values are taken into account for the first time, assuring that the assumptions behind the capacitance ratio values are physically sound.

A novel extrinsic resistance extraction based on *cold reverse* S-parameter measurements is presented to complement the calculation of high-quality measurement-correlated values for all extrinsic parameters. The *cold reverse* bias point is preferred over the usual *cold forward*, because in this thesis, that latter bias point was confirmed to be case-specific for GaN devices and potentially unsafe for the transistors.

The calculated extrinsic parameter values produce intrinsic parameters with the expected frequency- and voltage-dependency. S-parameters simulated with the developed small-signal models agree well with measurements on over a thousand active bias points distributed on all IV regions. For example, the percent error from modeled and measured S-parameters, defined as $100\% \cdot |S^{model} - S^{meas}| / |S^{meas}|$, averaged over the four S-parameters, over 197 frequency points from 0.4 to 10 GHz and over nearly 1200 active bias points, was 2.05% for the small-signal model of a 3.2-mm AlGaIn/GaN HEMT.

The extracted parameter values of the small-signal model scale accordingly with the scaling of device size, with singular deviations that are reasonably explained. Two models for a 3.2-mm device were obtained applying scaling rules to models of smaller devices: One through the

scaling of a 2-mm device model and another through the scaling of a 0.5-mm device model. Those indirectly-obtained models show good agreement with measured S-parameters, proving the model scalability.

The large-signal model includes a non-quasi-static formulation of the gate charge and a dispersive- I_{DS} model. Non-quasi-static parameters are calculated from small-signal intrinsic parameters using well-known path-integrals. The I_{ds} -model parameter extraction was demonstrated fully based on pulsed-DC IV and I_{DS} transient measurements, including the time constants of charge-trapping and self-heating effects. This highlights the empirical character of the modeling strategy of this thesis: For the first time each and every model parameter is demonstrated to be obtained from device characterization.

Large-signal models for two large-size AlGaIn/GaN HEMTs are developed and directly implemented in CAD-software to perform model simulations and compare them with measurements. One model was for a transistor built on a substrate of Si with total gate width of 2-mm and another for a transistor built on SiC with total gate width of 3.2-mm. These two models accurately simulate S-parameters and pulsed-DC IV measurements for different bias points, including points usually employed for the design of class-AB, class-B and class-C power amplifiers.

Furthermore, the developed large-signal models were tested with single-tone and two-tone stimuli, using input signal frequencies and spacing related to the frequencies of UMTS technology. In such tests the models provide accurate predictions compared to measurements of output powers of the fundamental, 2nd and 3rd harmonics and of IMD3 products, for bias points typically used to design class-AB, class-B and class-C power amplifiers.

In single-tone tests, output power is predicted correctly up to 37 dBm, approximately equivalent to 2.5 W/mm. On two-tone tests, the models predict accurately the input powers and bias point ranges where IMD3 *sweet spots* are measured.

Zusammenfassung

Die Eigenschaften von Halbleitern mit großer Bandlücke, z. B. SiC und GaN (Siliziumcarbid und Galliumnitrid), sind ideal für die Herstellung von Transistoren für hochlineare und effiziente Leistungsverstärker. Dabei sind AlGaIn/GaN-HEMTs besonders vielversprechend, denn sie miteinander verknüpfen die hervorragenden Materialeigenschaften von GaN und die vorteilhafte Funktionsweise eines HEMTs.

Die vorliegende Dissertation stellt eine Strategie zur empirischen Großsignalmodellierung von AlGaIn/GaN-Material-basierten Leistungs-HEMTs vor, die den rechnergestützten Entwurf von Leistungsverstärkern, beziehend auf UMTS-Technologien der 3G und 4G Mobilfunkstandards, zum Ziel hat.

Die beschriebene Modellierungsstrategie berücksichtigt die wesentlichen physikalischen Effekte, die in modernen großflächigen GaN-Transistoren zu erwarten sind, wie z. B. komplexe parasitäre Layout-Effekte sowie Effekte der Niederfrequenzdispersion, die ihre Ursache in Trapping- und Eigenerwärmungseffekten haben. Zudem erlaubt die Modellformulierung eine eindeutige physikalische Interpretation der Modellparameter sowie einen Einblick in die Bauelementephysik.

Die in dieser Arbeit entwickelten Modelle stellen den Transistor durch Ersatzschaltbilder dar; sie sind empirisch, d. h. ihre Parameterbestimmung beruht auf der elektrischen Charakterisierung des Bauelements. Zunächst wird ein Kleinsignalersatzschaltbild hergeleitet, das auf S-Parameter-Messungen basiert. Die Extraktion der Kleinsignalparameter beginnt mit der Bestimmung der extrinsischen Kapazitätswerte; es folgt dann die Bestimmung der extrinsischen Induktivitäts- und Widerstandswerte. In einem letzten Schritt werden die arbeitspunktabhängigen Werte der intrinsischen Modellparameter bestimmt. Das Kleinsignalmodell dient als Basis für die weitere Entwicklung eines Großsignalmodells. In dem Großsignalmodell, die Modellierung des dispersiven Drainstroms (I_{DS}) erfolgt auf der Grundlage von gepulsten DC-IV-Messungen.

Bei den gepulsten DC-IV-Messungen an großflächigen und mit entsprechend hoher Steilheit versehenen Transistoren treten Instabilitäten in Arbeitspunkten auf, in denen die Verlustleistung nicht mehr gering ist. Dieser unzulängliche Zustand konnte durch eine Stabilisierungstechnik überwunden werden, so daß die zunächst teilweise aufgetretene Meßdaten-

Streuung bereinigt und darüber hinaus die Datenbasis erweitert werden konnte.

Ein erweitertes Ersatzschaltbild wurde dem Kleinsignalmodell zugrunde gelegt; es enthält zehn arbeitspunktabhängige intrinsische und zwölf arbeitspunktunabhängige extrinsische Elemente, dazu sechs extrinsische kapazitive Modellparameter.

Ein Zusammenhang zwischen den sechs extrinsischen kapazitiven Parametern und den kapazitiven Bauelementeffekten wird hergestellt. Dies führt zu originären geschlossenen mathematischen Ausdrücken dieser Modellparameter, die unmittelbar die physikalischen Eigenschaften der Bauelementstruktur widerspiegeln. Diese neuartigen Gleichungen werden nicht direkt ausgewertet, sondern in Form von Kapazitätsverhältnissen weiter genutzt.

Es wurde bereits in der Literatur über einen Algorithmus zur Extraktion eines 22-Elemente-Ersatzschaltbildes berichtet, welcher auf S-Parameter-Messungen und definierten Kapazitätsverhältniswerten beruht. Grundlegende Annahmen für die Kapazitätsverhältniswerten dieses Algorithmus werden in dieser Dissertation hinterfragt und schließlich in den folgenden zwei Punkten verbessert:

A) Die Kapazitätsverhältnisse, die in der Extraktion des 22-Elemente-Ersatzschaltbildes benötigt sind, werden aus Draufsicht-Photographien des Fingerlayouts von den jeweils untersuchten Transistoren herangezogen und ausgewertet. Die Verwendung analytischer Ausdrücken für die Kapazitäten bsw. Kapazitätsverhältnisse, welche spezifisch für jedes Bauelement ausgewertet werden können, bedeutet eine hohe anwendungstechnische Allgemeingültigkeit für die Extraktion.

B) Erstmalig werden Einflüsse des Fingerlayouts von fortschrittlichen großflächigen HEMTs, die beispielsweise Feldplatten und Luftbrücken in der Source-Elektrode aufweisen, bei der Bestimmung der extrinsischen Kapazitäten bzw. Kapazitätsverhältnisse berücksichtigt, so daß ihre Werte physikalisch begründet sind.

Es wird eine neuartige Verfahren zur Extraktion der extrinsischen Widerstände vorgeschlagen, das auf *cold-reverse* S-Parameter-Messungen basiert; es erweitert die Bestimmung Messung-bezogener Werte auf alle extrinsischen Modellparameter. Gegenüber dem üblichen *cold-forward* Arbeitspunkt hat der *cold-reverse* Arbeitspunkt den Vorteil, daß bei den in

dieser Arbeit untersuchten GaN Leistungstransistoren kein Ausfallrisiko besteht.

Die berechneten Werte der extrinsischen Modellparameter führen zu intrinsischen Parametern, die die erwartete Frequenz- und Arbeitspunkt-abhängigkeit aufweisen. S-Parameter, die mit Anwendung der abgeleiteten Kleinsignalmodelle simuliert wurden, stimmen gut mit Messungen überein, und das in über tausend Arbeitspunkten im gesamten IV-Kennlinienfeld. Beispielsweise beträgt der prozentuale Fehler 2.05% für das entwickelte Kleinsignalmodell eines 3.2-mm Bauelements. Dabei ist der Fehler als $100\% \cdot |S^{model} - S^{meas}| / |S^{meas}|$ definiert, wobei über die vier S-Parameter in 1200 verschiedenen aktiven Arbeitspunkten mit jeweils 197 Frequenzpunkten im Frequenzbereich von 0.4 bis 10 GHz gemittelt wurde.

Die Werte der Kleinsignalmodellparameter skalieren im Einklang mit der Skalierung der Bauelementgröße; wenige Ausnahmen werden jeweils begründet.

Zwei Modelle werden für einen 3.2-mm Transistor auf der Grundlage der abgeleiteten Skalierungsregeln aus Modellen kleinerer Transistoren entwickelt: Eines auf der Basis eines 2-mm Transistors und eines auf der Basis eines 0.5-mm Transistors. Beide indirekt erzeugten Modelle zeigen eine gute Übereinstimmung mit gemessenen S-Parametern, was die Modellskalierbarkeit unterstreicht.

Das angewendete Großsignalmodell beinhaltet eine nicht-quasistatische (dispersive) Formulierung der Gate-Ladung und der I_{DS} -Stromquelle. Die nicht-quasi-statische Parameter werden wie üblicherweise aus intrinsischen Kleinsignalparametern über Integration gewonnen. Die Extraktion des Modells der dispersiven I_{DS} -Stromquelle auf der Grundlage gepulster DC-IV- sowie transienter I_{DS} -Messungen, einschließlich der Zeitkonstanten von Trapping- und Eigenerwärmungseffekten, wird eingehend beschrieben. Dies hebt den meßtechnischen Charakter der Modellierungsstrategie in dieser Arbeit hervor: Erstmals wird gezeigt, wie über die meßtechnische Bauelementcharakterisierung alle Modellparameter gewonnen werden.

Es werden Großsignalmodelle für zwei unterschiedliche großflächige AlGaIn/GaN HEMTs hergeleitet und in eine CAD-Software implementiert, um Modellsimulationen durchzuführen und sie mit Messungen der untersuchten Transistoren zu vergleichen. Es handelt sich um ein Modell für einen auf Si Substrat gebauten Transistor mit 2-mm Gesamtgatebreite und eines für einen auf SiC Substrat gebauten Transistor mit 3.2-mm

Gesamtgatebreite. Die beiden Modelle simulieren zutreffend S-Parameter- und gepulste DC-IV-Messungen in mehreren Arbeitspunkten, insbesondere auch in solchen, die üblicherweise in dem Entwurf von Leistungsverstärkern im AB-, B- und C-Betrieb Verwendung finden.

Außerdem, simulationen der hergeleiteten Großsignalmodelle werden mit Messungen mit Eintons- und Zweitonsignalen getestet, wobei UMTS-bezogene Frequenzen und Frequenzabstände verwendet wurden. Die Tests zeigen, daß die Modelle in Übereinstimmung mit Messungen in der Lage sind, zuverlässig die Ausgangsleistung der ersten drei Harmonischen sowie der IMD3-Intermodulationsprodukte in typischen Arbeitspunkten von Leistungsverstärkern im AB-, B- und C-Betrieb vorherzusagen.

Bei Eintontests wird die Ausgangsleistung bis zu 37 dBm, entsprechend 2.5W/mm, korrekt simuliert. Bei Zweitontests simulieren die Modelle zuverlässig die Ausgangsleistungen und die Arbeitspunktbereiche, in denen „sweet-spots“ im Verlauf von IMD3-Intermodulationsprodukten auftreten.

Chapter 1

Introduction

Cellular telephony consists of mobile stations, the mobile phones, linked through space by a network of fixed base stations geographically distributed in cells, as illustrated in Figure 1.1. The term “mobile communications” is frequently used referring to cellular telephony, in spite of other forms of mobile communication (e.g. via-satellite), this is maybe due to the marketing boom of mobile phones. Cellular telephony or mobile communications probably represent the most rapidly adopted technology in history. By the end of 2010, it has been with us close to 30 years and is now the most widespread and popular personal technology, with around 5.3 billion subscribers worldwide [1].

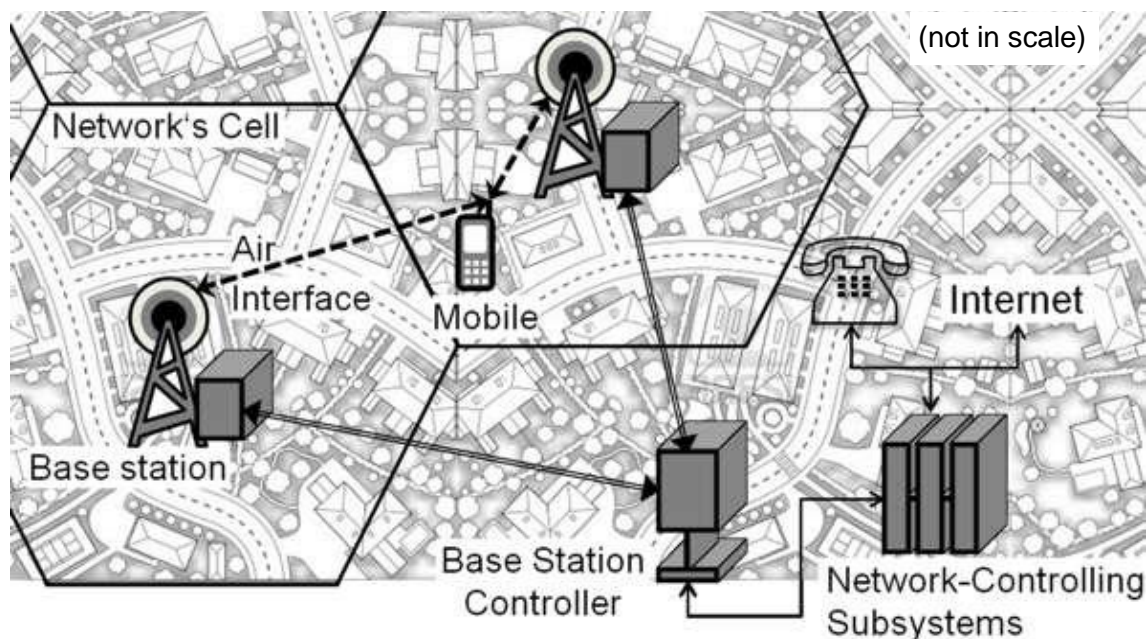


Figure 1.1 Main subsystems and links of a 3G mobile communication network.

Technical standards of cellular telephony were developed, so that the systems could function together, independent of the provider company or employed technology. The newest standard generations, 3G and 4G, as defined by the International Telecommunications Union (ITU) that directs the standardization tasks, should be able to provide mobile Internet access with transmission data rates of 2 and 100 Mbps, respectively [1, 2].

Commercial services branded 4G have been launched to the public, but are based on Long Term Evolution (LTE) technology that is a bridge towards 4G, but still part of the 3G, by ITU definitions [2]. At the time of writing this thesis, the actual 4G technology had not yet been defined by ITU.

The most widespread technological implementation of the 3G standard is called Universal Mobile Telecommunication System (UMTS). The definition of UMTS by ITU includes a method to control the access to the communication channel by the mobile and base stations, known as Wideband Code-Division Multiple-Access (WCDMA). WCDMA uses a modulation technique known as direct-sequence spread-spectrum (DSSS). Modulation reshapes the information created by the mobile and base stations so that it is better transmitted through the channel. Modulation of WCDMA allows a highly shared usage of the channel bandwidth [2]. The bandwidth is the frequency band assigned for the signals transmitted in the communication channel. ITU defined UMTS with frequency bands of 1.92-1.98 GHz for the uplink and 2.11-2.17 GHz for the downlink, channel bandwidth of 5 MHz and channel spacing of 200 kHz [2].

1.1 Elements of the UMTS Technology

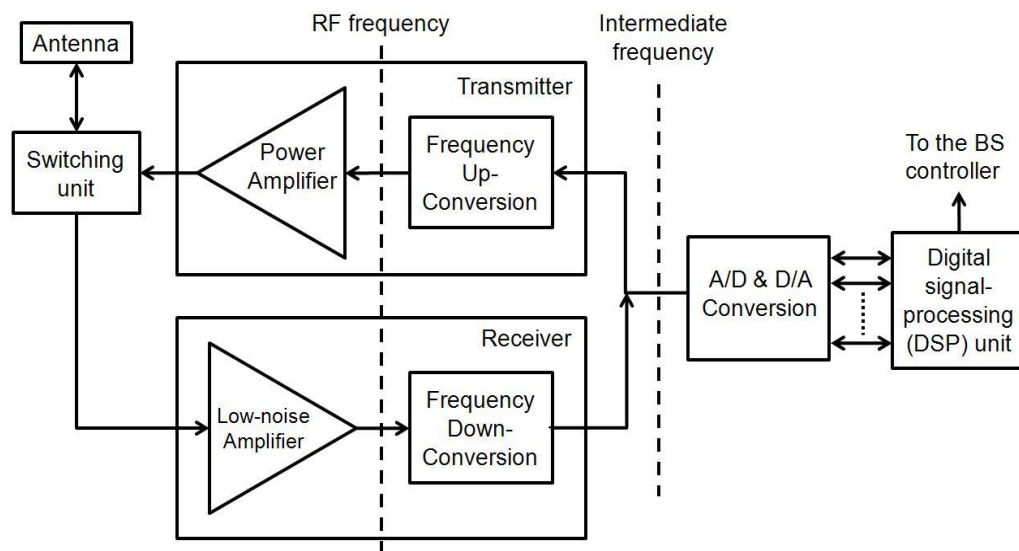


Figure 1.2 Block diagram of a conventional UMTS base station.

Figure 1.2, drawn after the functional descriptions and diagrams of [3, 4], shows the main blocks of a conventional UMTS base station. The antenna detects or propagates the communication signals. The receiver shapes up the detected signals so that they can be processed. The DSP unit processes information to and from the base station controller. The

transmitter shapes up the signals for their optimal propagation and its key circuit is a power amplifier, which amplifies the electrical power of the information-carrying signals. Signals with high electrical power are required by the antenna to cover wide geographical areas.

Figure 1.3 shows the elements and basic configuration of power amplifier. Its DC supplies provide signals constant in time, whereas the RF input and output are radio-frequency time-varying signals. Thus, basically put, power amplifiers “convert” electrical power of its DC-supplies to add it to the power of the RF input signal and deliver the result of the sum as an RF output signal.

As shown in Figure 1.3 the transistor is a key element of the power amplifier. Transistors are three-terminal devices in which the signal applied at one pair of terminals controls the current signal that flows through other pair of terminals. Figure 1.3 shows the symbol of a field-effect transistor (FET) that is the type of device most commonly used in modern mobile communications systems.

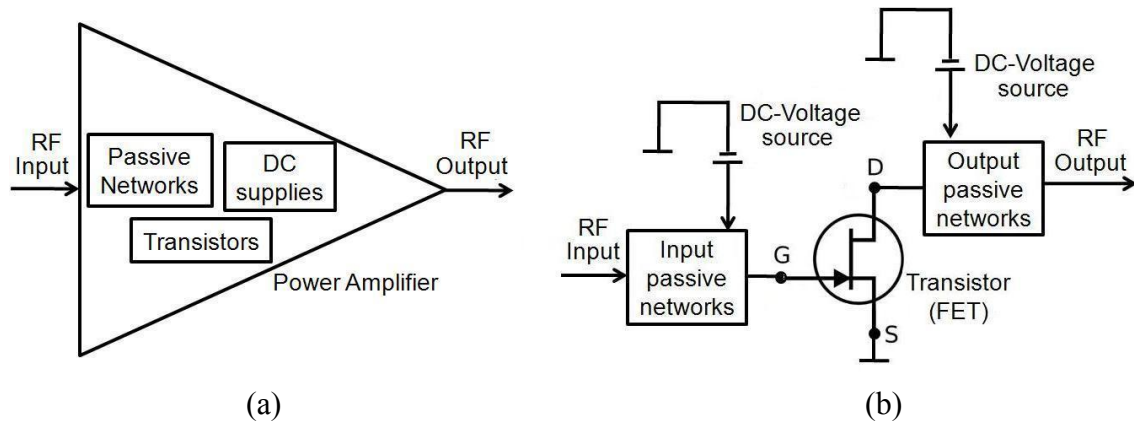


Figure 1.3 (a) Elements of the power amplifier (b) and basic configuration.

The terminals of the FET are known as gate (G), drain (D) and source (S), and the controlling signal is the voltage between the gate and the source, known as gate-source voltage (v_{GS}) or gate voltage. The controlled signal is the current through the drain and the source, known as drain-source current (i_{DS}) or drain current. The voltage between these terminals is known as drain-source voltage (v_{DS}) or drain voltage. The conversion factor of gate voltage into drain current (i_{DS}/v_{GS}) is known as the FET transconductance (g_M) and it gives the transistor its defining characteristic: The ability to amplify signals.

Power amplifiers exploit this transistor characteristic to perform their task in the transmitters: Due to the transconductance, the power of the RF

signal at the amplifier output (RF P_{out}) can be notably greater than the power of the signal at the input (RF P_{in}). The ratio P_{out}/P_{in} is the factor of power amplification, known also as power gain (G_P).

Modern transistors are fabricated stacking semiconductor layers on a material that serves as basis or foundation, then, metallic electrodes are placed at the top of the layer structure. The basis material is known as substrate layer and is a semiconductor available in wafers, for example silicon. The operation of these transistors is based on the properties of current conduction (movement of charge carriers, i.e. electrons) in the layers above the substrate, known as active layers.

1.2 Transistors with Wide-Bandgap Semiconductors for UMTS

Semiconductor materials with wide energy bandgap, like gallium nitride (GaN), diamond, sapphire and silicon carbide (SiC), are being proposed for the power amplifier transistors of modern and future mobile communications [5].

Physical properties of wide-bandgap semiconductors make devices fabricated with active layers of these materials ideal candidates for high temperature, high frequency and high power operation, as shown in the following Chapter 2. Wide-bandgap transistors are expected to overcome the performance of the currently dominant devices based on silicon (Si) and gallium arsenide (GaAs) [5].

Published research about different types of GaN FETs is at hand, but HEMTs (high-electron mobility transistors) are the most widespread and advanced form of GaN devices. GaN HEMTs are expected to decrease operation costs of UMTS base stations, which will make this technological solution commercially competitive versus the currently dominant solution based on devices built with silicon and gallium arsenide [6].

1.3 Transistor Modeling for Power Amplifier Design

The design of power amplifier improves using models of its components that can be implemented in a computer-assisted design (CAD) environment, because models allow to iterative simulation of performance of the circuit variants, so that the designer can find an optimal circuit

version before fabrication. This minimizes the iterations of fabrication that are required to achieve a successful prototype. The transistor is the most important power amplifier component to be modeled and the correctness of this modeling is critical for the circuit design.

Transistor modeling can help to evaluate and improve the process of device fabrication, linking measured performances with material properties and device structure. For this, the model parameters must maintain a correlation with physical phenomena or effects.

Small-signal models are the initial approach to transistor modeling and consist of *linearizations* around an operation point of the device nonlinear effects. However, accurate description of key nonlinear effects of modern transistors requires more complete models, known as large-signal models.

Large-signal modeling of GaN HEMTs is a hot research topic, due to the novelty of the processing technology related to these materials and the strong nonlinear effects observed in these devices [7].

1.3.1 Proposed Type of Modeling

This section gives basic concepts of transistor modeling that are necessary to introduce later the type of models developed in this thesis work. Transistor models can be generally classified as follows:

1. Physics models use physical data, e.g. geometric dimensions and material properties of the layers, to solve physics equations describing the device response (voltage, power, temperature, etc.).
2. Empirical models calculated on the basis of experimental data, like electrical measurements realized on the device, also called measurement-based models. These models use electrical equivalent circuits to relate the device response and the input signals, the circuit elements represent the effects to be modeled.

Real values of material properties or dimensions as needed by physics models are hardly available for commercial devices. These models are specific to a device technology and can be hard to apply in CAD of power amplifiers, since they are formulated and calculated in other software [8].

Empirical models are easier to apply in CAD of power amplifiers than physics models, giving faster simulations [8]. They also allow moderate

insight of device physical phenomena, if the model parameters are linked to physical effects. The model accuracy depends on the measurement accuracy of the data used to develop the model, and on the adequacy of the model formulation. The database consists of specific measurements sets that must cover the desired ranges and conditions of operation. Potential drawbacks are errors due to measurement techniques and to interpolation, the model customization to a specific circuit design and the possible need of large amounts of measurements.

Empirical models known as *compact* models represent the key device nonlinearities with parametric equations in terms of the input signals. Most *compact* models find the parameter values of the main nonlinearities by fitting the equations to measured data with mathematical optimization.

Other types of empirical models represent parameters of the equivalent circuit as multidimensional matrixes, instead of using parametric equations, and thus are known as table-based models. The employed matrixes are obtained by processing measured data. This modeling approach can describe device behavior in regions where *compact* models fail to fit the measured data with parametric equations [9]. Many table-based models are reported to be calculated without using mathematical optimization to process the database, then, model calculation is faster than in *compact* models and physical meaning of the model parameters is preserved.

Mathematical optimization can ease the parameter identification in very complex models, but if used carelessly, the physical interpretation of the parameters is lost. For novel device technologies, like GaN HEMTs, with complex phenomena still under investigation, there is a reasonable need to preserve the physical meaning of the model parameters.

The models developed in this thesis work are measurement-based, use equivalent circuits and table-based parameters, as shown in later chapters.

The main challenges of modeling GaN HEMTs considered in this thesis work are connected to physical phenomena that appears in wide-bandgap semiconductors or to physical features that are characteristic of modern devices for high-power amplifiers.

1.3.2 Challenges of Modeling Transistors of Wide-Bandgap Semiconductors

Performance shortcomings of power amplifiers, like the reduction of expected dynamic range, distortion of the amplified signals and increased interference between adjacent bandwidths, have been connected with dispersive behavior of the transistor electrical response [6]. The dispersion of the transistor response is partly attributed to physical phenomena known as charge trapping [10], which appear more if the active layers have different crystalline lattice than the substrate material [11], as it happens in GaN devices. These devices are fabricated in substrates of other materials, because GaN wafers for the substrate layer are unavailable [10]. Chapter 2 gives more details about dispersion of the device response, the charge trapping phenomena and its causes. In general, devices with strong dispersion are more complex to model accurately.

The high levels of output power per device size, i.e. power densities, and high operation temperatures that are typical of GaN devices have the drawback of enhancing certain unwanted effects known as self-heating effects [7]. Self-heating effects cause or stress a nonlinear behavior known as thermal memory, which is the undesired dependency of present output signals on previous input signals and states of the device, and which is considered a source of dispersion of the response in GaN devices [7]. Accurate representation of the thermal effects is therefore a characteristic challenge of modeling GaN transistors.

1.3.3 Challenges of Modeling Advanced Large-Size Transistors for High-Power Amplifiers

It is desirable to fabricate larger devices that generate higher output powers, in order to widen the linear dynamic range of power amplifiers built with such transistors and to overcome the comparative drawback of cost of GaN devices with respect to their competitors.

Besides, advanced devices for power amplifiers use a feature known as field-plate technology (which is explained in the following Chapter 2) to improve the output power performance.

In another hand, undesired effects that are inherent to the transistor operation are known as parasitic effects. Both the increased device size and the field-plate technology notably accentuate the parasitic effects, making

the devices more complex to model. The immaturity of the device fabrication process that is associated with the novelty of GaN technology also stresses parasitic effects.

If the modeling is strongly based in electrical measurements, direct modeling of large devices can face complicated issues regarding measurement techniques, due to the required high ratings of voltage, current or power. In that case, models that can be scaled according to transistor size are more interesting.

Because of the complex parasitic and nonlinear effects, modeling GaN devices with equivalent electric circuits requires more comprehensive networks with more parameters. However, more model parameters leads to an increase in complexity of the method used to calculate them and the size of the database required. For a fixed database, as the models become more complex they usually need to apply mathematical optimization to find the parameter values. Intense use of mathematical optimization has the drawbacks of emphasizing local-minima problems and obscuring the physical interpretation of the model parameters.

1.4 Main Objectives of the Research Work

The main purpose of this thesis is to investigate a large-signal modeling strategy for large-size GaN HEMTs for the design of power amplifiers applied in modern mobile communications. It is pursuit:

- To formulate the modeling strategy comprehensively to represent the complex effects of modern GaN HEMTs, and to produce accurate predictions of performance relevant for UMTS power amplifiers.
- To maintain the physical interpretation of the model parameters as much as possible.
- To base the calculation of the model parameters on electrical measurements or on data that is commonly accessible, to maintain a high generality of application of the model.
- To keep a moderate size of the database for modeling that is reasonably easy to acquire.
- To assure an accessible implementation of the model in CAD-software.

Another objective is to study the scalability of the model, as a possible alternative solution to the direct modeling of large-size devices.

1.5 Outline of the Thesis

Chapter 1 introduces the reader into the research field, providing a guideline to the general problematic of the thesis, from the everyday-world topic of cellular communications into the specific aspects of transistor modeling for power amplifiers of modern mobile communication technologies; and also, stating the main objectives of the research work.

Chapter 2 clarifies the advantages and drawbacks of wide-bandgap semiconductors to be used in the fabrication of transistors, comparing GaN with currently-used materials. That chapter also gives an insight on the principle of operation of HEMTs and on the related effects, presenting the specific challenges for transistor modeling of GaN HEMTs.

Chapter 3 deals with the initial subtask of the modeling strategy: The device characterization. It explains the database that is used later to find the values of the model parameters. Besides, a description is given of the different operation modes in which the measurements are performed, as well as the equipment and test-benches required, mentioning the practical problems faced in that modeling subtask and presenting solutions.

The proposed modeling strategy is divided in two stages. The first stage is called small-signal modeling and is treated in Chapter 4, explaining the model formulation and why it is chosen. Chapter 4 also delineates the methods to find the values of the model parameters and exemplifies the application of the methods with measured data of the studied transistors. The prospected scaling of the model parameters is also presented there.

Chapter 5 presents the key results of the small-signal modeling stage, and the tests carried out to verify the validity of the model and its parameters. Results of scaled models are also reported in that chapter, and the model scalability is examined.

Chapter 6 deals with the ideas adopted in this thesis work regarding the large-signal modeling stage. The model formulations is presented and reasoned, and the methods to identify the model parameters are explained. Such methods are illustrated applying them to measured data until the resulting values of the large-signal model parameters are found.

Chapter 7 presents and discusses the tests carried out to verify the validity of the complete large-signal model. Comparisons of model predictions with large-signal measurements of the studied transistors are reported and analyzed using different types of stimuli and operation conditions.

In the final Chapter 8, the conclusions of this thesis are presented, as well as an outlook of future work.

Chapter 2

GaN HEMTs for UMTS Power Amplifiers

Devices fabricated with active layers of wide-bandgap semiconductors, like GaN and SiC, are considered ideal candidates for UMTS power amplifiers due to the physical properties of those materials [10]. The following subchapter 2.1 compares material properties of different semiconductors employed to fabricate devices, with respect to their optimality for power amplifier performance. Most of the available research on wide-bandgap semiconductors focuses on GaN HEMTs, so subchapter 2.1 also shows the advantages of these devices with respect to other device types that are present competitors in the field of power amplification.

The nature and benefits of the traits of GaN HEMTs, their structure and principle of operation are explained in subchapter 2.2.

2.1 GaN HEMTs Compared with Devices of Other Semiconductors for UMTS Power Amplifiers

2.1.1 GaN Compared with GaAs, Si and SiC

Conclusions of several publications [5, 8, 10-14] indicate that device performance for power amplification improves if the material properties of the device semiconductor change as follows:

- Higher energy bandgap E_g
- Higher breakdown field E_c
- Higher electron mobility μ
- Higher electron saturation velocity v_{sat}
- Higher thermal conductivity k
- Lower dielectric constant ϵ .

Table 2.1 lists values (collected from references [5, 10, 12]) of these properties for bulk materials like GaN, SiC, diamond, Si and GaAs. GaN and SiC are the most promising wide-bandgap semiconductors for devices of power amplifiers, whereas Si and GaAs are being commonly used for these applications. For each property, the cells corresponding to the three best values are shaded in the table, to ease the comparison.

Table 2.1 Comparison of values of material properties for different semiconductors.

Property of bulk material [unit]	GaN	4H-SiC	Diamond	GaAs	Si
Bandgap [eV]	3.4	3.2	5.5	1.4	1.1
Electron mobility at 300 °K [$\text{cm}^2/\text{V}\cdot\text{s}$]	440	700	1900	4000	1500
Electron saturation velocity [10^7 cm/s]	2.5	2.0	2.7	1.0	1.0
Breakdown field [MV/s]	3.3	3.0	5.6	0.4	0.3
Thermal conductivity [$\text{W}/\text{cm}\cdot^\circ\text{K}$]	1.3	3.7	20	0.5	1.5
Relative dielectric constant [-]	9.0	10.0	5.5	12.8	11.8

Present research on diamond devices is in its early stages, despite its relatively better properties than GaN and SiC, mainly due to the related high costs of production and the complexity of the fabrication process [13].

The possibility to fabricate devices with higher values of electron mobility than in bulk materials (HEMTs) is well-known for GaAs [14] and GaN [10]. Thus, the low value for bulk GaN in Table 2.1 does not mean a real drawback, whereas the values of the other properties for GaN and SiC allow better performances in power amplifiers than GaAs and Si [15].

2.1.2 GaN Compared with SiC

The ability to form heterojunctions with GaN allows the fabrication of HEMTs that have higher values of electron mobility than bulk GaN (up to $6160 \text{ cm}^2/\text{V}\cdot\text{s}$ [16]) than SiC MESFETs ($700 \text{ cm}^2/\text{V}\cdot\text{s}$ of bulk SiC), making GaN a more attractive material [17].

In GaN HEMTs, electron density in the conduction channel, n , is also increased, causing higher conductivity values, σ , (since σ is proportional to the product $\mu \cdot n$) and higher maximum values of drain current and linear output power [16].

Table 2.1 shows that the thermal conductivity of bulk materials is nearly three times larger for SiC than for GaN. In the praxis, this is overcome using SiC within the fabrication of GaN devices, as substrate layer, which equalizes their thermal capabilities to those of bulk SiC [18].

2.1.3 GaN HEMTs Compared with LDMOS FETs of Si

Material properties of Si for power amplifier performance, like wide bandgap and high breakdown field, can appear suboptimal from the examination of Table 2.1. Nonetheless, Si-based LDMOS FETs, which take their name from the acronym of laterally-diffused metal-oxide-semiconductor technology, are used extensively nowadays in power amplifiers of transmitters of base stations, due to their excellent ratio of price and performance [19]. The production cost per unit of LDMOS FETs is low because the comparatively cheaper fabrication technology of silicon transistors is used, which has been developed and matured over the last decades. Presently, LDMOS FETs are the prime commercial technology for power amplifiers of base stations, fabricated by major companies like Freescale[®], Motorola[®], Philips[®] or Ericsson[®].

Yet, GaN HEMTs are being considered to replace LDMOS, due to its advantages, like higher cut-off frequency and higher current density [20]. The related higher efficiency, higher operation frequency and smaller size with respect to LDMOS FETs reduce operation costs. This reduction is beginning to balance the price advantage of Si-based technology, as evidenced by the next example given in [20]: GaN HEMTs for power amplifiers of transmitters used in WiMax^{®1} technology are being commercialized by CREE[®], such GaN-based solution successfully satisfies specifications of linearity and frequency range with efficiencies of up to 28%, using a single GaN HEMT, instead of the three LDMOS FETs used in typical Si-based solutions whose efficiency is only 18%.

The output power performance of LDMOS FETs is basically supported by its high breakdown voltage, whose value can be adjusted through physical changes of the device structure [21]. However, the adjustment is limited and a maximum value to be achievable is estimated around 200V, which contrasts with the breakdown voltages already reported for GaN devices, as large as 450V [15].

Output power densities between 2.5 and 5 W/mm, common with GaN HEMTs for UMTS, are 2 to 4 times the record values of LDMOS FETs [22] (3 to 6 times those of GaAs devices [23]). Power densities up to 32

¹ WiMax[®] is a communications protocol that provides fixed and mobile Internet access.

² CMOS (Complementary Metal-Oxide-Semiconductor) FETs are a Si-based device type invented in the

W/mm have been reported for GaN HEMTs of UMTS [20], and excellent values on higher frequencies, even beyond 30 GHz, as shown in Figure 2.1.

The main drawback of LDMOS FETs is that their performance for power amplification degrades rapidly above 3 GHz [20]. Notably, the future success of GaN HEMTs is linked to the success of amplification schemes with switching-mode power amplifiers, because the frequency limitations of LDMOS FETs make them unsuitable to design such highly-efficient fast-switching power amplifiers [20].

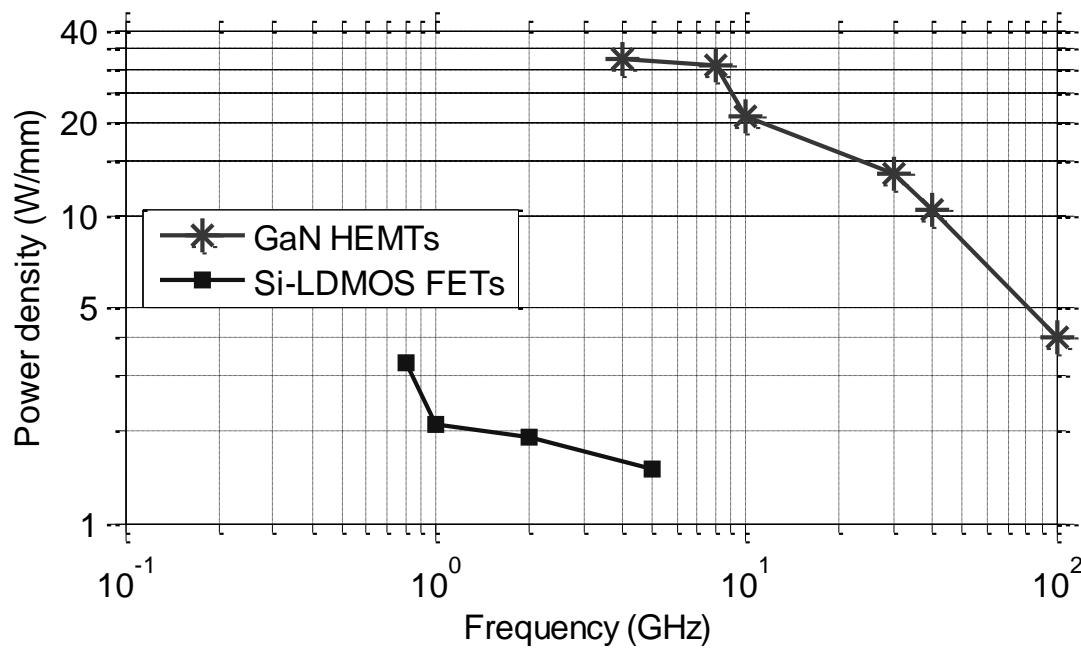


Figure 2.1 Illustration of record power densities versus operation frequency based on diverse published results of GaN HEMTs [24-28] and Si LDMOS FETs [22, 29, 30].

The high thermal conductivity obtained using SiC substrates in GaN HEMTs, compared with the value of bulk Si, reduces temperature changes of the channel and makes the drain current and power less dependent on temperature than in LDMOS FETs. The superior bandwidth and temperature stability of power amplifiers built with GaN HEMTs compared with the same circuits built with LDMOS FETs have been demonstrated, like in the results of [31]. In [31], power amplifiers built with GaN HEMTs are shown to be more efficient with comparable power gain and linearity than a similar circuit version built with LDMOS FETs.

The ability to fabricate a whole system in one chip (e.g. from the digital to the high power parts of a base station) is an attractive trait of LDMOS

FETs; they are easily integrated with multipurpose CMOS FETs², since both are built with Si [21]. But, the feasibility to fabricate GaN devices on Si substrates has inspired research on the Si and GaN integration, like the results of [32] that present the fabrication of a GaN HEMT aside a Si MOSFET on a same Si substrate. Such results promise to balance GaN HEMTs and LDMOS FETs regarding system integration [32].

2.2 Physical Structure and Operation of AlGaN/GaN HEMTs

On basic terms, FETs consist of stacked semiconductor layers with the device terminals on the top. The thickness, arrangement and materials of the layers are specific for each kind of transistor. The HEMT layer structure basically consists of a wide-bandgap semiconductor grown on top of another material with a narrower bandgap. This is known as a heterojunction. Mimura of Fujitsu[®] invented the HEMT concept in 1980 for GaAs devices [14].

The typical FET operation is based on the control of the current of the conduction channel applying a potential in the gate and an electric field along the channel space. A particularity of HEMTs is that the channel thickness is negligible, and thus the channel is considered bidimensional instead of a volumetric part of the material, as in MESFETs. Due to this, the channel is known as a two-dimensional electron gas or 2DEG. Another characteristic of HEMTs is that the gate controls the current by changing the electron concentration of the 2DEG, known as sheet carrier density, and not by varying the transversal area of the channel as in MESFETs [10].

2.2.1 Basic Layer Structure and Band Diagram

GaN HEMTs heterojunction was originally formed with n-type doped³ AlGaN as barrier layer and GaN as channel layer. This basic layer structure is shown in Figure 2.2, with the related energy band diagrams, before and

² CMOS (Complementary Metal-Oxide-Semiconductor) FETs are a Si-based device type invented in the 1960s, which is used in a variety of electronics: digital circuits like microprocessors, microcontrollers and memory, and analog circuits like sensors, data converters and transceivers of low-frequency communications.

³ Doping is the process of adding atoms from a different element to a semiconductor. The added atoms are called *impurities* and the source elements *dopants*. These added atoms donate electrons or accept them, and then are called *donors* or *acceptors* and the source elements n-type or p-type *dopants*.

after forming the heterojunction. Semiconductor-to-metal contacts are placed on the top, ohmic contacts for drain and source and a Schottky contact for the gate. A semi-insulating substrate lies at the bottom.

In the basic GaN HEMT structure shown in Figure 2.2 (a), when the heterojunction is formed, the excess electrons of the n-type doped AlGaN barrier layer will move to the GaN channel layer trying to minimize their energy, as indicated in Figure 2.2 (c), until the balance of the Fermi level between the two materials takes place and equilibrium state is established. Heterojunction structures benefit from the improved electron mobility appearing in the quasi-triangular quantum well formed at the boundary of the heterojunction, shown in Figure 2.2 (c).

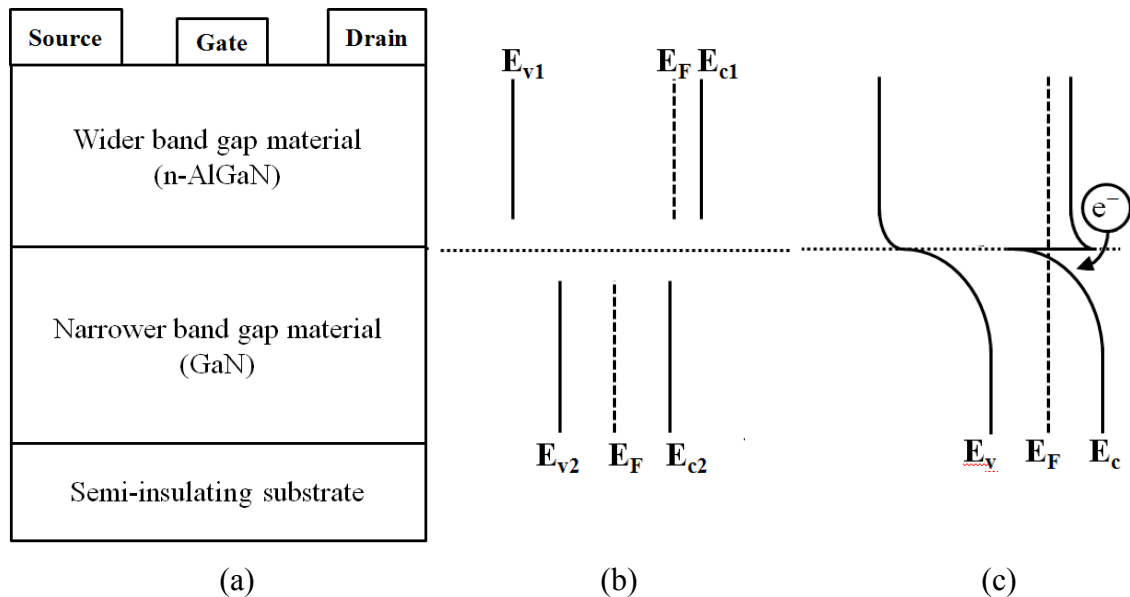


Figure 2.2 (a) Basic AlGaN/GaN HEMT layer structure, (b) band diagram of the heterojunction before the equilibrium condition and (c) afterwards.

2.2.2 Formation of the 2DEG

In HEMTs, the 2DEG forms in the quantum well at the interface of the heterojunction, in the channel layer side. Initially, the electron concentration depends on the doping density of the barrier layer. In MESFETs, the doping density decreases electron mobility by impurity scattering, but since the 2DEG of HEMTs does not flow in the n-type doped layer, the electron mobility in HEMTs does not decrease when the doping density increases [14].

In AlGaN/GaN HEMTs, the electron density of the 2DEG is not entirely due to the doping profile of the n-type doped layer and it can be

formed even in the case of a barrier layer without intentional doping (undoped). The case of undoped barrier layer the 2DEG is due to the charge carriers appearing at the interface of the heterojunction caused by an inherent electric field [33]. This electric field has two components, one is related to a phenomenon called spontaneous polarization and the other to a phenomenon called piezoelectric polarization.

According to [33], the polar nature of GaN and AlGaN crystals, related to the high electronegativity of nitrogen, produces a negative sheet charge at one face of the crystal, and a positive sheet charge at the opposite face. The presence of the polarization charges originates a built-in polarization field along the layer thickness, known as spontaneous polarization, as shown in Figure 2.3(a).

The different lattice constants of the AlGaN and GaN crystals cause tensile stress on the AlGaN layer near the interface of the heterojunction. To illustrate this, a suitable analogy is given in [34]: One can think about the crystal lattices as two combs, each of which has different teeth spacing. When the combs are joined, their teeth tilt trying to fit the spacing of each other, which introduces tensile stress. In the example the combs represent AlGaN and GaN layers and the teeth atoms and bonds of the crystalline lattices. The channel layer has no noticeable stress because the device below the barrier layer is much thicker in comparison. The tensile stress from growing lattice-mismatched AlGaN on GaN induces a static charge and a built-in polarization field in the barrier layer due to piezoelectric properties of nitrides [33]. This piezoelectric polarization has the same direction than the spontaneous polarization, as shown in Figure 2.3(b).

The spontaneous and piezoelectric polarization fields induce a net positive charge at the AlGaN/GaN interface and a net negative charge at the top of the barrier layer forming what is known as the polarization dipole [33], as shown in Figure 2.3(c). Such net charges are not actually free charge carriers, but induced charges as in typically polarized dielectrics. The polarization dipole and the electric field induced in the barrier layer, allow the 2DEG formation even with undoped AlGaN, because electrons are prone to compensate the net positive charge at the interface (implying that the energy levels of the conduction band are below the Fermi level). Figure 2.2(c) shows the resulting quantum well.

Another distinctive aspect of the operation principle of GaN HEMTs is the origin of the electrons that form the 2DEG. The most proved and

accepted theory, explained in [35], is that the source are surface donor states from near the top of the barrier layer. This theory states that to generate the final charge distribution the polarization dipole is complemented by an opposing dipole. The opposed dipole, as shown in Figure 2.3(d), contains the 2DEG at the heterojunction interface and a hole-gas at the top of the barrier layer, which is a thin channel of hole-type positive-charge particles.

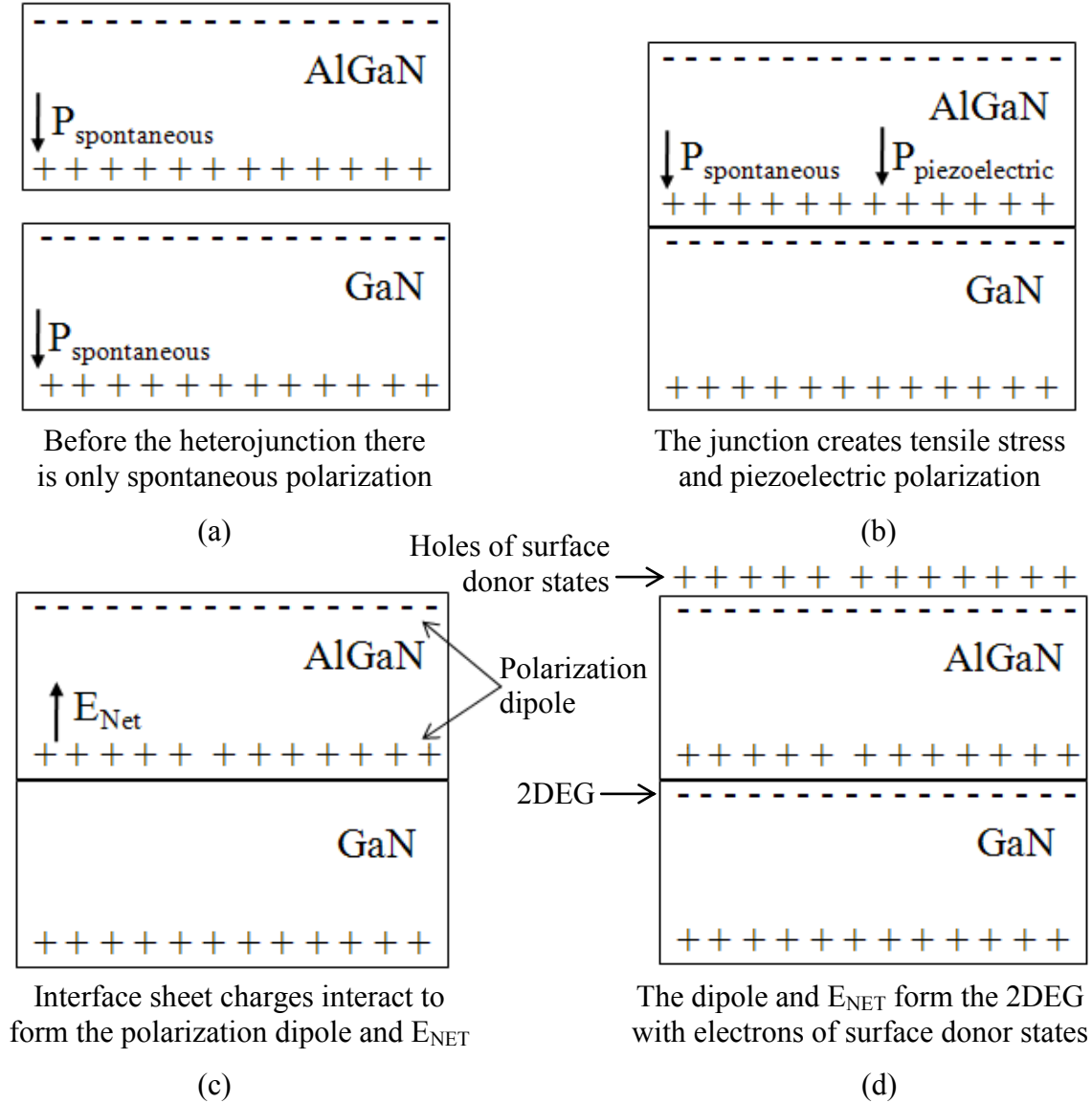


Figure 2.3 Illustration of 2DEG formation on GaN HEMTs redrawn from [35]: In (a) the heterojunction does not exist yet, in (b) the heterojunction is created and tensile stress occurs, in (c) the polarization dipole appears, and in (d) the 2DEG is formed.

2.2.3 Functional Description of Advanced Layer Structures

GaN HEMTs performance can be improved adding layers to the basic structure or modifying material compositions or thicknesses. This leads to more sophisticated structures, like that shown in Figure 2.4 that was composed from the published data of references [17, 19, 26, 33, 35-38]. Although other variations are possible, this structure is a fairly general representation of what is presently found in advanced AlGaN/GaN HEMTs. The following paragraphs of this section discuss the typical composition of the layers, as well as their function and influence on device performance.

SiC, Si, sapphire, diamond or aluminum nitride (AlN) are used as substrate layer, but GaN itself as substrate is uncommon. The use of non-native substrates means a crystalline lattice mismatch between the substrate and the GaN layers above, which, as explained in a later section, tends to produce unwanted charge-trapping, degrading the device performance.

The function of the nucleation layer is to ease the heteroepitaxy process of the GaN layers (buffer/channel) above the substrate and to suppress undesired current leakage due to extension of the applied electric fields into the substrate [38]. Heteroepitaxy is the growth of material layers on substrates of a different material. The nucleation layer is frequently AlN, but GaN and AlGaN can also be employed, if grown in lower temperatures than the upper layers [33].

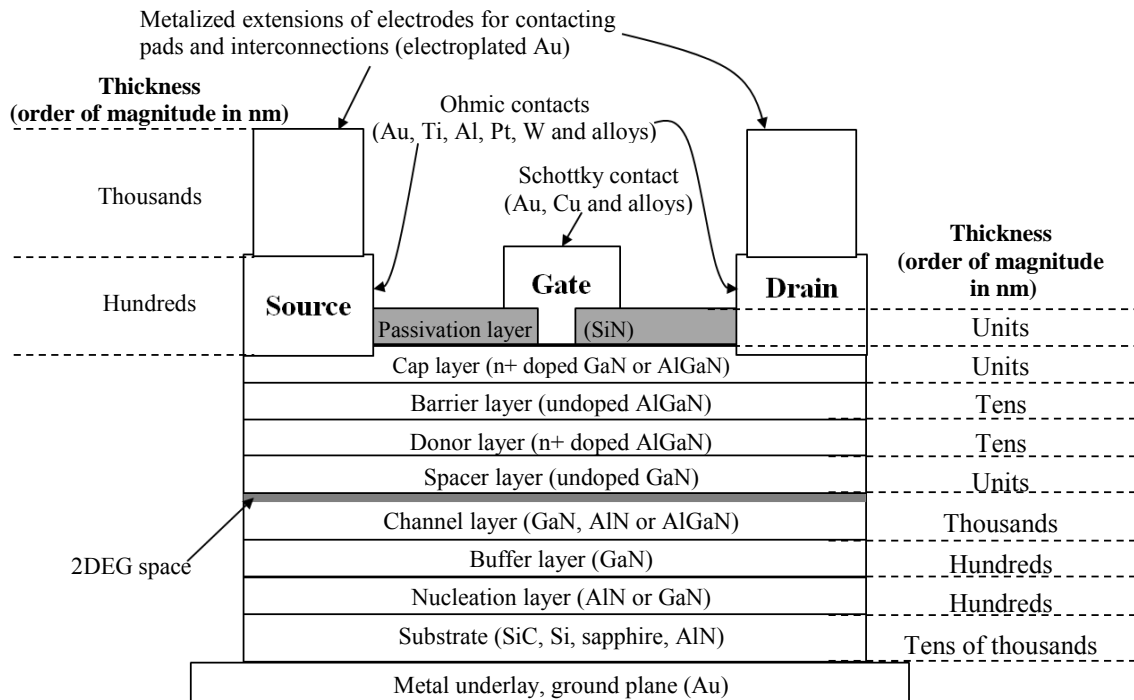


Figure 2.4 Layer structure with detail of different layers that are commonly found in advanced AlGaIn/GaN HEMTs to improve performance [17, 19, 26, 33, 35-38].

The main function of the buffer layer is to reduce the density of dislocations due to mismatch between crystalline lattices of the substrate and the GaN layers above [39]. If the nucleation layer is GaN or AlGaIn, it is not distinguished from the buffer layer.

As explained before, the channel layer is where the 2DEG forms and is usually undoped GaN. If the nucleation layer is AlN and the buffer layer GaN, then the buffer and channel layers are not strictly distinguished and only one layer is specified. The electron density of the 2DEG is increased by n-type doping this layer, but it decreases electron mobility [19].

The function of the spacer layer is to separate the 2DEG from ionized donors generated by the donor layer. The spacer is usually a thin layer of undoped AlGaIn. A drawback of the spacer is a reduced concentration of electrons in the 2DEG directly proportional to the spacer thickness [35].

The function of the donor layer is to increase the electron density in the 2DEG, by supplying electrons of its own, and is therefore made of electron-rich n-type doped AlGaIn.

The function of the barrier layer is to reduce the leakage to the gate metal of the donor layer electrons destined to the 2DEG. It is usually a thin layer of undoped AlGaIn. If the donor layer is undoped (i.e. not used), then the barrier, donor and spacer layers are made of the same material (undoped AlGaIn) and only the barrier layer needs to be specified [40].

The function of the cap layer, made of n-type doped GaN, is to reduce drain and source resistances due to the access regions between the electrodes and the channel [37].

All the layers discussed up to this point are often known as the epi-structure or the mesa of the device, and the contacts for the electrodes are placed above it. Ohmic contacts are used for the drain and source electrodes and a Schottky contact is used for the gate electrode.

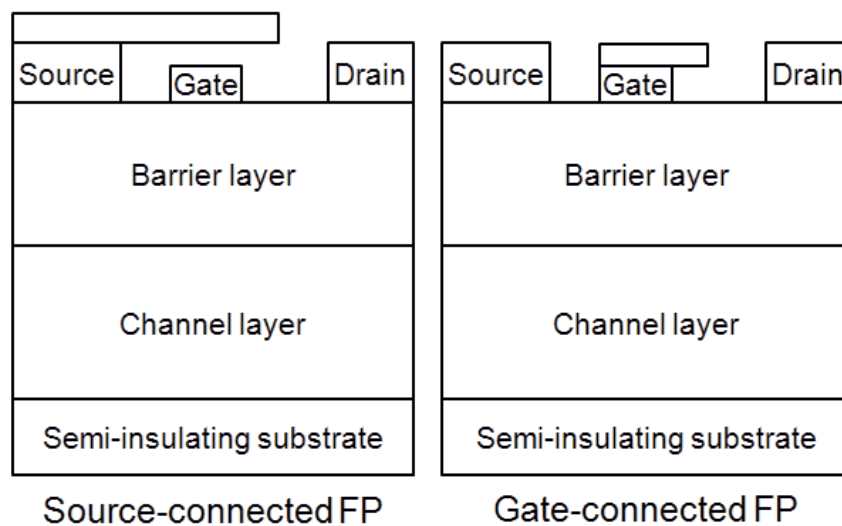
The ohmic contacts have the function of producing a stable low-resistive connection between the electrode metal and the semiconductor below. These contacts usually consists of thin layers of different metals stacked, like Ti, Al, Au, Mo, Pt or W [33].

The Schottky contact of the gate is produced with Au or Cu and alloys of other metals and is placed directly over the mesa. T-shaped electrodes reduce the gate footprint, which means a lower effective gate length. Small gate footprints are preferred because the upper frequency limitation of the device operation is inversely proportional to the effective gate length [17].

The function of the passivation layer, usually made of SiN, is to reduce charge trapping attributed to the interface between the layer structure and surface above [26].

Above the ohmic contacts, the device electrodes are extended with a metal layer of electroplated Au, to serve as contacting surface for the connection to other circuit elements or measurement equipment.

Several investigations discuss improved device performance using features known as field-plate technology, to improve the maximum output power by increasing the breakdown voltage. The application of higher drain voltages is possible due to the reduction of the electric field at the edge of the gate electrode on the drain side [41]. The field plate is a metallic electrode extension placed over the gate and the gate-drain region [41]. Different variants of field plates are possible, but those mostly used are shown in Figure 2.5, redrawn from [42].



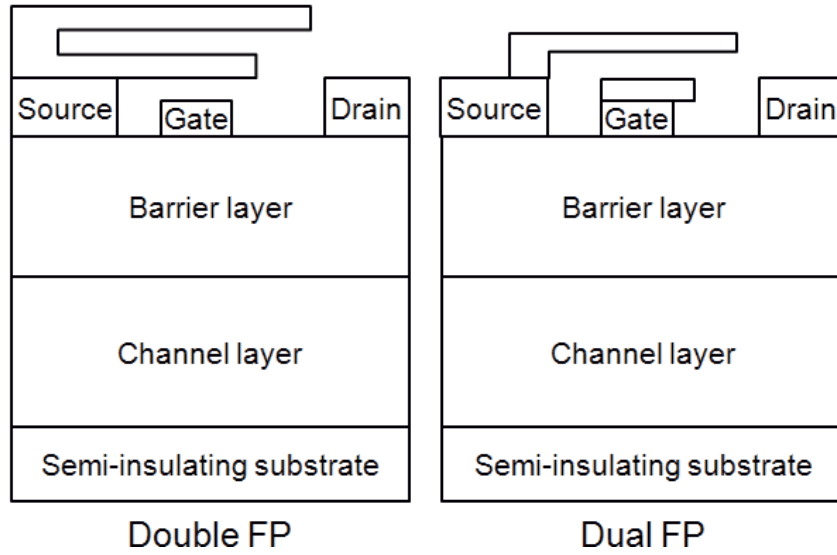


Figure 2.5 Different variants of field plates of modern GaN HEMTs, redrawn from [42].

2.3 Drawbacks of GaN HEMTs and Modeling Challenges

2.3.1 Charge-Trapping Induced Dispersion

Dispersive phenomena on GaN HEMTs limit the performance of the power amplifiers, decreasing the dynamic range, linearity behavior and efficiency [43]. Charge-trapping effects show themselves in electrical delays of the amplifier response, generating undesired memory effects, where the present state and output becomes dependent on previous inputs. Different effects observed experimentally on the performance of GaN devices have been related to dispersive behavior and attributed to charge-trapping phenomena [43, 44].

GaN HEMTs present characteristic challenges to accurately model dispersion induced by charge trapping and self-heating effects. For measurement-based models, like those developed in this thesis work, additional and more advanced measurements are needed with respect to standard models usually developed for Si or GaAs devices.

2.3.1.1 Definition of Dispersion and Attributed Effects

Dispersion can be generally defined as the unwanted variation of a given parameter of the device response with respect to the frequency of the RF signals that are handled. In FETs, dispersion usually refers to the dispersive behavior of the output signals, either of current or power.

Dispersion-inducing phenomena of GaN HEMTs has been detected by the appearance of effects that degrade performance, like the effects called power or current slump, current dispersion and current collapse [43, 44].

Current collapse is a decrease observed in the continuous-wave output current after applying a high bias voltage at the output with respect to the current observed when the previous state was repose (no bias voltage) [44], as illustrated in Figure 2.6. This effect results of the charge trapping in regions of the device layer structure outside the conduction channel [45].

Current dispersion refers to the difference of the drain current measured in static-DC and RF modes. This difference is dependent on the frequency of the RF signal and on the bias condition [46]. This effect can also be noticed by the difference between static-DC and pulsed-DC IV characteristics, then, it depends on the pulse repletion and duty cycle, and on the *quiescent* bias condition [43]. Frequency dispersion of the drain current in MESFETs has been explained by the finite times that the electrons require to form and deplete the channel (characteristic speed of the transistor), which lags the current response for rapidly-varying inputs with respect to non-variant or slowly-varying inputs [43]. In strongly dispersive devices, like GaN HEMTs, the observed current dispersion cannot be explained only by that response lag, but is mainly attributed to charge trapping and leakage currents in the layer structure [45].

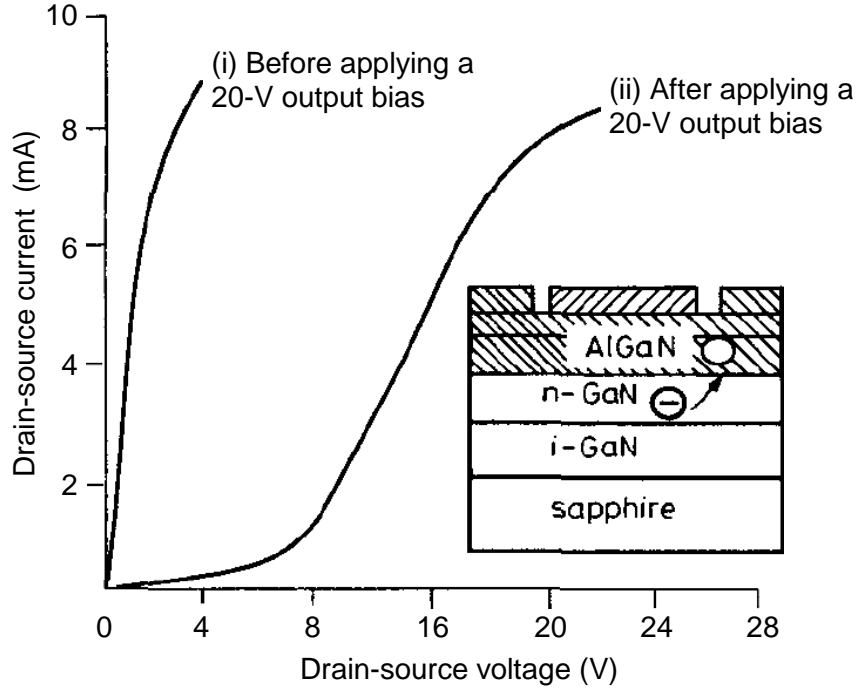


Figure 2.6 Illustration of the current-collapse effect induced by charge trapping. Inset: Suggested location of the traps in the layer structure [44].

The term power slump is used to designate the observation that lower RF power is available than that expected from DC operation, which is due to effects known as current slump and knee walkout [46]. Current slump is a form of current dispersion, e.g. for a specific operation frequency and bias point [43].

The current lags induced by trapping effects have been experimentally related to the variation of the applied gate or the drain voltages; they are consequently known as gate lag or drain lag, respectively.

As explained in [47], traps interfere with device operation by offering to the 2DEG electrons intermediate energy states inside the bandgap between the valence and the conduction band. Those energy states are distinguished between shallow-level and deep-level states, depending on the amount of energy that a trapped electron needs to gain in order to be released. The trapped electron can be released either into the valence or the conduction band. The trapped electrons imply a decrease of electron concentration in the 2DEG, as shown in the inset of Figure 2.6, which results in degradation or *collapse* of the drain current.

The term *trap* or *trapping center* is generally used in the literature of the field to designate the case of capture and emission of an electron from and to the conduction band. If the nature of the trap is such that it captures an

electron of the conduction band and later emits it to the valence band, then often it is simply called recombination center. From another perspective, a recombination center captures a hole after an electron, which actually means that the captured electron is incorporated to the valence band [47].

In principle, traps can be located at the surface, at interfaces between layers or in the bulk of the semiconductor layers [45]. Surface trapping effects refer to electrons of the gate metal moving to states of the nearby surface layer. Bulk traps are thought to be caused by native defects in the crystalline lattice of the semiconductor that are also called point defects, and by impurities. The impurities can be due to unintentional or intentional doping of the material [48]. Traps at the interfaces between layers of different materials are considered to be caused by dislocations of the crystalline structure that appear due to mismatch of crystalline lattices and mechanical or thermal stress of the crystal growth.

2.3.1.2 Trapping due to the Novelty of GaN Technology

The novelty of wide-bandgap semiconductor devices is a drawback due to the technological immaturity of the fabrication process [49]. Undesired variations of the parameters of this process produce or accentuate charge-trapping effects and undesired limitations of performance.

GaN devices built on SiC lack the decades of maturity of the processing technology of Si. The combined novelty of fabrication technologies of GaN and SiC makes GaN devices built on SiC substrates more prone to show dispersion induced by charge-trapping, due to variations of parameters of the fabrication process, like quality of interfaces between layers, doping profile or density of unintentional impurities.

2.3.1.3 Trapping due to the Nonnative Substrate

Ideally, the substrate layer of the transistors and the layers above are of same material to avoid crystalline lattice mismatch, which is known to bring out charge trapping effects and strongly degrade the device performance [10]. However, native GaN substrates are not used because the GaN ingots that are sliced to get substrate wafers are not found in

nature with sufficient crystalline purity, and the technology to manufacture cost effective, synthetic ingots is in early stages of research .

GaN layers can be grown on other substrates, like diamond, sapphire, SiC and Si. Most research focus on the fabrication of GaN devices over SiC and Si, whereas sapphire and diamond are disfavored due to their high costs [13]. Table 2.2 lists key characteristics of substrate materials.

Table 2.2 Key features of nonnative substrate materials for GaN HEMTs, from [7, 46].

Substrate material	Lattice mismatch to GaN (%)	Thermal conductivity ($\text{W m}^{-1} \text{ }^{\circ}\text{K}^{-1}$)	Largest wafer size available (inches/ ^{company})	Normalized cost (relative to Si-wafers)	Normalized cost per inch of wafer size
SiC	3	≈ 400	4/Cree®	100	25.000
Sapphire	13	≈ 50	8/Rubicon®	10	1.250
Si	17	≈ 150	6/Nitronex®	1	0.166

The lattice constant of SiC provides the best match to GaN and that material is a better heat conductor than Si or sapphire, but presently it is also the most costly substrate per wafer size.

2.3.2 Parasitic Effects of GaN Devices

Nowadays it is desired to fabricate GaN devices with greater output power capabilities to counteract the comparative drawback of cost with respect to Si LDMOS FETs. In FETs, the power handling capabilities are generally increased by enlarging the total horizontal area of the gate electrodes. Preferably, the electrode width is enlarged, because increasing the electrode length has the drawback of reducing the device bandwidth. Another way to increase the total horizontal area is obviously to increase the number of gate electrodes, which is equivalent to connecting additional transistor cells in parallel. The product of unit width per number of gate electrodes is known as gate periphery, and devices with increasingly large gate peripheries present comparatively more parasitic effects.

Field-plate technology, which is commonly used in modern GaN HEMTs to improve performance, significantly changes parasitic effects due to the modification of capacitive phenomena by the field-plate metal, which complicates the overall modeling of these parasitic effects.

Capacitive effects between the device electrodes are well-known parasitics and the related capacitance values depend on the separations between the respective metal surfaces, for instance, gate-to-drain, gate-to-

source and drain-to-source [50]. In devices with field plates the effective separations between electrodes change, notably modifying the parasitic capacitive effects with respect to the devices without field plates. Capacitive effects between the device electrodes that are normally neglected can become significant due to the field-plate metal.

In consequence, more comprehensive equivalent circuits are needed to model the more complex parasitic effects of modern GaN HEMTs with respect to the standard circuits commonly used for Si and GaAs FETs. New algorithms are also needed to obtain the parameter values of the equivalent circuits with the same measurements employed to model parasitic effects of Si and GaAs FETs, and eventually, different or additional measurements need to be used.

2.3.3 Self-Heating Effects on GaN Devices

Due to the large power densities that are typically achieved with GaN devices and the high temperatures of operation that are possible, memory effects due to self-heating phenomena are accentuated, especially for GaN devices built on Si and sapphire substrates with lower thermal conductivities than SiC or diamond.

The finite times that the semiconductor layers of the device need to transfer the heat created by the current flow to the environment and the substrate result in significant temperature changes in the conduction channel that modify the output current and power ratings. These effects are known as self-heating and are another cause of current dispersion.

Self-heating effects cause that the present state and output signals of the device and of the power amplifier become dependent on previous states or input signals. This undesired behavior is known as thermal memory [45].

Accurate modeling of the self-heating effects in GaN HEMTs usually employs electro-thermal model formulations, which are a distinctive feature of modeling wide-bandgap devices with respect to devices built with other materials.

Chapter 3

Device Characterization for Modeling

The models developed in this thesis work are measurement-based, so a phase of device characterization must be carried out initially to acquire the database for modeling.

Subchapter 3.2 describes the electrical measurements, measurement techniques and results of the device characterization performed to acquire the database for modeling.

Once the model parameter values are known, the models are ready to be implemented in CAD-software and this makes possible the model verification phase. In the model verification phase, simulations of device response are performed and compared with actual measurements.

Subchapter 3.3 discusses the device characterization carried out for model verification.

The devices characterized and modeled in this thesis work were unpackaged on-wafer chips (dies), and thus, the measurement setups used an on-wafer probing station (Cascade Microtech[®], model 42) to connect the devices to the stimuli generators and measurement equipment. In the on-wafer probing station, probe tips for up to 40 GHz were used (Microprobes by Cascade Microtech[®] models ACP40-GSG-150, 250 and 350).

The static-DC bias voltages were supplied with two DC voltage sources that also acted as current sensors (HP[®], models 6633A and 6655A).

The measurement setups were computer-controlled through the GPIB protocol and with scripts written in Matlab[®] (except for pulsed-DC IV measurements).

3.1 Manufacturers and Technology of the Studied Devices

The following devices were characterized and modeled in this work:

- a) AlGaN/GaN HEMTs manufactured by Nitronex[®] Corporation.

- This device type has a gate periphery of 2 mm, with a unit gate width of 0.2 mm (10 gate fingers).
- The layer structure of this device type is shown in the schematic of Figure 3.1. As depicted in that schematic, Nitronex[®] employs a GaN-over-Si fabrication process (the AlGaIn/GaN HEMT is build over a Si substrate).

GaN Cap	Cap Layer (15 Å)
AlGaIn Barrier	Barrier of Composition - x (26% Al) and Thickness - d (180 Å)
GaN Channel & Buffer	2DEG $n_s = 8.5 \times 10^{12} / \text{cm}^2 \pm 2.9\%$ $\mu_n = 1,500 \text{ cm}^2 / \text{V-s} \pm 2.5\%$ Semi-insulating GaN Buffer Layer (0.8 μm)
Transition layer	Stress Mitigating Transition Layer
Silicon	High Resistivity Silicon Substrate (10,000 $\Omega\text{-cm}$)

• >600 NRF1 Baseline Wafers processed since October 2005

Figure 3.1 Layer structure schematic of the studied Nitronex[®] device, taken from [51].

- This device type had source-connected field plates, as highlighted in the images shown in Figure 3.2 (abbreviated as S-c FP).
- b) AlGaIn/GaN HEMTs fabricated by the Fraunhofer Institute for Applied Solid-State Physics (IAF) of Freiburg im Breisgau, Germany.
- Devices of this type were available in four different sizes: gate peripheries of 0.5, 0.8, 2 and 3.2 mm, with unit gate widths of 0.25, 0.4, 0.25 and 0.4 mm (2, 2, 8 and 8 gate fingers), respectively.
 - IAF fabricated these devices over SiC substrates. Further details of the considered device layer structure are found in [52].
 - The IAF devices studied in this thesis work did not present source-connected field plates.

Modeling of the 0.5-mm, 0.8-mm and 2-mm IAF devices (smallest gate peripheries) will be discussed mainly in subchapter 5.3 dealing with model scalability, since this thesis focuses on large-size device modeling.

In consequence, the device measurement results that are reported in the present chapter, to exemplify device characterization results or aspects of

measurement techniques, correspond exclusively to the 2-mm Nitronex[®] device and the 3.2-mm IAF device.

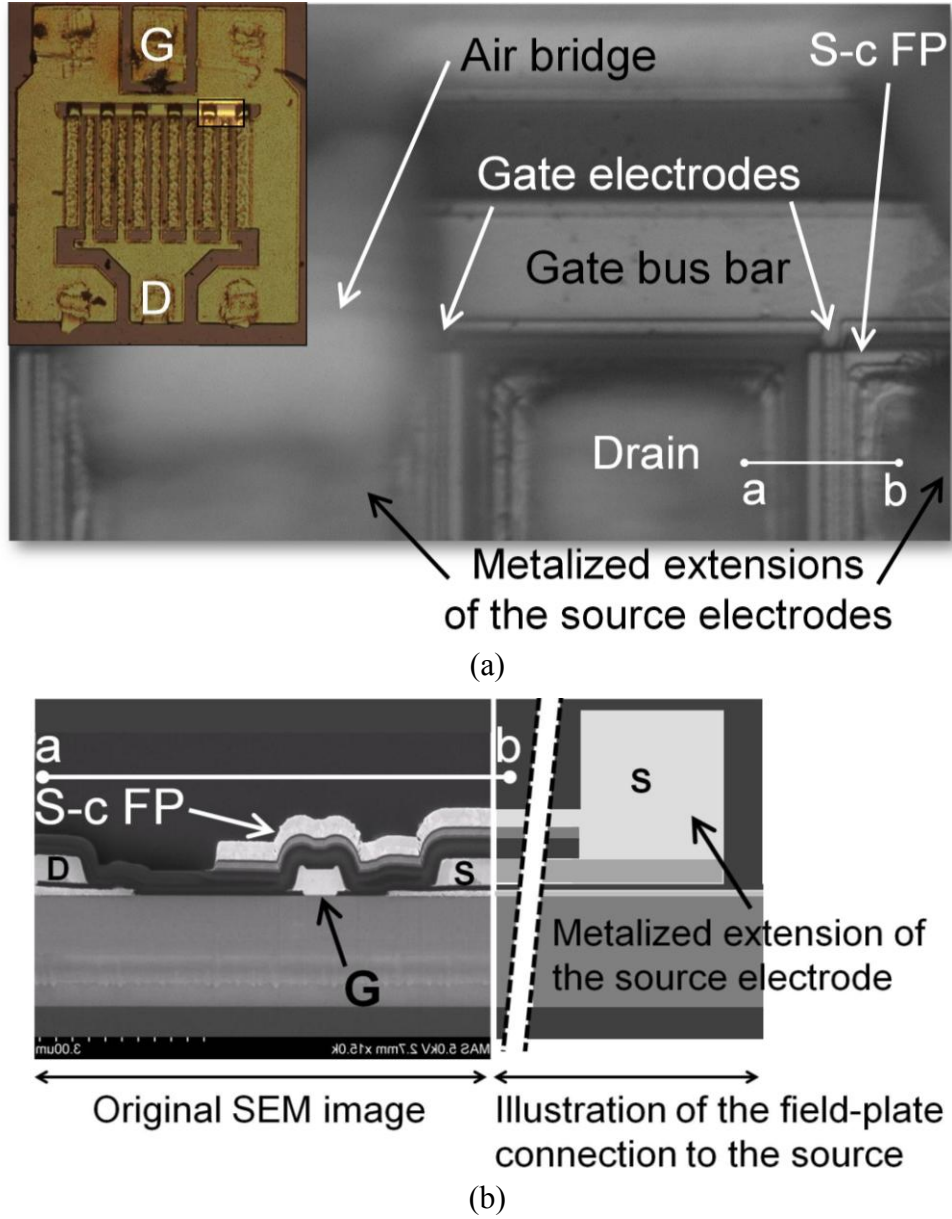


Figure 3.2 Images of the studied 2-mm device highlighting the source-connected field plates along the segment a-b: (a) Top-view micrograph made for this work with an inset to point out the location of the image in the finger layout. (b) Side-view SEM image taken from [51] with an added diagram to show the field-plate connection to the source.

3.2 Data Acquisition for Modeling

In this thesis, the modeling strategy is presented split in two stages: (i) small- and (ii) large-signal modeling.

Calculation of the extrinsic parameters of the small-signal model is based on S-parameter measurements of a specific type (*cold* S-parameters,

i.e. with $V_{DS} = 0V$). However, performing static-DC IV characterization as initial step provides advantageous and indispensable information for further characterization phases, regarding device bias conditions.

The small-signal model is completed with the calculation of its intrinsic parameters, using S-parameters measured on additional bias points besides *cold* bias conditions: S-parameters characterization on active bias points.

Calculation of the large-signal model also requires results of pulsed-DC IV characterization.

Static-DC IV, S-parameter and pulsed-DC IV characterizations will be addressed respectively in the following sections 3.2.1, 3.2.2 and 3.2.3. Each of these sections provides a description of the measurement mode, aspects related to measurement techniques and the most relevant characterization results.

3.2.1 Static-DC IV Measurements

Static-DC IV characteristics help to set the voltage values for the bias points of the measurements for whole device characterization.

The static-DC IV transfer characteristic provides the value V_{th} that is an good initial approximation to the V_{GS} value of the measurement called *cold pinch-off* S-parameters ($V_{DS} = 0V$, $V_{GS} = V_{pinch-off}$). This measurement plays later an important role as database for small-signal modeling.

Static-DC IV characteristics also serve to define specifically the bias points on which bias-dependent model parameters are of interest.

3.2.1.1 Description

The static-DC IV measurements comprise the output characteristic and the transfer characteristic, and describe the behavior of the DC drain current with respect to the DC-voltage supplies.

These characteristics are obtained sweeping values of the gate and drain bias voltages with two supply sources and measuring the static-DC drain current for each sweep step. In the output characteristic, I_{DS} is plotted versus V_{DS} at fixed discrete V_{GS} values. In the transfer characteristic, I_{DS} is plotted versus V_{GS} .

The different IV regions of a prototypical static-DC output characteristic are shown in Figure 3.3, as well as important voltage and current values that appear in that IV characteristic.

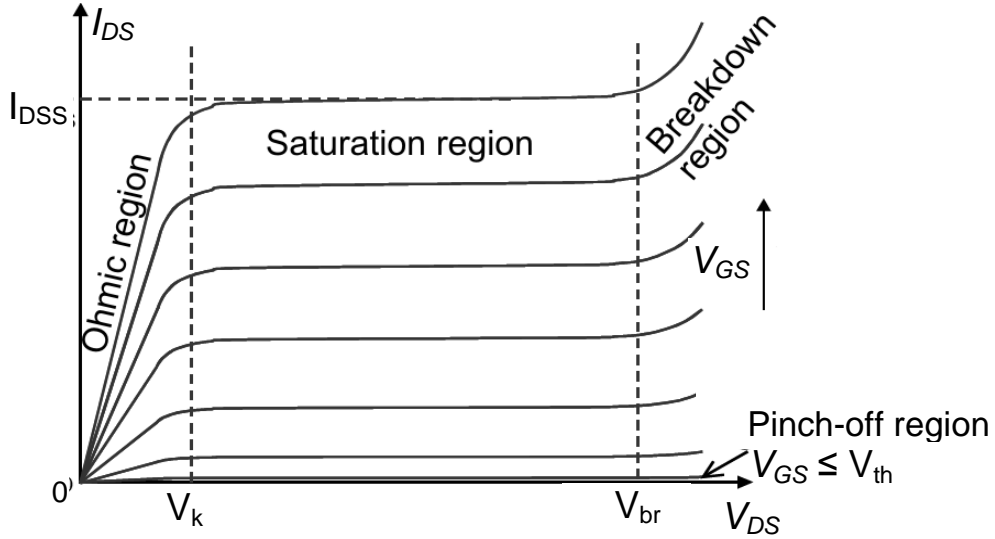


Figure 3.3 Regions and relevant values of an ideal static-DC IV output characteristic.

The V_{DS} value known as the knee voltage V_k generally characterizes the transition between the ohmic and saturation regions.

The I_{DS} value denoted by I_{DSS} corresponds to V_k with $V_{GS} = 0V$ and is commonly used as reference for the maximum output current of the device.

V_{th} is V_{GS} value known as threshold voltage and characterizes the transition into the pinch-off region, that is, into the region where I_{DS} is reduced to its minimum values. A precise definition of V_{th} and its actual values obtained from measured data are presented in subsection 3.2.1.3.

The indicated V_{br} value characterizes the transition to the breakdown region. V_{br} is known as drain-source off-state breakdown voltage when the related V_{GS} value belongs to the pinch-off region ($V_{GS} \leq V_{th}$). When the V_{GS} value corresponds to the saturation region, e.g. open channel conditions ($V_{GS} > V_{th}$), the value that characterizes the transition to the breakdown region is called drain-source on-state breakdown voltage, V_{br-on} .

3.2.1.2 Measurement Techniques and Setup

Experiences in device characterization gathered in this thesis work indicated that the most important aspect of static-DC measurement techniques is observing the device limits in voltage, current and power, during the definition and realization of the bias voltage sweeps.

The static-DC voltage limits were denoted by BV_{GD} and V_{br} . BV_{GD} is the gate-drain breakdown voltage, typically specified by the manufacturers as the voltage limit of FETs. BV_{GD} is related to a semiconductor material property called critical field, E_c , which defines the maximum electric field, thus the maximum voltage, applicable across a two-terminal semiconductor device before avalanche breakdown occurs [5]. If static-DC voltages above BV_{GD} and V_{br} are applied, device failure is likely to occur. V_{br} is the V_{DS} value associated with BV_{GD} when the device is biased in the pinch-off region ($V_{GS} = V_{th}$), i.e. V_{br} is the V_{DS} value of off-state breakdown, as defined for example in [53].

The static-DC power limit is related to the device safe-operation area (SOA). The SOA comprises the area of the I_{DS} - V_{DS} plane where operation without risk of device failure is expected. In this thesis work, the maximum level of static-DC power was denoted by P_{DSmax}^{SOA} .

The I_{DS} value I_{DSS} corresponds to the saturation current in open-channel conditions, $V_{GS} = 0V$, and is commonly used as reference for the static-DC current limit. However, it does not represent a strict limit, but a reference of the highest current values that are safely generated in the device. Static-DC measurements are often performed with positive V_{GS} values up to a few volts, and thus, with I_{DS} values above I_{DSS} . In any case, the actual maximum value of static-DC current is included in the fabricant definition of the SOA and generally complied as long as P_{DSmax}^{SOA} is observed.

The setup of static-DC measurements consists of the on-wafer probing station and the DC voltage sources that also act as current sensors. The sources only supply positive voltages, and thus, manual rearrangement of the connections is needed to produce negative V_{GS} values.

3.2.1.3 Measured Results

Table 3.1 lists static-DC limits that were considered for the studied large-size devices, according to recommendations of the manufacturers.

Table 3.1 Static-DC limits of the studied devices recommended by the manufacturers.

Manufacturer	Maximum DC output power normalized to the total gate periphery P_{DSmax}^{SOA} [W/mm]	I_{DS} in the saturation region with $V_{GS} = 0V$ I_{DSS} [A/mm]	Breakdown voltage BV_{gd} [V]
IAF	< 7.5	< 0.7	>100
Nitronex [®]	< 5	< 0.5	~60

The static-DC IV output and transfer characteristics that were measured for the studied large-size devices are presented in Figure 3.4 and Figure 3.5.

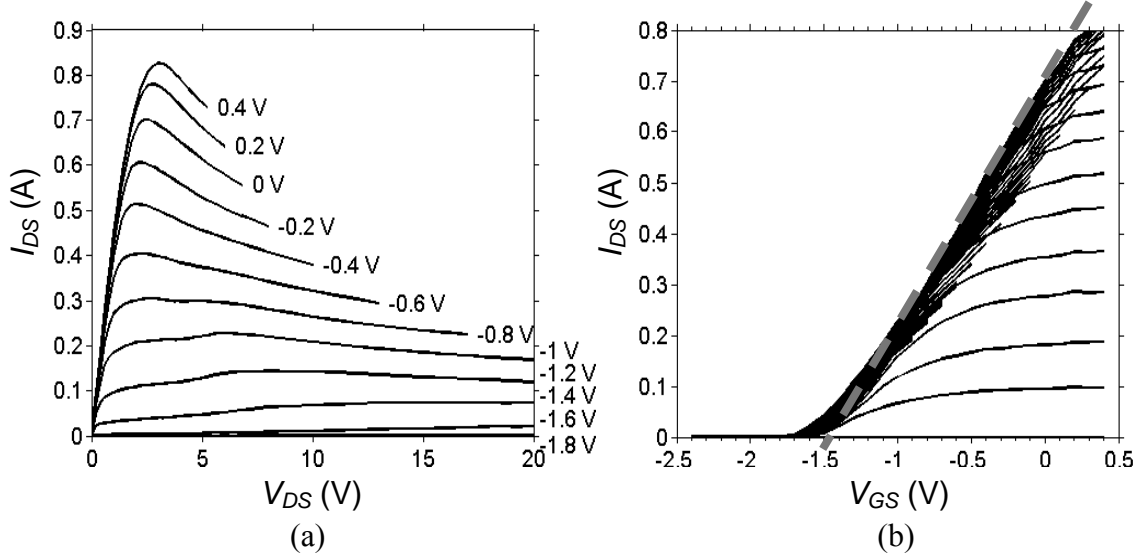


Figure 3.4 Static-DC IV (a) output and (b) transfer characteristics of the 2-mm device. In (b) the graphical estimation of $V_{th} = 1.4V$ is sketched (thick dashed line).

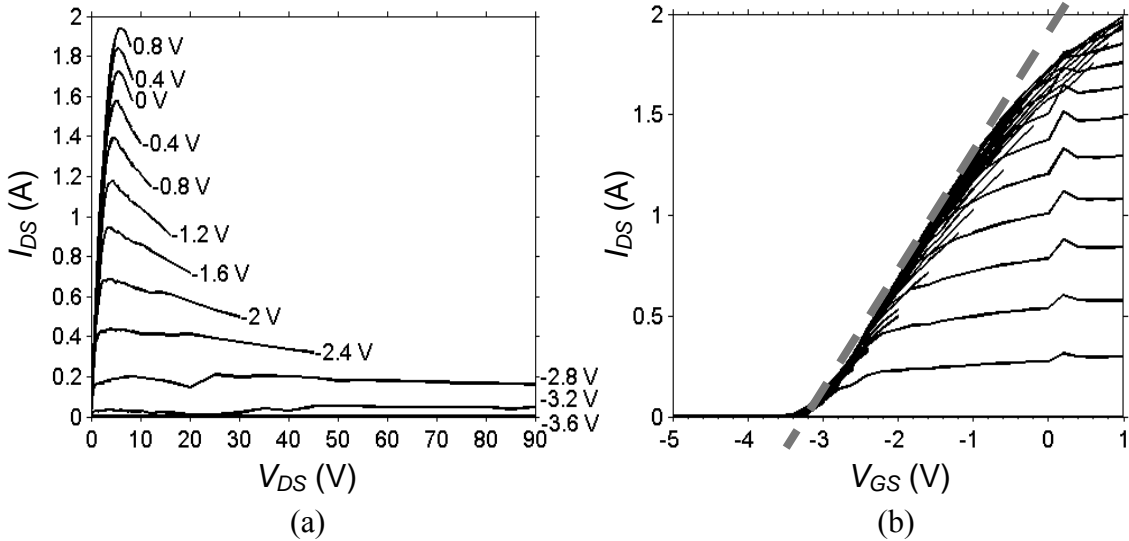


Figure 3.5 Static-DC IV (a) output and (b) transfer characteristics of the 3.2-mm device. In (b) the graphical estimation of $V_{th} = -3.3V$ is sketched (thick dashed line).

Cold pinch-off S-parameters measured on the bias point with $V_{DS} = 0V$ and $V_{GS} = V_{pinch-off}$ are database for a key part of the small-signal modeling that will be presented later. The V_{th} value represents a first approximation to the actual $V_{pinch-off}$ value required for *cold pinch-off* S-parameter measurements.

As explained in subsection 3.2.1.1, V_{th} represents the transition into the pinch-off region. In classical textbook definitions, V_{th} is identified in the

static-DC IV transfer characteristic as the voltage value at which linear extrapolation of I_{DS} intercepts the V_{GS} -axis. The V_{DS} -curve that must be extrapolated corresponds to the one with the largest slope, i.e. the V_{DS} -curve related to the peak transconductance G_m .

The above definition was graphically implemented with the measured static-DC IV transfer characteristics of the studied large-size devices, as sketched in Figure 3.4(b) and Figure 3.5(b). Then, V_{th} values were received as -1.4V for the 2-mm device and -3.3V for the 3.2-mm device.

Besides the measurement in the *cold pinch-off* condition, S-parameters measured on a multitude of bias points distributed among all IV regions (active bias points) are also database for the modeling. Sweeps of V_{DS} and V_{GS} values were selected for the active bias points of such S-parameter measurements, according to the bias-dependency of the current observed in the static-DC IV characteristics. The static-DC limits of devices and of the measurement equipment were also taken into account.

The selected V_{DS} sweeps were dense enough in the low-value range to portray the nonlinearity of the transition from the ohmic to the saturation region, but in the saturation region, this density was gradually decreased, reducing the total number of bias points and overall duration of the measurement sessions.

Table 3.2 summarizes the selected voltage sweeps for the studied large-size devices.

Table 3.2 Selected voltage sweeps for S-parameter measurements on active bias points.

Device	V_{GS} sweep (V)	V_{DS} sweep (V)
3.2-mm device	-5.0 to 1 every 0.2	0 to 8.5 every 0.5, 10 to 16 every 2 and 20 to 60 every 5
2-mm device	-2.4 to 0.4 every 0.1	0 to 3.8 every 0.2, 4 to 8 every 0.4 and 10 to 30 every 2

3.2.2 S-Parameter Measurements

3.2.2.1 Description

S-parameters describe the electrical behavior of linear networks in the same way as Y- or Z-parameters do. However, S-parameters are preferred for high-frequency devices, because they do not require measuring the device response to short-circuit or open terminations, but instead, to specific impedance terminations. These terminations match the system

characteristic impedance and are preferred, because reactive effects at high frequencies difficult the current and voltage measurements related to Y- or Z-parameters and also the fabrication of broadband short-circuit and open terminations [54].

The S-parameters are the elements of the *scattering* matrix of linear electrical networks, where the term *scattering* refers to how traveling waves (of voltage, current or electrical power) are affected, or *scattered*, by inserting the network in a transmission-line system [54]. The scattering of light by a lens is an analogous example often used to explain the S-parameters.

In two-port networks, such as a transistor in common-source configuration, the scattering matrix has two rows and two columns. The S_{11} and S_{22} matrix elements, known as input and output reflection coefficients, are directly related to the input and output impedances of the network. Because of this, S_{11} and S_{22} are usually plotted in a special chart called Smith chart, in which each point has associated a reflection coefficient and an impedance value [54].

The Smith chart is the result of a plane transformation, by which the second quadrant of the rectangular complex plane of impedances is mapped into a circular polar complex plane, as illustrated in the following Figure 3.6. The impedance values mapped in the Smith chart are normalized to the characteristic impedance of the system Z_0 (a standard is 50 Ω), and thus the most external circle of the chart has unity radius [54].

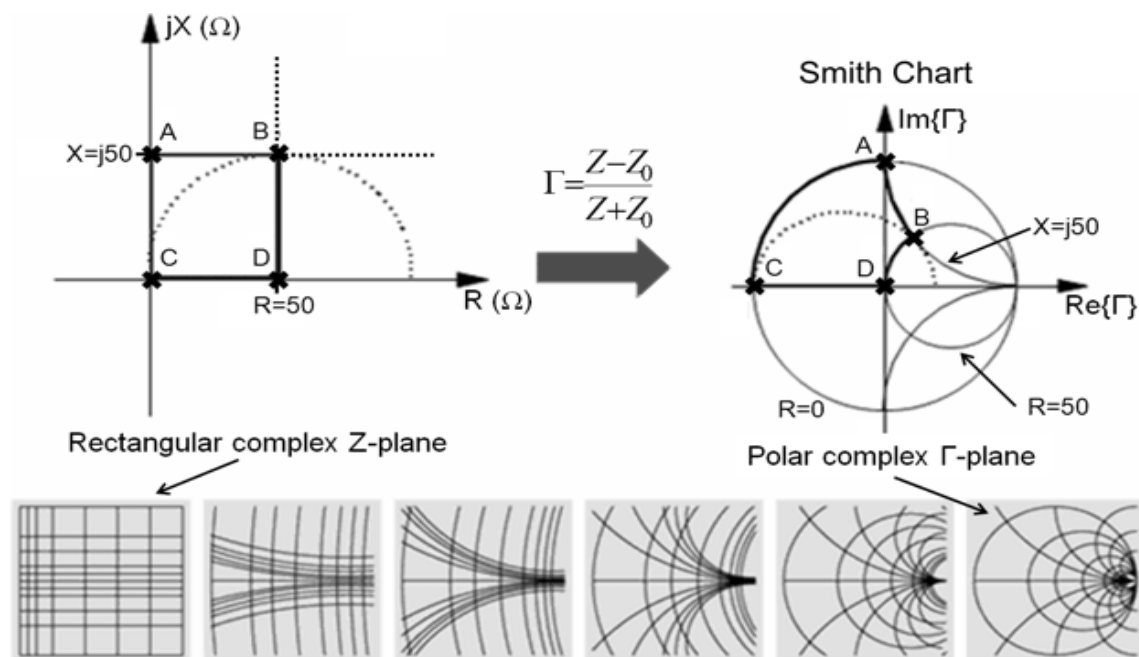


Figure 3.6 Illustration of the Smith Chart and plane transformation, redrawn from [55].

The S-parameters depend on the frequency of the input signal and are called continuous-wave (CW) S-parameters when the bias conditions are static DC. *Pulsed* S-parameters measured on pulsed bias conditions or *large-signal* S-parameters measured with impedance tuners as terminations are not considered in this thesis work as database for modeling.

3.2.2.2 Measurement Techniques and Setup

The S-parameters measurement setup consisted of a vector network analyzer (VNA) connected with coaxial cables (Agilent®) to the on-wafer probing station. Two different VNAs were available for this thesis work (both by Hewlett Packard®/Agilent®), one capable of measurements from 45 MHz up to 40 GHz (model VNA HP8510C), and another that allows measurements from 30 kHz up to 20 GHz (model ENA HP5071C). Bias conditions were set by the same DC-voltage sources as in the static-DC characterization. The bias voltages were supplied with the internal biasing circuits of the VNAs for devices with expected I_{DS} lower than 0.6A. For devices with higher expected I_{DS} , external bias tees were required. The commercial biasing circuits employed are specified for a frequency range of 0.4 to 40 GHz (Model 11612A Opt 001 by Agilent®).

Model parameter extraction must be based on a measured database that is a reliable device characterization not dominated by S-parameter measurements errors [56]. VNA calibration of S-parameter measurements was carried out applying the SOLT technique as in [56], using commercial standards for coaxial and on-wafer calibration (coaxial calibration kit model HP85052A by Agilent® and on-wafer impedance standard substrate ISS model 101119 by Cascade Microtech®). SOLT is an acronym from the names of the employed calibration standards: *Short*, *open*, *load* and *thru*. The SOLT calibration technique is discussed extensively in [57].

Verification of VNA calibration is commonly performed using offset-open (or offset-short) structures [56]. For on-wafer VNA calibration, offset open structures were implemented with open-ended 50-Ω coplanar lines available in the employed impedance standard substrate. Structures to implement off-set short structures are not included in the substrate.

Figure 3.7 shows the reflection coefficient of an offset open measured after on-wafer calibration (VNA model HP8510C) and phase compensation

of the offset length. The observed worst-case amplitude and phase errors, 0.25 and 1°, indicate S-parameter measurement accuracy comparable with that reported in [56], and with the VNA accuracy specified by the manufacturer [58]. Similar verification results were obtained for both VNA ports in each measurement session of S-parameter characterization.

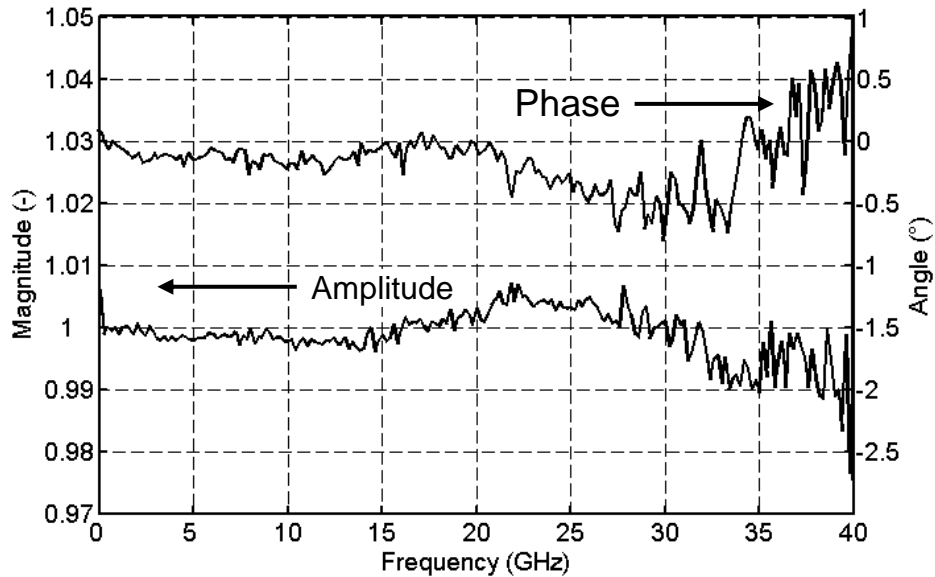


Figure 3.7 Measured reflection coefficient of an off-set open employed for verification of the VNA on-wafer calibration (including phase compensation for the offset length).

Degradation of the VNA calibration over time is known as drift [56]. Figure 3.8 shows the reflection coefficient magnitude of the calibration verification standard measured right after calibration (solid line) and after a 12-hours period (squares). Similar results were obtained for the phase.

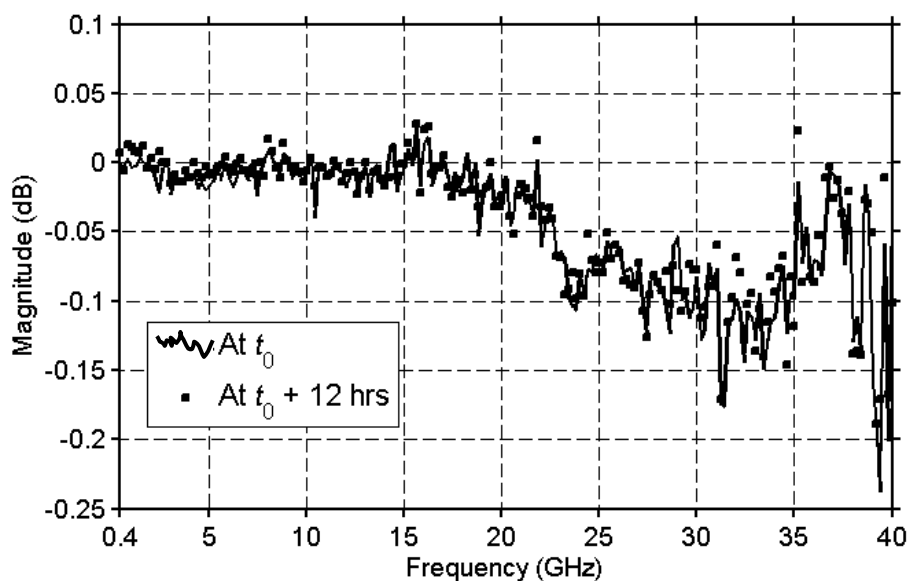


Figure 3.8 Measured reflection coefficient of an off-set open before and after a 12-hour measurement session, indicating similar verification results of the on-wafer VNA calibration, and thus absence of short-term drift.

The closeness of the traces shown in Figure 3.8 indicates that absence of short-term drift in the measurement setup. This test was important because complete sessions of S-parameter characterization for each studied device took several hours (e.g. overnight).

3.2.2.3 Measured Results

S-parameters to be used as database for modeling were measured on two sets of bias points, one set around the V_{th} estimated with static-DC characterization, and another set with bias points in the active region of the IV plane.

Cold pinch-off S-parameters are used in an essential part of the small-signal modeling. Thus, it is important to clearly identify the V_{GS} value corresponding to this bias condition ($V_{DS} = 0V$), which is called $V_{pinch-off}$ in this thesis. The voltage V_{th} estimated with static-DC characterization is usually not precise enough, and therefore a set of S-parameters is measured with V_{GS} varying around V_{th} ($V_{DS} = 0V$).

As will be clarified in the Chapter 4 (section 4.2.3), identification of small-signal model parameters begins with the capacitance parameters. The database to calculate capacitance parameters consists of low-frequency Y-parameter data obtained from *cold pinch-off* S-parameter measurements, using well-known formulae of S- to Y-parameter conversion [54].

Thus, for the selection of $V_{pinch-off}$, S-parameters were measured on *cold* bias points ($V_{DS} = 0V$) with V_{GS} around V_{th} . Then, they converted to Y-parameters and analyzed in the lowest 1-GHz frequency range (between 0.4 and 1.4 GHz). The obtained variations of $Im[Y_{11}]$, $Im[Y_{12}]$ and $Im[Y_{22}]$ with respect to V_{GS} around V_{th} are shown in Figure 3.9.

The $V_{pinch-off}$ value was selected as the first V_{GS} value within pinch-off at which the traces exhibit a steady trend after the transition around V_{th} . According to the results observed in Figure 3.9, the selected $V_{pinch-off}$ value for the 3.2-mm device was -4.2V (highlighted in the graphs of Figure 3.9). Using a similar analysis with measurements of the 2-mm device a $V_{pinch-off}$ value of -2V was selected.

For the presented analysis with the results shown in Figure 3.9, the trends of $Im[Y_{11}]$, $Im[Y_{12}]$ and $Im[Y_{22}]$ were considered steady when the relative variation from one V_{GS} value to the next was lower than 10%.

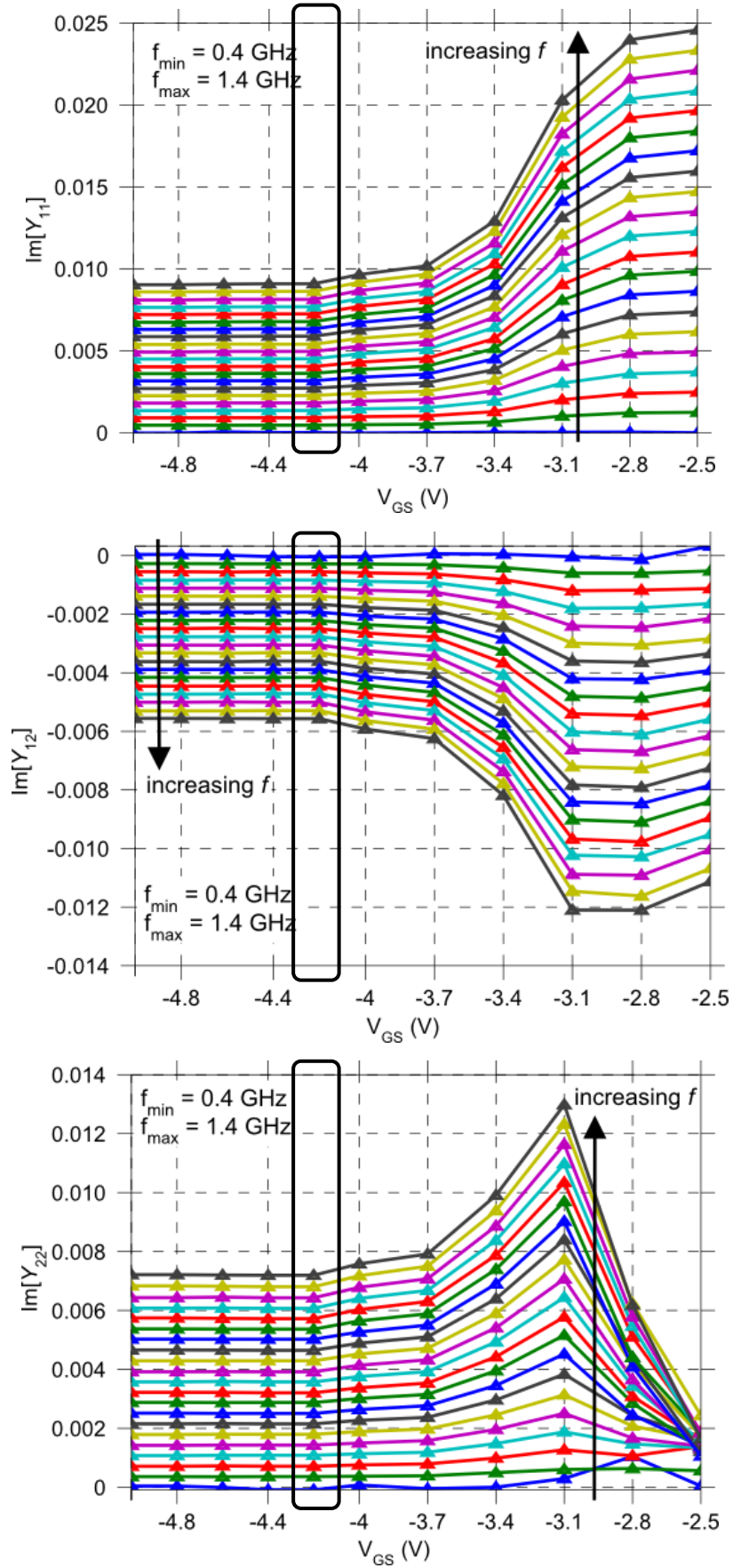


Figure 3.9 Variations with respect to V_{GS} of the low-frequency $\text{Im}[Y]$, obtained from S-parameters measured around V_{th} , for the selection of $V_{\text{pinch-off}}$ for the *cold pinch-off* condition of the 3.2-mm device.

In addition to the measurements used to select $V_{\text{pinch-off}}$, S-parameters were measured on active bias points distributed in all IV regions, following the bias voltage sweeps selected during static-DC IV characterization (see Table 3.2). This resulted in a multitude of measurements for each device, around 1200 for the 3.2-mm device and nearly 1100 for the 2-mm device.

Figure 3.10 and Figure 3.11 show S-parameters of the studied large-size devices measured on active bias points. They exemplify the reliability check by visual inspection performed on all S-parameter measurements. For brevity and clarity of presentation, example measurements are shown only on a selection of V_{DS} values with: (i) $V_{GS} = V_{\text{pinch-off}}$, (ii) $V_{\text{pinch-off}} < V_{GS} < 0V$ and (iii) $V_{GS} = 0V$.

Visual inspection of frequency dependency of the example measurements confirms continuous variations with frequency and lack of inconsistencies (step-like discontinuities), resonances or major ripples. Following [59], the above remarks, besides VNA calibration verification, provide confidence to accept the measurements as reliable description of device response. Double-arch S_{22} traces⁴, often seen for large-size GaN HEMTs [61-66], are well portrayed in the measurements of Figure 3.10(b) and Figure 3.11(b).

Visual inspection of the bias dependency of the example measurements allows the following observations that reassure measurement reliability:

- In Figure 3.10(a) and Figure 3.11(a) with $V_{GS} = V_{\text{pinch-off}}$, the S_{11} and S_{22} traces are similar, with visible differences only at the highest and lowest frequencies, whereas S_{12} and S_{21} traces are equivalent (note that the negation of the S_{22} trace means a graphical 180°-translation with respect to the chart center). S_{11} - S_{22} similarity and S_{12} - S_{21} equality are consistent with passive behavior of pinched-off devices, e.g. as in [64, 65, 67-69].
- In Figure 3.10(b-c) and Figure 3.11(b-c) with $V_{GS} > V_{\text{pinch-off}}$, S_{11} - S_{22} similarity and S_{12} - S_{21} equality vanish. The S_{22} and S_{21} traces transform more evidently with increasing V_{GS} than the S_{11} and S_{12} traces, as usually reported [64, 65, 67-69]. It is thought that the more marked transformations of the S_{22} and S_{21} traces with V_{GS} are due to the V_{GS} -dependences of the device output impedance and transconductance. The shift leftwards in the Smith chart of the S_{22} traces, with increasing V_{GS} , is explained by related increase of device output conductance.

⁴ Often called “kink phenomenon”, though this thesis disfavors the term to avoid confusion with well-known “kink-effects” of DC IV characteristics. In [60] double-arch S_{22} traces are attributed to a general ambivalence of the output impedance: series- and shunt-RC at low and high frequencies, respectively.

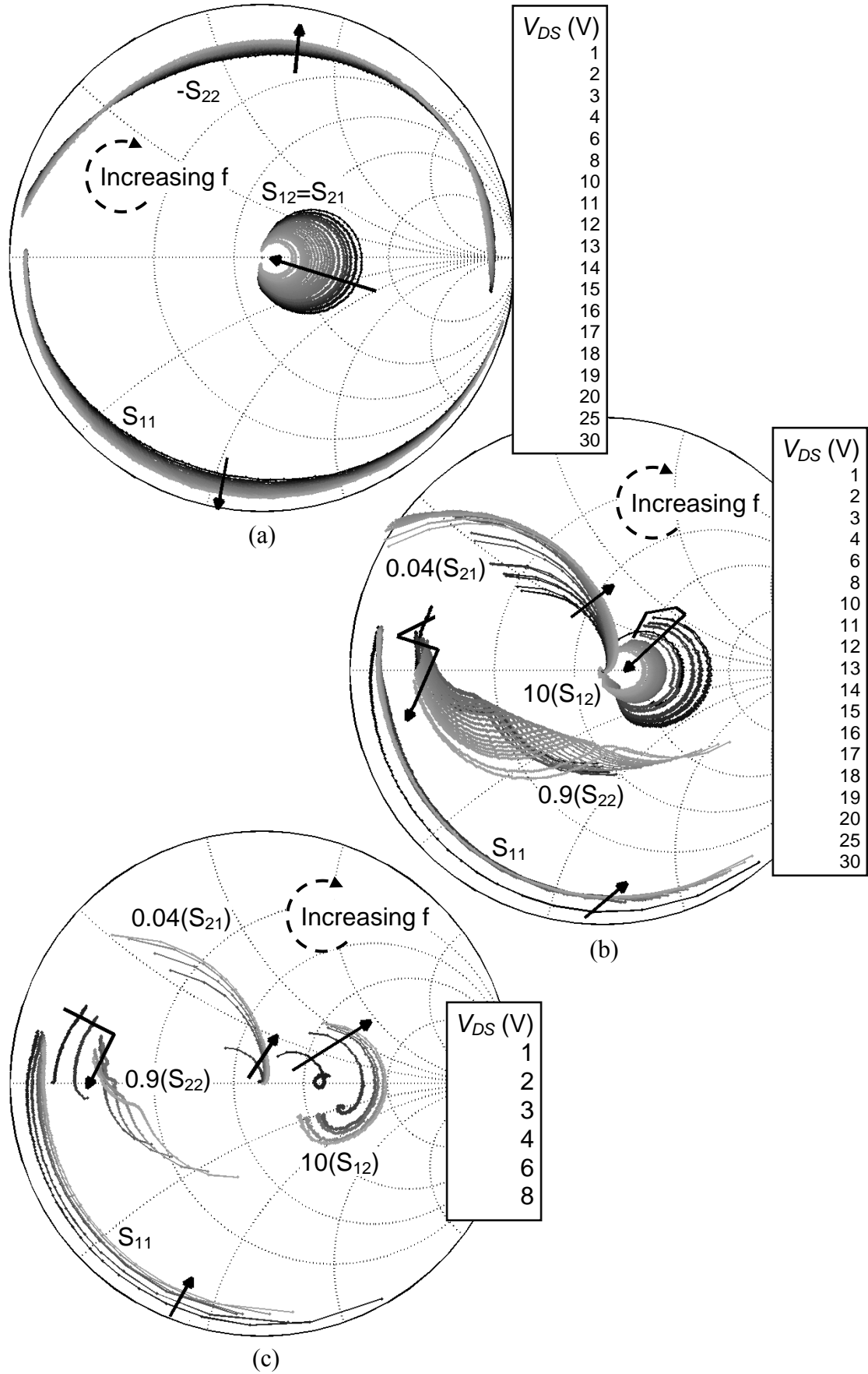


Figure 3.10 Example S-parameters of the 3.2-mm device measured on 200 frequency points from 0.4 to 18 GHz on active bias points with: (a) $V_{GS} = V_{\text{pinch-off}}$, (b) $0V > V_{GS} > V_{\text{pinch-off}}$ and (c) $V_{GS} = 0V$ (solid arrows indicate variations with increasing V_{DS}).

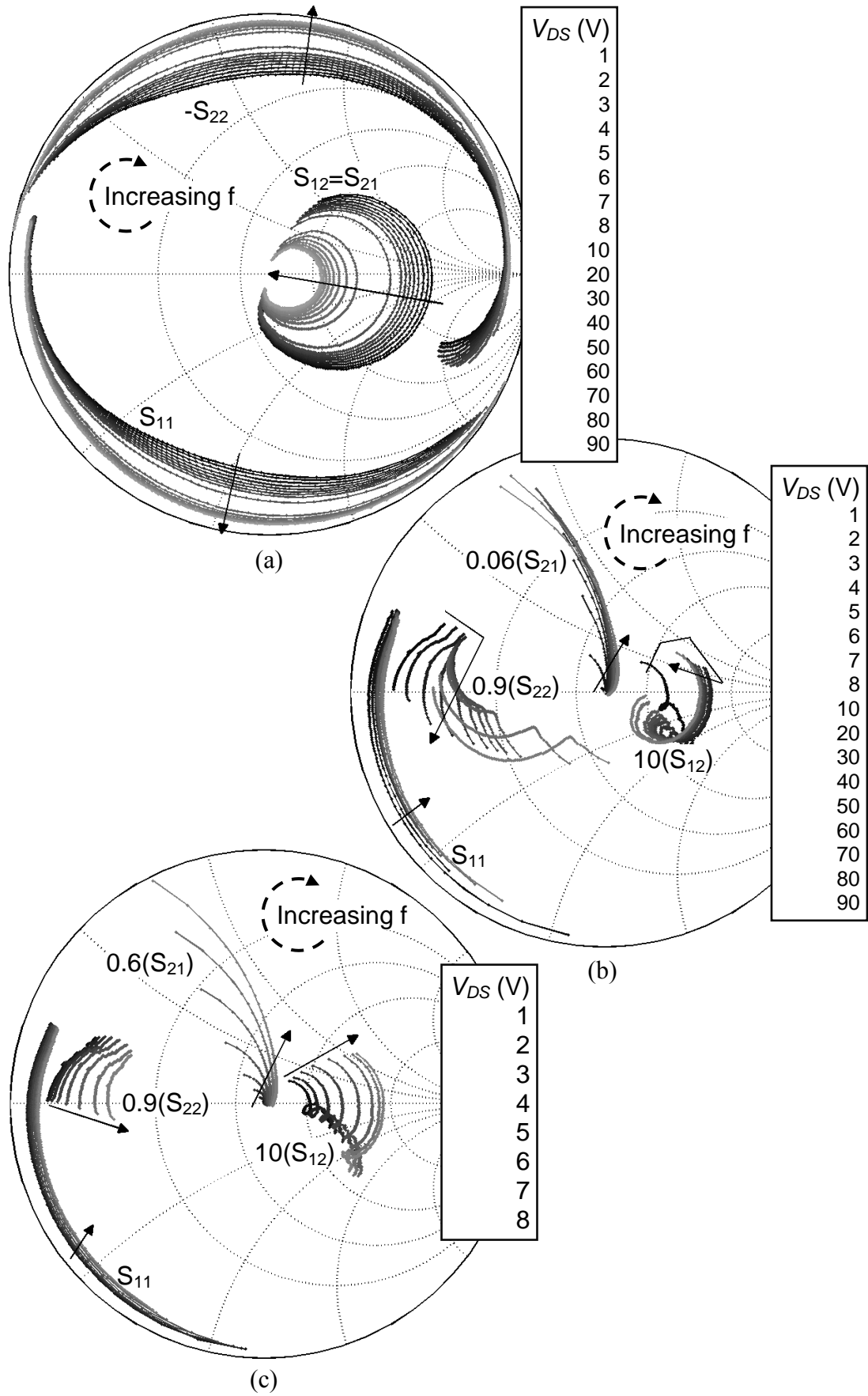


Figure 3.11 Example S-parameters of the 3.2-mm device measured on 197 frequency points from 0.4 to 18 GHz on active bias points with: (a) $V_{GS} = V_{\text{pinch-off}}$, (b) $0V > V_{GS} > V_{\text{pinch-off}}$ and (c) $V_{GS} = 0V$ (solid arrows indicate variations with increasing V_{DS}).

3.2.3 Pulsed-DC Measurements

3.2.3.1 Description

Measurements of the drain current were performed using pulsed voltages as bias condition instead of static-DC values. This was proposed to minimize thermal effects. Since such effects are delay processes with specific time constants, drain current is in fact measured without important thermal effects using widths of the voltage pulses significantly smaller than the time constants of thermal effects. If the pulse repetition time is much larger than the pulse width, i.e. the duty cycle is low, the heat produced by the current on each pulse cannot add up effectively to the next pulse. The static-DC bias point characterized by V_{GS} and V_{DS} , on which the pulses are superimposed, is referred to as the *quiescent* bias point. From the *quiescent* bias point, voltage pulses with varying amplitude produce any *pulsed-to* point desired, that is, any pair of v_{GS} and v_{DS} . Sweeping the v_{GS} and v_{DS} values of these *pulsed-to* points produces a pulsed-DC IV characteristic that is specific to the *quiescent* bias point employed.

Figure 3.12(a) shows an example pulsed-DC IV characteristic with the *quiescent* bias point marked with a star marker. Pulses are applied from this point to the *pulsed-to* points that are indicated with circle markers.

Figure 3.12(b) shows the applied voltage pulses and measured current transient for one example *pulsed-to* point. These signals were illustrated in Figure 3.12(a) with an arrow and the example point with a square marker.

Generally, the measured current transient has four recognizable phases or regions in the time scale [70], which are indicated at the bottom of Figure 3.12(b) and whose descriptions are the following:

- Region I is the turn-on transient. It usually includes ringing and the adjustment of the fast device processes to the *pulsed-to* voltages [70].
- Region II represents a fast-process plateau of current where fast device processes have adjusted to the dynamic condition but slow device processes have not yet changed from the *quiescent* condition [70].
- Region III contains slow-process adjustments to the *pulsed-to* voltages. It involves charge interaction with traps (typically in the order of μ s to ms) and electrical changes due to the device heating/cooling (typically in the order of ms to s) [70].

- Region IV corresponds to the steady-state (static-DC) current that appears when the adjustment to the dynamic condition is complete [70].

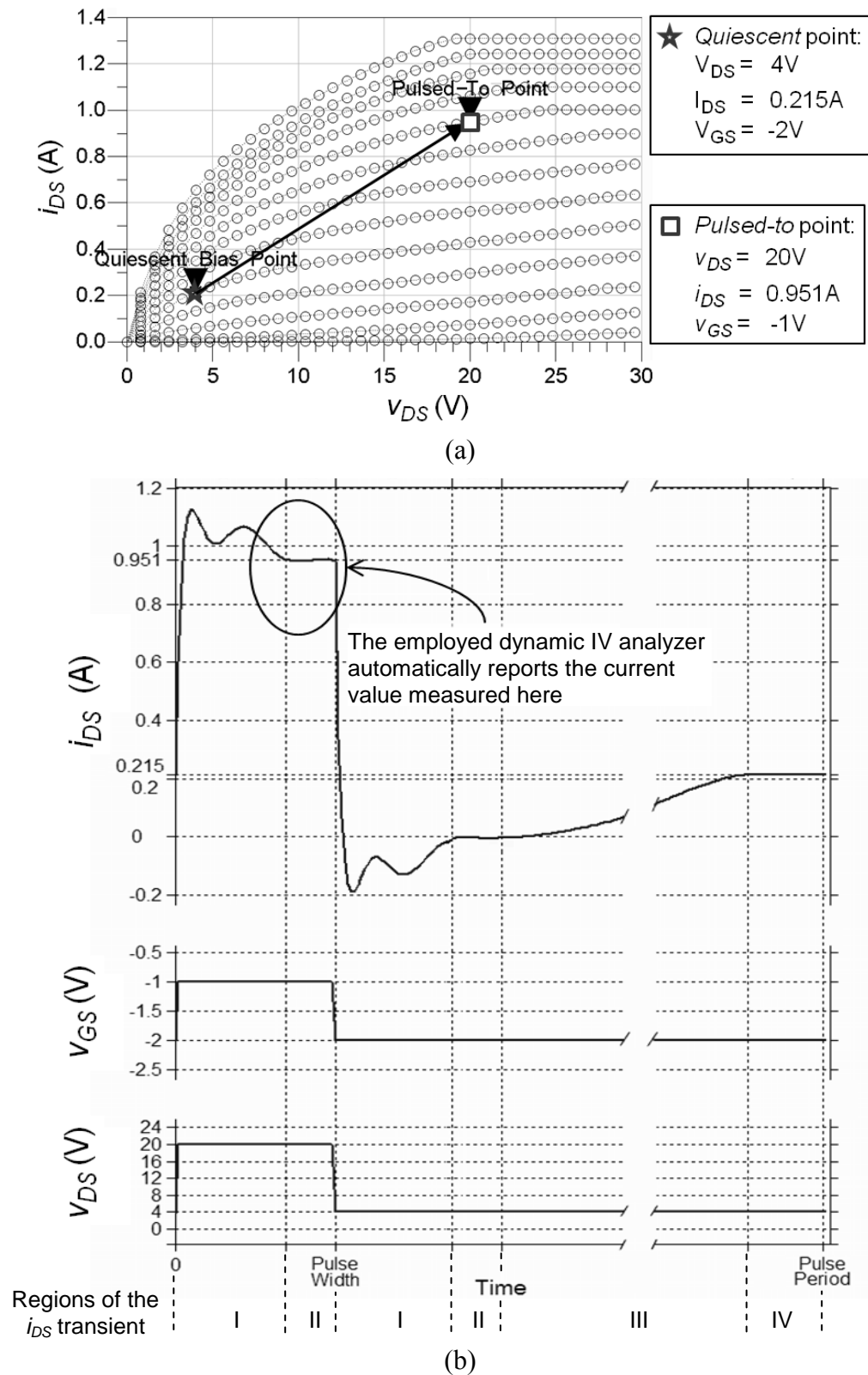


Figure 3.12 (a) Example of pulsed-DC IV characteristics (circles) from a *quiescent* bias point (star), highlighting an example *pulsed-to* point (square). (b) Applied voltage pulses and measured current transient that are illustrated in (a) by an arrow between the *quiescent* bias and an example *pulsed-to* point, hinting the regions of the i_{DS} transient.

Each i_{DS} value in the pulsed-DC IV characteristic must be measured after the turn-on transient and before the onset of the slow-process adjustments [70]. The dynamic IV analyzer employed in this thesis work automatically reports the current measured during the plateau of region II.

In pulsed-DC IV measurements, the device temperature is defined by the case temperature (*thermo-chuck*) and by the device dissipated power at the *quiescent* bias point.

3.2.3.2 Measurement Techniques and Setup

The setup for pulsed-DC IV measurements consisted of the on-wafer probing station connected to a dynamic IV analyzer (DiVA[®] D265EP by Accent[®]). This equipment sets the *quiescent* bias point, generates the DC-voltage pulses with the desired duration and repetition rate and measures the dynamic drain current of the device.

The reference temperature of the measurements was set with a *thermo-chuck* (probing surface of the on-wafer station) and a temperature-control unit, with an accuracy of $\pm 0.1^\circ\text{C}$ and maximum temperature of 150°C .

The power and current limits must be set in the controlling software of the DiVA[®] to assure that the measurements observe the SOA of the device. The static-DC power related to the *quiescent* bias points of interest, P_{DS} , observed $P_{DS\text{max}}^{\text{SOA}}$ of the devices (maximum static-DC drain-source power). The DiVA[®] ratings were I_{DS} of 2A, V_{DS} of 65V and P_{DS} of 30W.

The most important issue of the pulsed-DC IV measurement techniques was the appearance of unstable operation (active device instabilities). According to [70], when the device transconductance is high, spurious oscillations occur, as those of the measurements shown in Figure 3.13.

Measurements with unstable operation occurred mainly on *quiescent* bias conditions located in the IV region associated with high transconductance (V_{GS} and V_{DS} ranges for the steepest I_{DS} slope in the static-DC IV transfer characteristic) and exclusively for the largest device sizes (the 2-mm and 3.2-mm IAF devices and the Nitronex[®] device).

Unstable pulsed-DC IV measurements are unsuitable to be part of the database for the calculation of the model. Besides, strong instabilities generate significant oscillations of the current, which caused the DiVA[®]

controlling software to stop responding and abrupt interruption of the measurement session. When that happens, there is an elevated risk of high-current damage for the device and the measurement equipment.

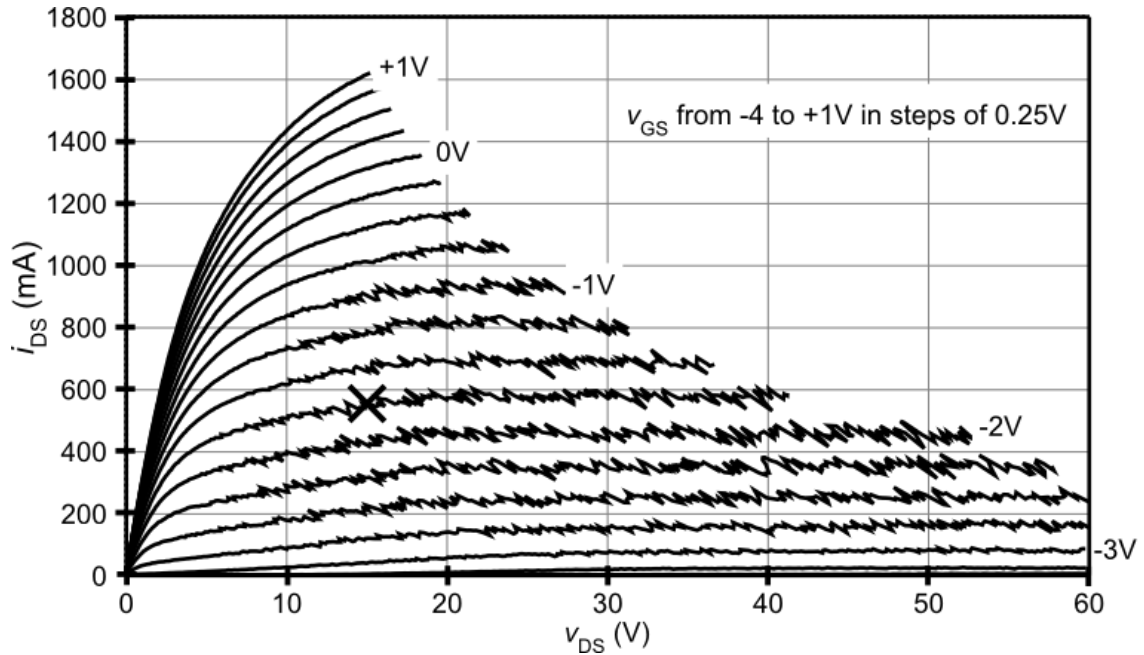


Figure 3.13 Unstable pulsed-DC IV measurements of the 3.2-mm device on the *quiescent* bias point (X-marker) $V_{GS} = -1.75V$, $V_{DS} = 15V$, $I_{DS} \approx 0.55A$, $P_{DS} \approx 8.3W$.

The appearance of instabilities in the measurements constrained the region where *quiescent* bias points can be selected and where reliable and safe measurements are achievable. Unstable operation has not emerged for *quiescent* bias points with zero or negligible drain power, but for points where this power is significant, i.e. $P_{DS} > 0W$. For the studied large-size devices P_{DS} of *quiescent* bias points on which unstable operation appeared was as low as 1W/mm. On another hand, pulsed-DC IV measurements on such *quiescent* bias points with non-negligible P_{DS} are needed to calculate key large-signal model parameters (as will be explained later in subchapter 6.3). Furthermore, unstable operation constrained the pulsed-DC IV database achievable and also the IV region where the model can be successfully verified, ultimately reducing the model validity region.

A stabilization technique was utilized in this thesis work to overcome these drawbacks. The manufacturer of the DiVA[®] recommends to use a stabilizing resistor connected in shunt to the output of unstable FETs and HEMTs (between the drain terminal and ground) [70]. Moreover, the controlling software of the DiVA[®] has a built-in feature that calibrates the effects on the measurements produced by the stabilization technique, where the user only must input the resistance value used as stabilizing resistor.

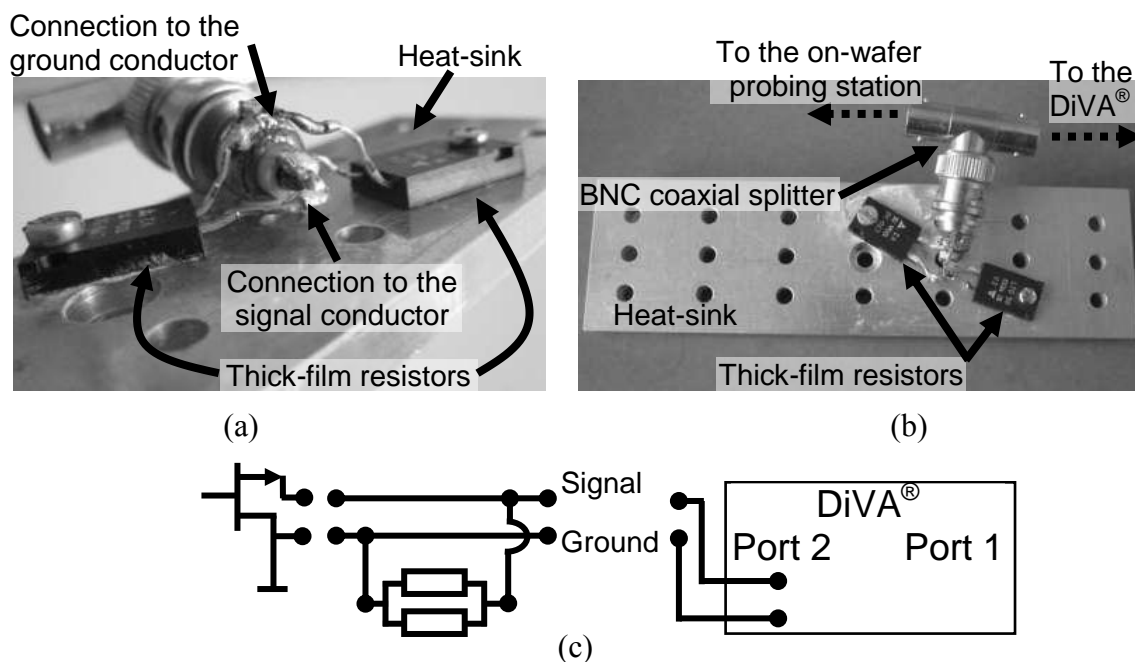


Figure 3.14 (a) Side-view and (b) top-view photographs of the stabilizing element and (c) equivalent circuit of the implementation of the stabilization technique.

The stabilizing element was realized with a BNC coaxial splitter (T-junction) as shown by the photographs in (a) and (b) of Figure 3.14. Thick-film high-power resistors were welded between the ground and signal conductors at one of the three ports of the T-junction, implementing the selected resistance value with two resistors (50W thick-film resistors by Vishay[®] model LTO 50) to split the high heat dissipation expected at the output of the studied devices. Also because of the expected high heat dissipation, a suitable heat sink was included in the stabilizing element, as shown by the photographs in (a) and (b) of Figure 3.14. The stabilization technique was implemented inserting the stabilizing element in the drain path between the corresponding ports of the DiVA[®] and the on-wafer probing station, as shown with an equivalent circuit in Figure 3.14(c).

Figure 3.15 shows stabilizing effects of different resistance values used in the stabilizing element for a device that displayed unstable pulsed-DC IV measurements (the 3.2-mm device). As the figure demonstrates, the stabilizing effect increases as the employed resistance value approaches the device output resistance (measured around 60Ω for the example device whose measurements are presented in Figure 3.15). Figure 3.15(d) shows stable measurements with traces of crosses and circles, corresponding to uncalibrated and calibrated results, respectively. Calibration of the effect of the stabilizing element is carried out by the controlling software of the DiVA[®] (the user inputs the resistance value of the stabilizing element).

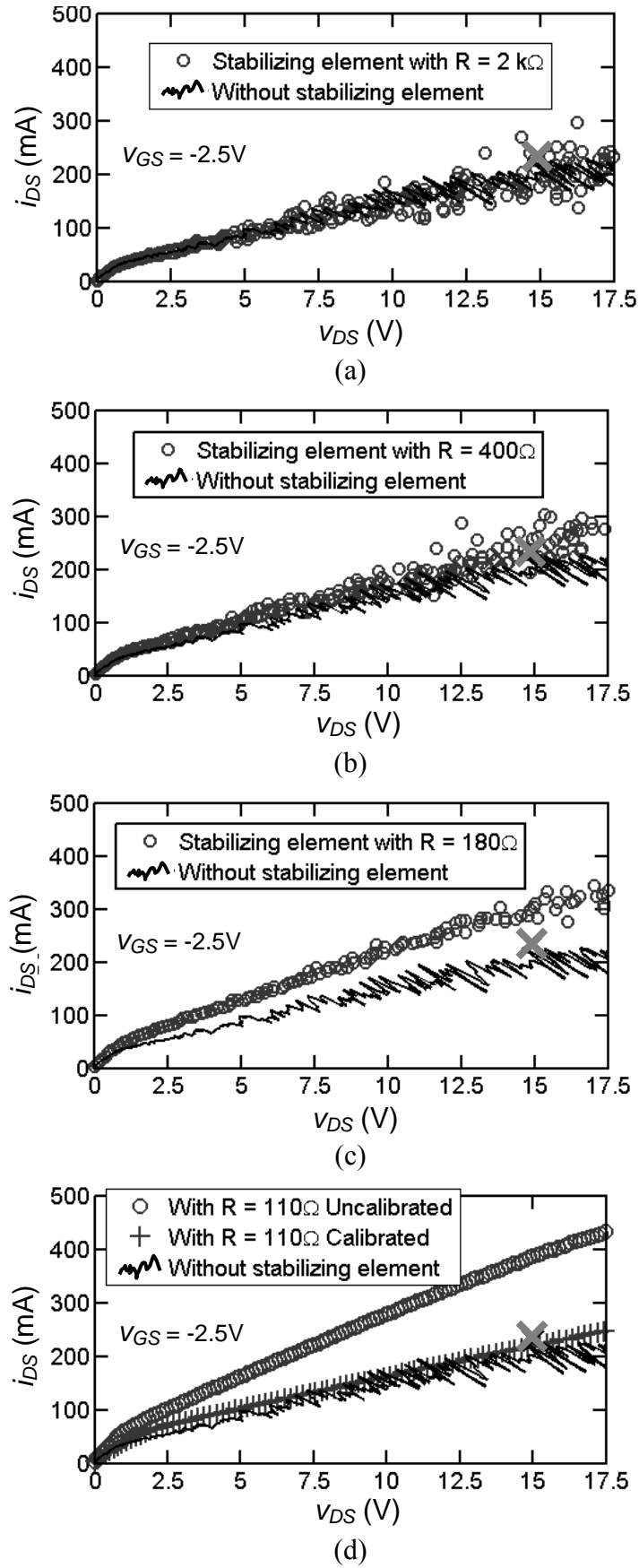


Figure 3.15 Pulsed-DC IV tests using the 3.2-mm IAF device and stabilizing elements with different resistance values: (a) 2 k Ω , (b) 400 Ω , (c) 180 Ω and (d) 110 Ω . Common quiescent bias point (X markers) with $V_{GS} = -2.5\text{V}$, $V_{DS} = 15\text{V}$, $I_{DS} \approx 0.24\text{A}$, $P_{DS} \approx 3.6\text{W}$.

When the stabilization technique is implemented, for every *pulsed-to* point (every pair of v_{DS} and v_{GS}) the current measured by the DiVA[®] in the drain port is different than the current actually flowing through the device output. This is observable in Figure 3.15(d), where the trace of the actual current measured using the stabilizing element without calibration (circle markers), differs from the trend of the unstable measurements (solid line). In reality, during measurements with the stabilizing element the current measured by the DiVA[®] contains two components: (i) One component due to the current flowing through the device output and (ii) another due to the current through the stabilizing element.

After subtracting the effect of the stabilizing element, the calibration done by the DiVA[®] software, the resulting calibrated trace (shown in Figure 3.15(d) with cross markers) approximates better the trend of the unstable measurements (solid line). The difference that is left, although arguably small, suggests that after the calibration done by the DiVA[®] software a residual error remains in the determination of the device drain current. This residual error is likely to be passed to the large-signal model, since pulsed-DC IV measurements are a main part of its database.

In this thesis work, the effect of this residual error was taken into account with an adjustment of the operation bias point in the later simulations performed with the large-signal model. This means, an adjustment of the V_{GS} and V_{DS} values used as bias point for the simulations with respect to the V_{GS} and V_{DS} of the corresponding measurements. The required adjustment was estimated to be lower than $\pm 10\%$ of the nominal V_{GS} and V_{DS} values. This was thoroughly tested with stabilized pulsed-DC IV measurements on several *quiescent* bias points of the studied large-size devices. Figure 3.16 and Figure 3.17 show two examples of those tests.

Figure 3.16 shows pulsed-DC IV measurements on a *quiescent* bias point ($V_{GS} = -2.5\text{V}$, $V_{DS} = 15\text{V}$) in three situations: (i) unstable, (ii) with the stabilizing element and (iii) with the stabilizing element and the *quiescent* bias point adjusted ($V_{GS} = -2.65\text{V}$, $V_{DS} = 16\text{V}$).

Similarly, Figure 3.17 shows unstable pulsed-DC IV measurements on a *quiescent* bias point ($V_{GS} = -1\text{V}$, $V_{DS} = 15\text{V}$) and stabilized measurements with the *quiescent* bias point adjusted ($V_{GS} = -0.94\text{V}$, $V_{DS} = 14\text{V}$).

In the tests presented, the V_{GS} and V_{DS} adjustments (with respect to the original V_{GS} and V_{DS}) that were required to receive equivalent i_{DS} behavior

with and without the stabilizing element were -6% of V_{GS} and $+6.7\%$ of V_{DS} for Figure 3.16 and $+6\%$ of V_{GS} and -6.7% of V_{DS} for Figure 3.17.

In consequence, these tests confirmed that bias-point adjustments lower than $\pm 10\%$ of the nominal V_{GS} and V_{DS} values accounted well for the residual error due to imperfect calibration of the stabilizing element.

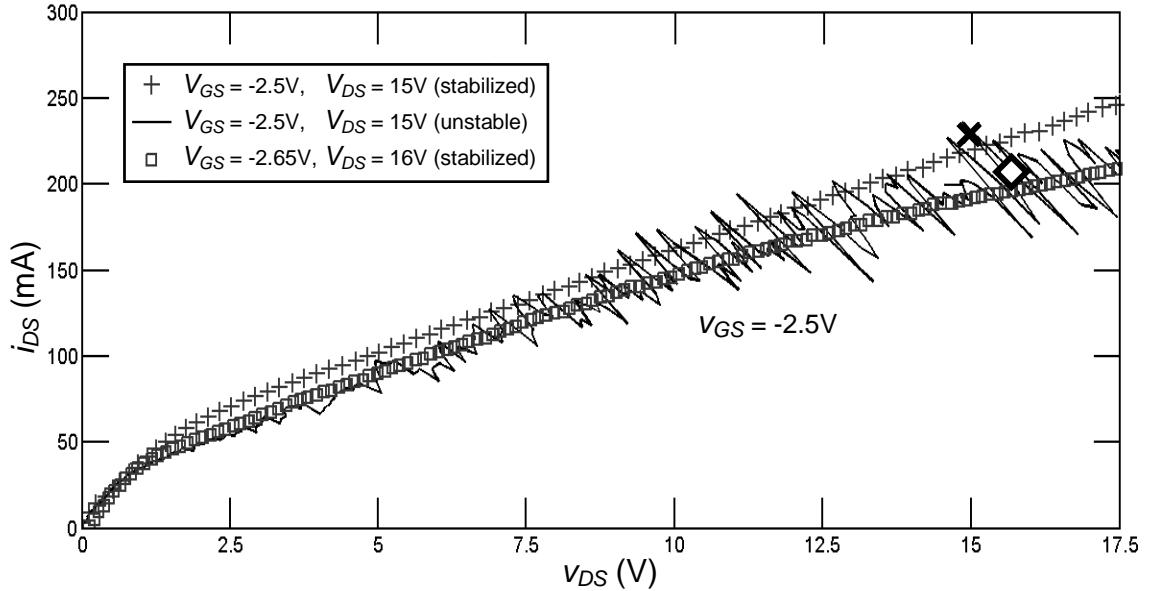


Figure 3.16 Test of bias-point adjustment to account for the residual error of the stabilizing element, showing unstable (solid line) and stable (crosses and squares) pulsed-DC IV measurements on a *quiescent* bias point (X marker) and stable measurements equivalent to the unstable trace with the bias point adjusted (diamond).

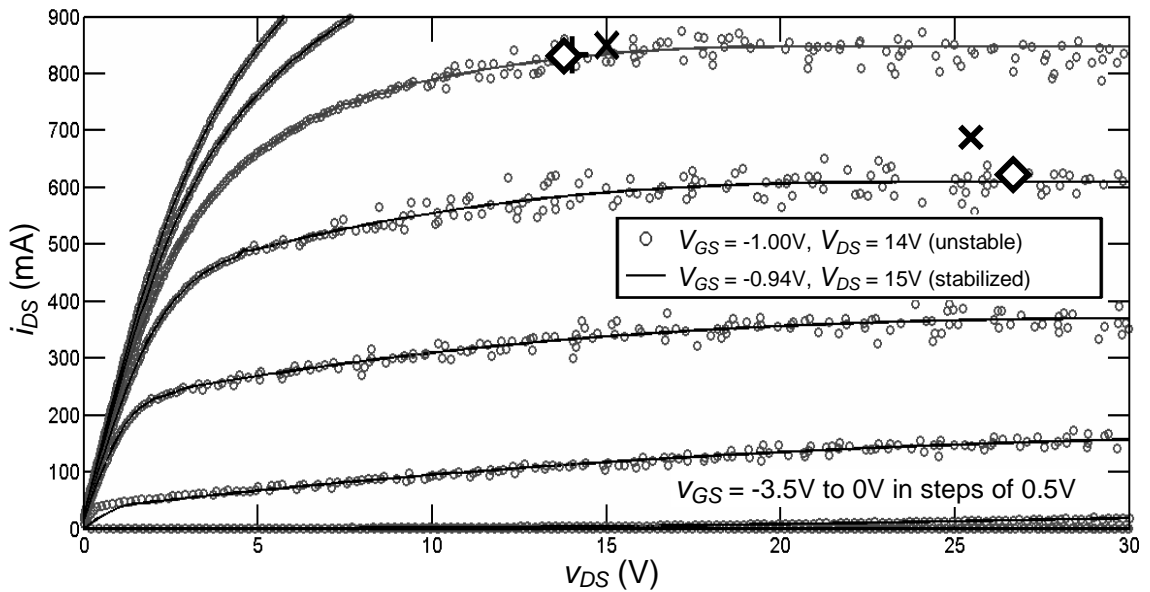


Figure 3.17 Further test of bias-point adjustment to account for the residual error of the stabilizing element, showing unstable pulsed-DC IV measurements (circles) on a *quiescent* bias point (X marker) and stable measurements that are equivalent (solid lines) on an adjusted *quiescent* bias point (diamond).

The stabilization technique was tested to assure that characterization was possible with *quiescent* bias points in a broad IV region, in order to allow later the optimal selection of the database for large-signal modeling and for the model verification with pulsed-DC IV measurements.

Figure 3.18 displays a stable pulsed-DC IV characteristic measured utilizing the stabilization technique discussed above, on a *quiescent* bias point with a P_{DS} of approximately 16W.

That level of output power of the *quiescent* bias point is almost 5 times the level of the stable measurements previously shown in Figure 3.15. The maximum P_{DS} achievable in pulsed-DC IV measurements of the same device without the stabilization technique was roughly 5W.

Without stabilization it was a must to avoid *quiescent* bias points on the IV region related to high transconductance, where unstable operation appeared more often (such region is observable in the static-DC IV transfer characteristic as the V_{GS} and V_{DS} ranges for the steepest I_{DS} slope).

Clearly, the stabilization technique effectively relieved the constraints to the database of pulsed-DC IV measurements.

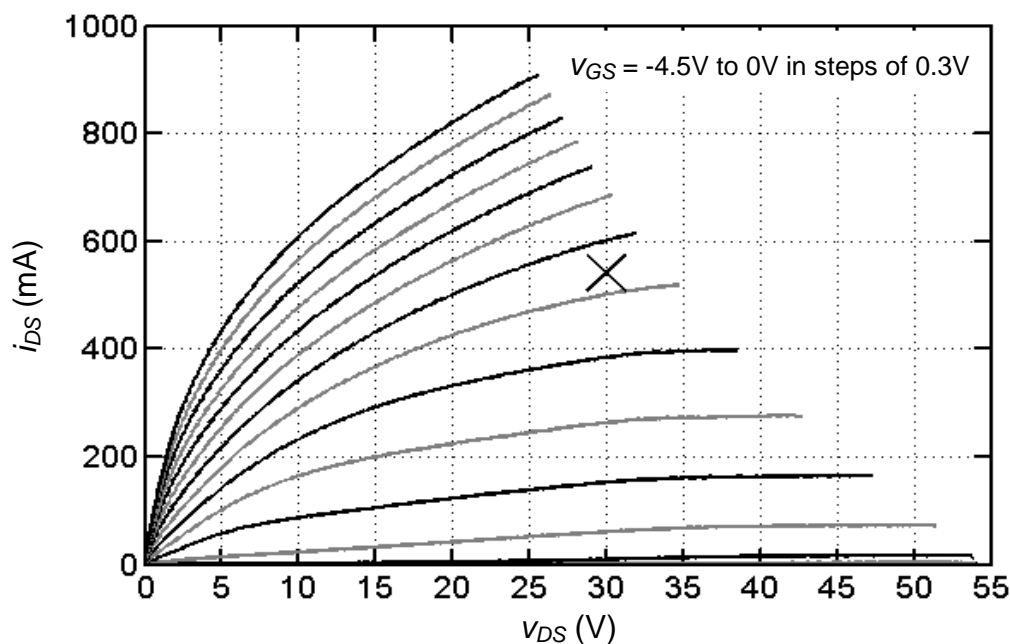


Figure 3.18 Pulsed-DC IV measurement obtained with the stabilization technique, otherwise unfeasible due to the high P_{DS} of nearly 16W and the *quiescent* bias point location (X marker), which was $V_{GS} = -2V$, $V_{DS} = 30V$, $I_{DS} \approx 0.54A$.

For pulsed-DC IV measurements using the stabilizing element, the maximum V_{DS} achievable is 54V, in contrast with the nominal DiVA[®] rating of maximum V_{DS} equal to 65V.

Conversely, the maximum P_{DS} for stable pulsed-DC IV measurements is approximately 17W (with $V_{DS}=30V$), in contrast with the nominal DiVA[®] rating of maximum P_{DS} equal to 30W.

Maximum ratings of stable pulsed-DC IV measurements are lower than the DiVA[®] nominal values because the current attributable to the device output is only a part of the current actually measured, and there is always another component of the current that is flowing in the stabilizing element (thus, also a component of power that is being dissipated there).

3.2.3.3 Results on Passive *Quiescent* Bias Points

Table 3.3 lists the passive *quiescent* bias points for pulsed-DC IV characterization (i.e. $I_{DS} \approx 0A$, $P_{DS} \approx 0W$) of the studied large-size devices.

Figure 3.19 and Figure 3.20 show the pulsed-DC IV characteristics that were measured for the studied large-size device sizes on the *quiescent* bias point with $V_{GS} = 0V$ and $V_{DS} = 0V$.

Table 3.3 Passive *quiescent* bias points for pulsed-DC IV characterization of the studied large-size devices.

General nomenclature	3.2-mm device		2-mm device	
	V_{DS} (V)	V_{GS} (V)	V_{DS} (V)	V_{GS} (V)
$V_{DS} = 0V$, $V_{GS} = 0V$	0	0	0	0
$V_{DS} = 0V$, $V_{GS} < V_{th}$	0	-6	0	-2.4
$V_{DS} \gg 0V$, $V_{GS} < V_{th}$	54	-6	30	-2.4

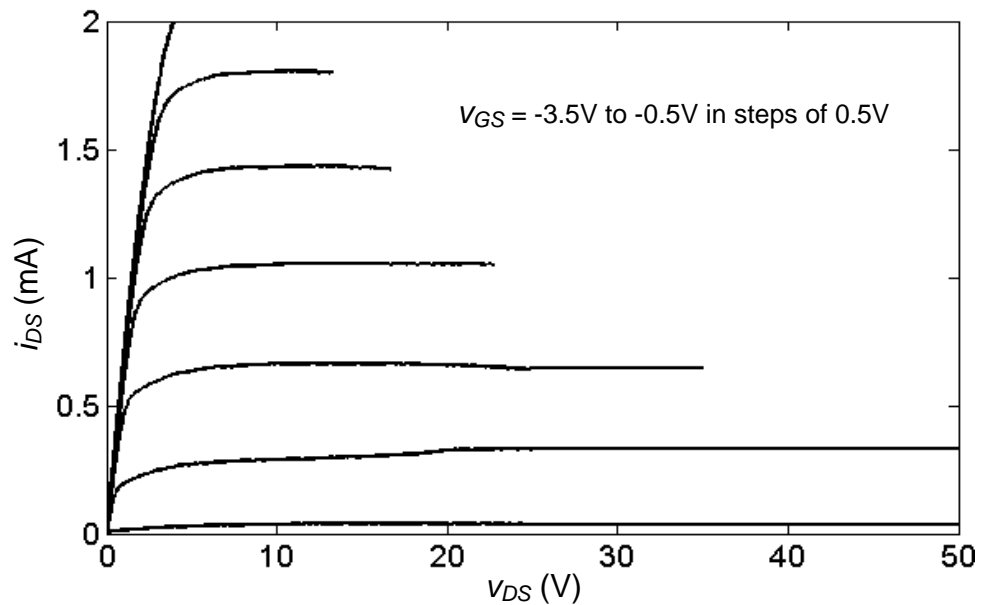


Figure 3.19 Results of pulsed-DC IV measurements on $V_{GS}=0V$ and $V_{DS}=0V$ of the 3.2-mm device.

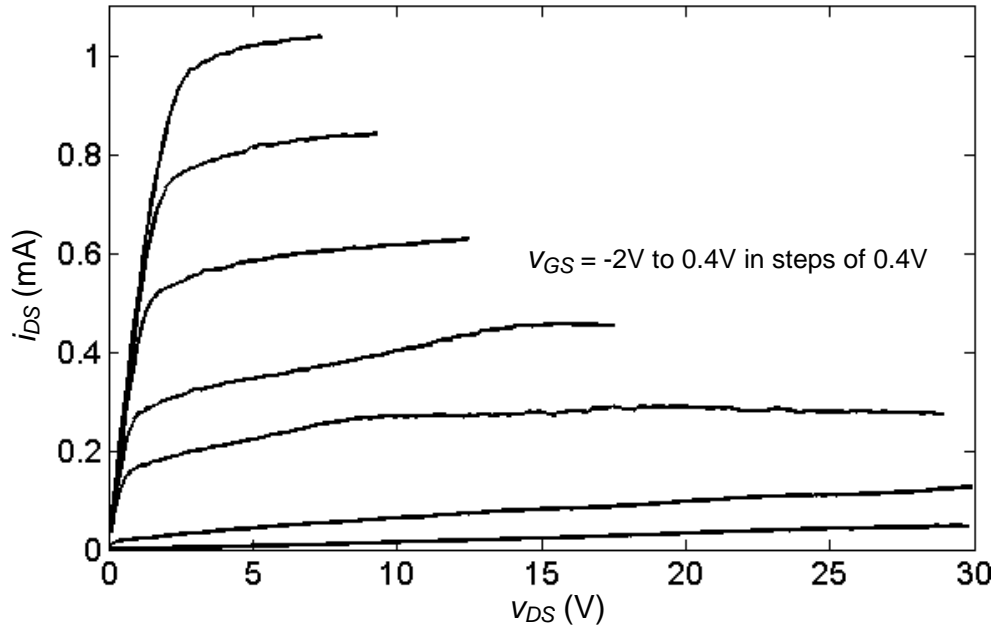


Figure 3.20 Results of pulsed-DC IV measurements on $V_{GS} = 0V$ and $V_{DS} = 0V$ of the 2-mm device.

On $V_{GS} = 0V$ and $V_{DS} = 0V$ the pulsed-DC IV measurements usually present the maximum i_{DS} values, because charge-trapping effects activated by V_{GS} and V_{DS} are not triggered, and because pulsed-DC operation itself diminishes self-heating effects. Therefore, the i_{DS} reduction induced by dispersion is minimized and the highest i_{DS} values can be measured.

This conduced to pulsed-DC IV measurements on such *quiescent* bias point with i_{DS} values reaching the maximum current rating of the DiVA[®] (2A), for the 3.2-mm device and v_{GS} approaching 0V. As a result, in the measurements shown in Figure 3.19, the curve for $v_{GS} = -0.5V$ appears truncated before reaching the saturation region, at $v_{DS} > 4V$. In curves for $v_{GS} \leq -0.5V$, measured i_{DS} values were only constrained by the power limit.

That truncation of i_{DS} shown in Figure 3.19 demonstrates one major reason why model scalability is important for empirical transistor modeling applied to large-size GaN HEMTs: The capabilities of such devices potentially surpass the measurement equipment ratings.

Figure 3.21 and Figure 3.22 present pulsed-DC IV measurement results for the studied large-size devices on *quiescent* bias points where $V_{GS} < V_{th}$ with (i) $V_{DS} = 0V$ and with (ii) V_{DS} equal to a large value (54V for the 3.2-mm device and 30V for the 2-mm device). These are also *quiescent* bias points, since $I_{DS} \approx 0A$ and $P_{DS} \approx 0W$.

In the measurement results of Figure 3.21 and Figure 3.22, charge-trapping effects activated by V_{DS} appeared more pronounced for 3.2-mm

device than for the 2-mm device. This is partly because the change in V_{DS} for the 3.2-mm device was larger than for the 2-mm device, 54V and 30V, respectively. Besides, the different of the current collapse effects seemed to indicate different kind of activated V_{DS} -activated charge-trapping effects.

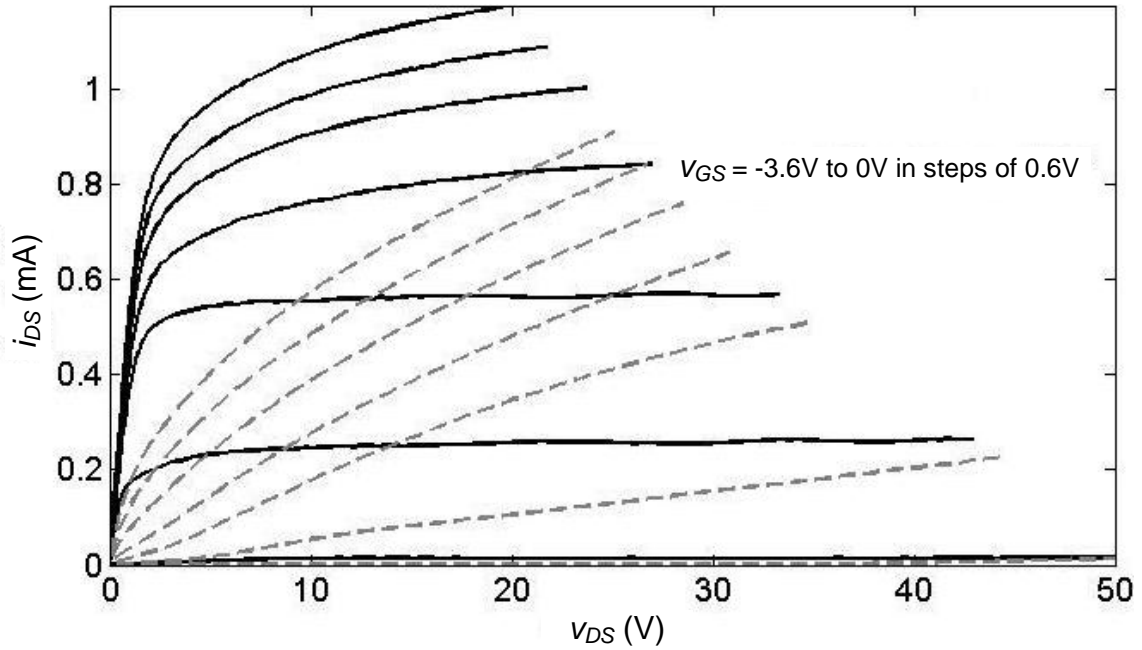


Figure 3.21 Results of pulsed-DC IV measurements for the 3.2-mm device on passive *quiescent* bias points ($I_{DS} = 0A$ and $P_{DS} = 0W$) with $V_{GS} = -6V$ and $V_{DS} = 0V$ (solid line), and with the same V_{GS} and $V_{DS} = 54V$ (dashed line).

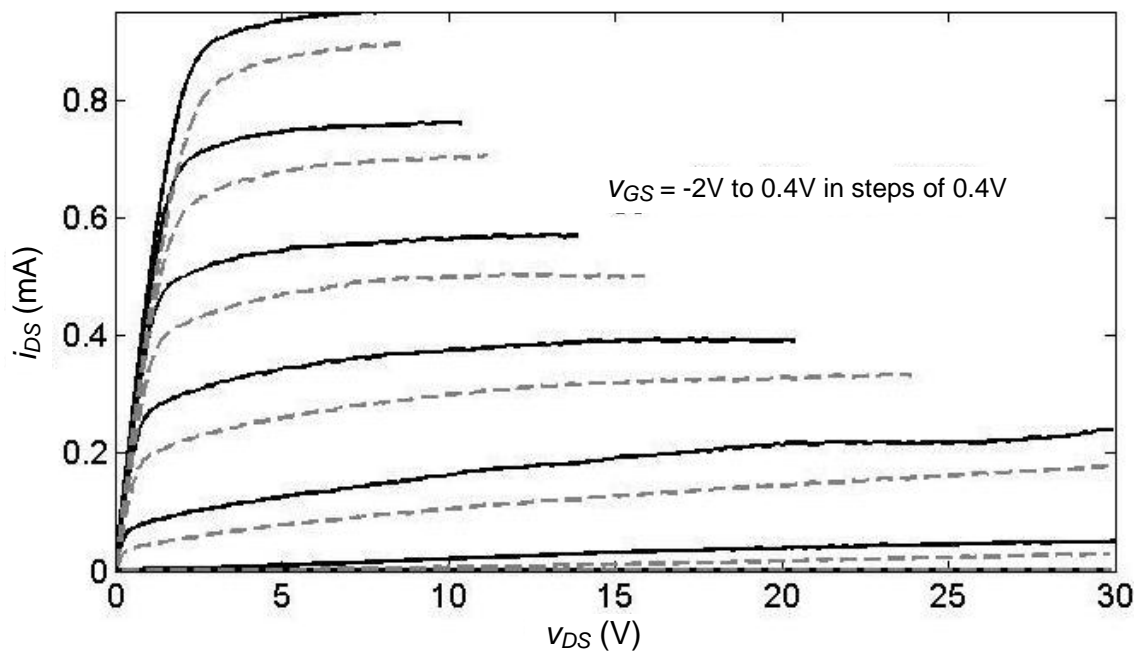


Figure 3.22 Results of pulsed-DC IV measurements for the 2-mm device on passive *quiescent* bias points ($I_{DS} = 0A$ and $P_{DS} = 0W$) with $V_{GS} = -4V$ and $V_{DS} = 0V$ (solid line), and with the same V_{GS} and $V_{DS} = 30V$ (dashed line).

Moreover, device fabrication technology engineered by Nitronex[®] seems to be the main reason for the lower V_{DS} -activated charge-trapping effects observed for the 2-mm device, than for the 3.2-mm device.

That patent-protected highly-optimized fabrication technology of the device layer structure is reported in [51]. According to Nitronex[®], their high-quality growth process of active GaN layers, with optimized compositions and thicknesses, produces devices with improved material properties, RF performance and reliability [51].

3.2.3.4 Results of Active *Quiescent* Bias Points

The stabilization technique presented in section 3.2.3.2 was implemented as illustrated in Figure 3.14(c) to perform pulsed-DC IV characterization on active *quiescent* bias points of the large-size devices. The measured P_{DS} of these active *quiescent* bias points ranges from approximately 0.25 to 5W for the 2-mm device and from 1 to around 16W for the 3.2-mm device.

The set of active *quiescent* bias points selected the studied large-size devices are illustrated in the following Figure 3.23 and Figure 3.24 with star markers.

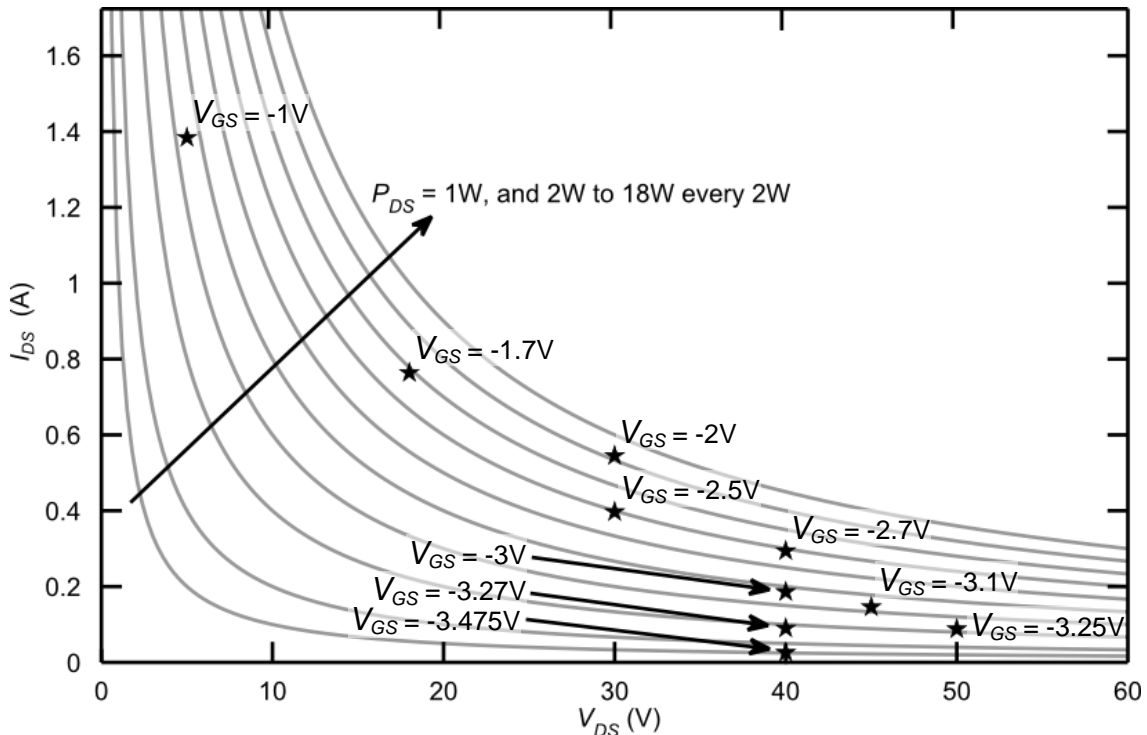


Figure 3.23 Set of active *quiescent* bias points selected for this part of pulsed-DC IV characterization of the 3.2-mm device (star markers).

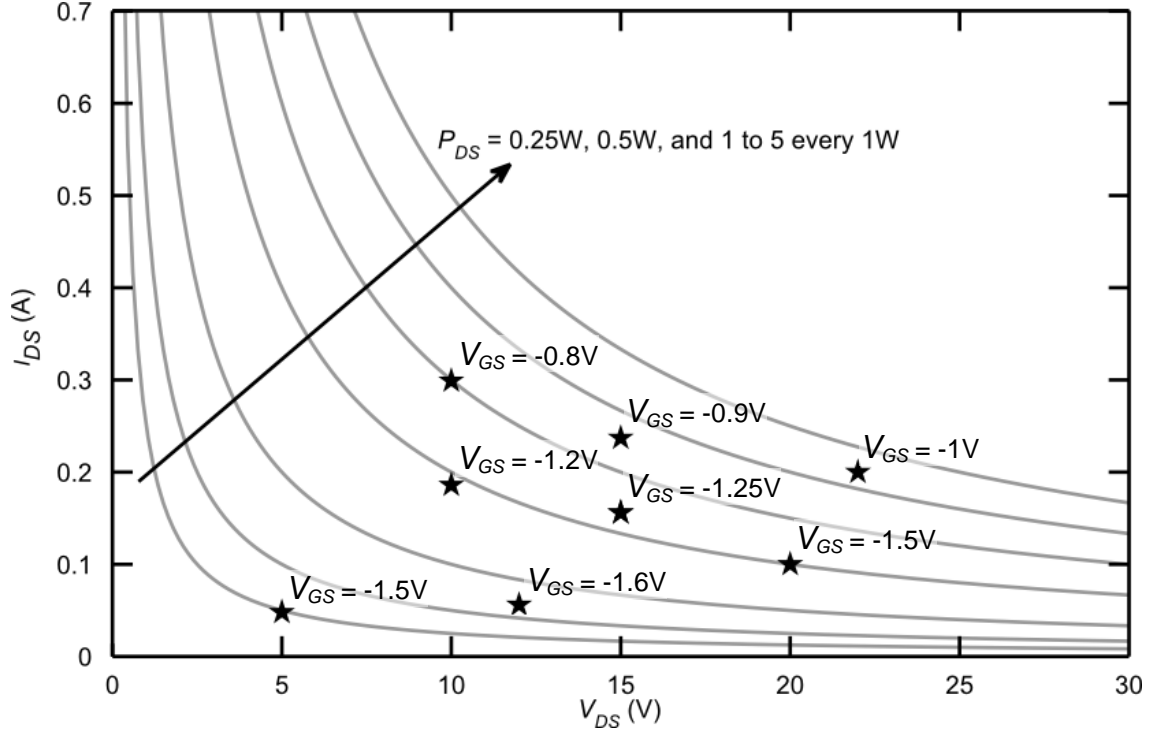


Figure 3.24 Set of active *quiescent* bias points selected for this part of pulsed-DC IV characterization of the 2-mm device (star markers).

The graphs of Figure 3.23 and Figure 3.24 are mapped in V_{DS} - I_{DS} planes, indicating the V_{GS} value of each *quiescent* bias point and containing curves of constant- P_{DS} , so that all the DC-values that characterize each point (V_{DS} , V_{GS} , I_{DS} and P_{DS}) are adequately represented.

Figure 3.23 and Figure 3.24 show that active *quiescent* bias points of pulsed-DC IV measurements were distributed along ranges of V_{DS} , V_{GS} and P_{DS} that in essence were limited only by the device SOA and IV limits of the DiVA[®]. The selection of active *quiescent* bias points along broad V_{DS} , V_{GS} and P_{DS} ranges is especially important for the parameter extraction of the large-signal I_{ds} model, because the V_{DS} , V_{GS} and P_{DS} values control the equation adopted in this thesis work for the low-frequency dispersive behavior of the drain current (this model formulation and related parameter extraction are explained in detail in subchapters 6.3 and 6.3.2). In general, characterization on active *quiescent* bias points along extended ranges of V_{DS} , V_{GS} and P_{DS} provides a broad database for the modeling phase of parameter extraction, and also for the posterior phase of model verification.

Figure 3.25 and Figure 3.26 present example results of pulsed-DC IV characterization on active *quiescent* bias points for the studied large-size devices. Each figure presents two active *quiescent* bias points with the same V_{DS} , but two different P_{DS} values: $V_{DS} = 40V$ with $P_{DS} \approx 1W$ and $12W$

for the 3.2-mm device, and $V_{DS} = 15\text{V}$ with $P_{DS} \approx 2\text{W}$ and 4W for the 2-mm device. Those two bias points for each device were chosen to highlight the influence of thermal effects related to *quiescent* power dissipation (self-heating effects) on the pulsed-DC IV measurements.

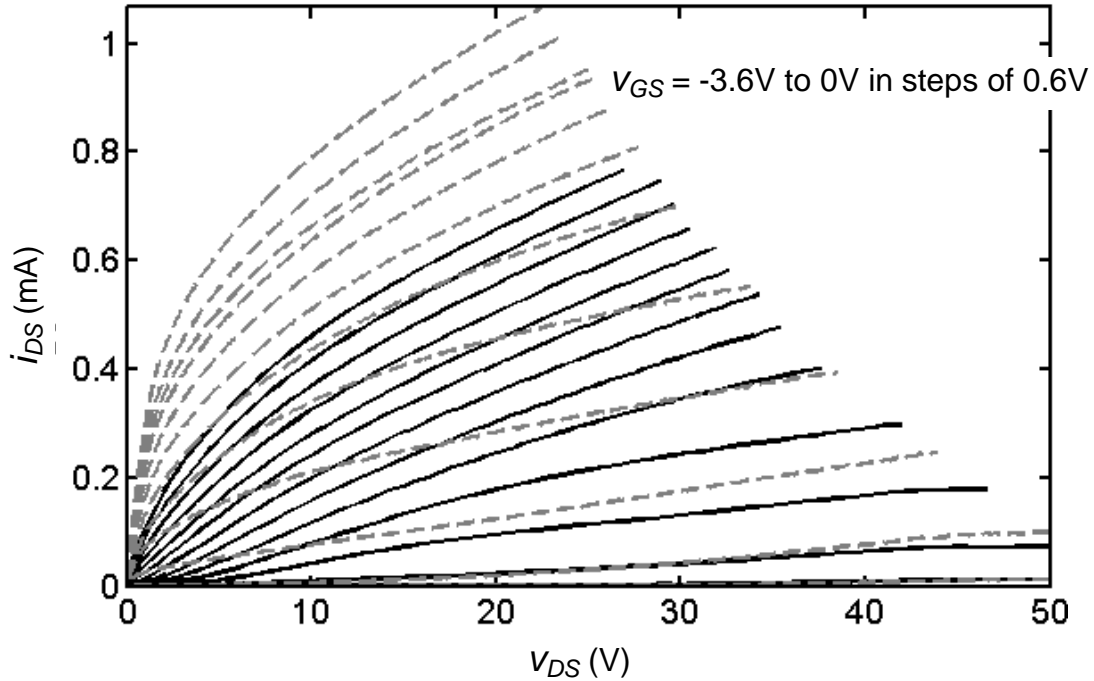


Figure 3.25 Pulsed-DC IV characteristics of the 3.2-mm device measured on the active *quiescent* bias points $V_{GS} = -3.475\text{V}$, $V_{DS} = 40\text{V}$, $P_{DS} \approx 1\text{W}$ (solid line), and $V_{GS} = -2.7\text{V}$, $V_{DS} = 40\text{V}$ and $P_{DS} \approx 12\text{W}$ (dashed line).

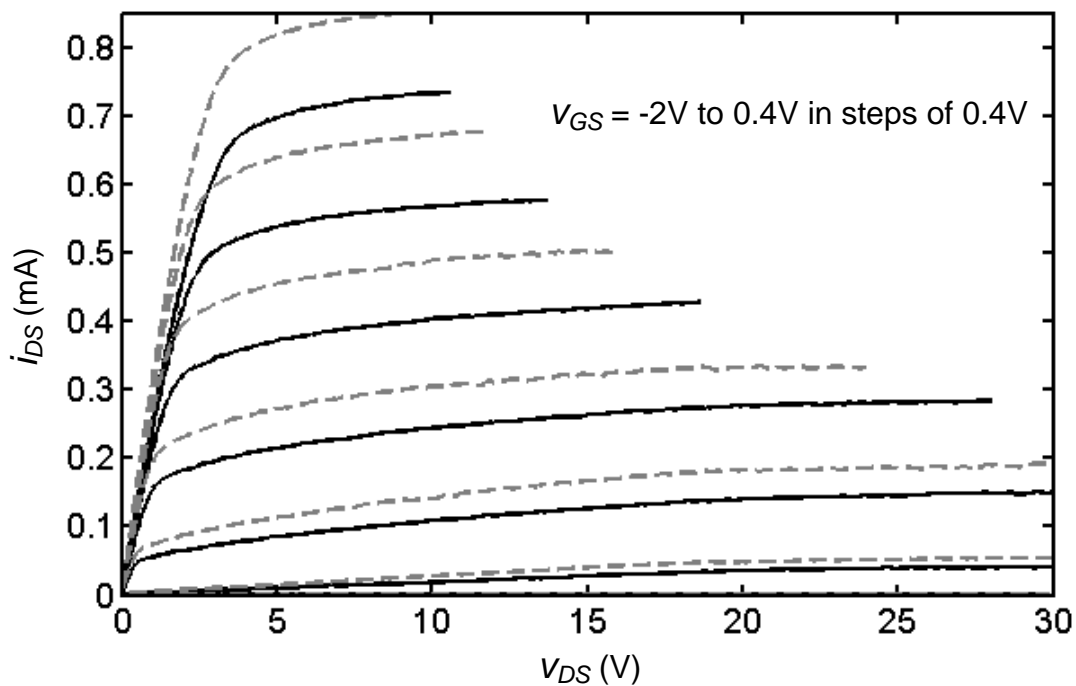


Figure 3.26 Pulsed-DC IV characteristics of the 2-mm device measured on the active *quiescent* bias points $V_{GS} = -0.9\text{V}$, $V_{DS} = 15\text{V}$, $P_{DS} \approx 2\text{W}$ (solid line), and $V_{GS} = -1.25\text{V}$, $V_{DS} = 15\text{V}$ and $P_{DS} \approx 4\text{W}$ (dashed line).

The characterization results presented in Figure 3.25 and Figure 3.26 show that an increase on *quiescent* dissipated power produces a drop of the measured i_{DS} values, due to the augmented heat generation. For instance, the maximum i_{DS} value that was measured decreased around 35% for the 3.2-mm device, and dropped nearly 20% for the 2-mm device.

However, these drop percentages of current alone are misleading and they must be put into context taking into account two further aspects: (i) the difference in device sizes and (ii) the P_{DS} increases of the example *quiescent* bias points considered. The increase percentages of P_{DS} were 1100% for the 3.2-mm device and 100% for the 2-mm device.

Now let us analyze these increase percentages of P_{DS} in correlation with the device size, by denoting P_{DS} as power density per mm. The results are a 343%-increase of P_{DS}/mm for the 3.2-mm device and a 50%-increase of P_{DS}/mm for the 2-mm device.

Then, interestingly, the 3.2-mm device seems to have a better thermal capability, because it manages a 343%-increase of P_{DS}/mm with a 35%-drop of current, whereas the 2-mm device exhibits a 20%-drop of current with a 50%-increase of P_{DS}/mm .

This conclusion was to be expected, because the 3.2-mm device is built over a SiC substrate, whereas the substrate of the 2-mm device is Si (this was explained at the beginning of the chapter where the studied transistors were introduced).

The advantageous thermal capability of the 3.2-mm device is thought to originate in the better thermal conductivity of SiC compared with Si (subsection 2.3.1.3 discussed the comparison of SiC and Si and gave values of their thermal conductivities in Table 2.2).

3.3 Large-Signal Characterization for Model Verification

3.3.1 Description

Large-signal measurements were used in this thesis work for model verification. These measurements characterize the real device behavior under different excitations on the large-signal regime, that is, with input

signals that cause the appearance of dominant nonlinear effects. Large-signal measurements with single-tone and two-tone stimuli were used.

In single-tone operation, the transistor is first biased on fixed point of interest with DC-voltages V_{GS} and V_{DS} , and then a sinusoidal RF input signal is provided in the gate-source port, at a fundamental frequency (f_0). In the drain-source port, the resulting output power is measured, at the fundamental frequency and at the second and third harmonics ($2f_0$, and $3f_0$).

In measurements with single-tone stimulus, the input power level was swept, starting with values where the power gain was linear and gradually increasing towards gain compression up to the 1-dB, 2-dB or even 3-dB compression points. For every input power level, the output power levels at the fundamental tone and its harmonics enabled the calculation of values of drain efficiency η_D and power-added efficiency PAE .

In two-tone operation, the transistor was also biased with fixed DC-voltages V_{GS} and V_{DS} . Then, two sinusoidal RF input signals were used on different fundamental frequencies f_1 and f_2 . As mentioned in Chapter 1, the third-order intermodulation products IMD3, the power levels at $2f_1+f_2$ and $2f_2+f_1$ provide a measure of the device linearity.

3.3.2 Measurement Setups

For the large-signal characterization of the device with single-tone and two-tone stimuli for model verification, the setups were arranged and the corresponding measurements were performed by B. Wittwer and E.R. Srinidhi, co-workers of the author of this thesis in the Microwave Electronics Lab (Micel), former FG Hochfrequenztechnik (HFT), of the Kassel University.

Figure 3.27 and Figure 3.28, as published by Srinidhi *et al.* [71] and Wittwer *et al.* [72], illustrate the measurement setups used for single- and two-tone characterization, whose results were used in this thesis work for model verification.

The detail functionality of the setups and in-depth aspects of the related measurement techniques have been presented in publications by Srinidhi *et al.* [71] and Wittwer *et al.* [72].

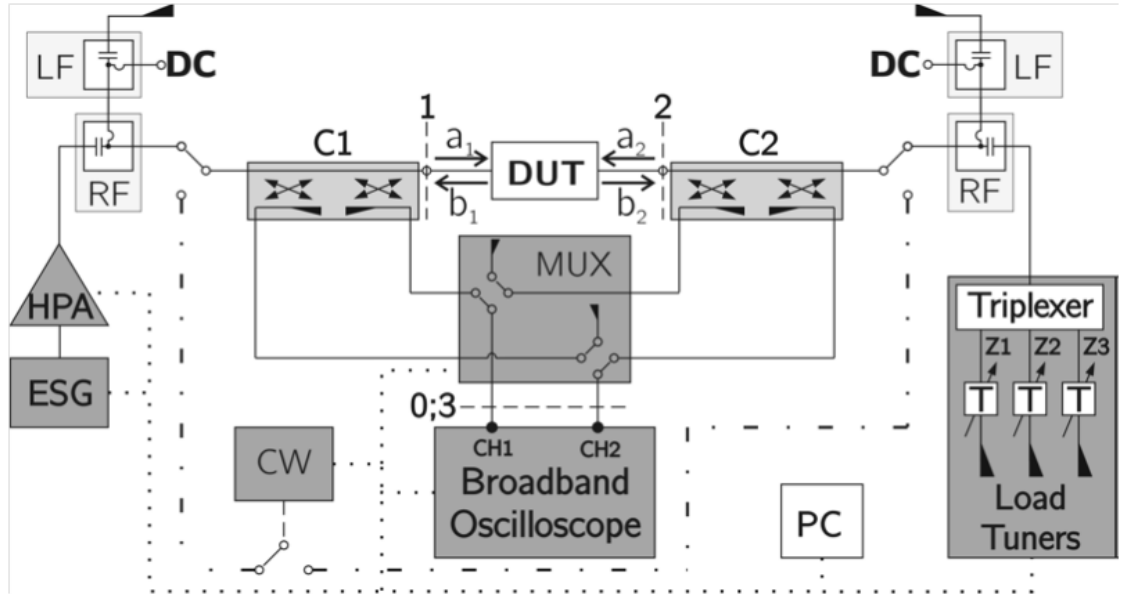


Figure 3.27 Large-signal multi-harmonic load-pull measurement setup proposed by Wittwer *et al.* [72] applied for the single-tone and two-tone device characterization used for model verification.

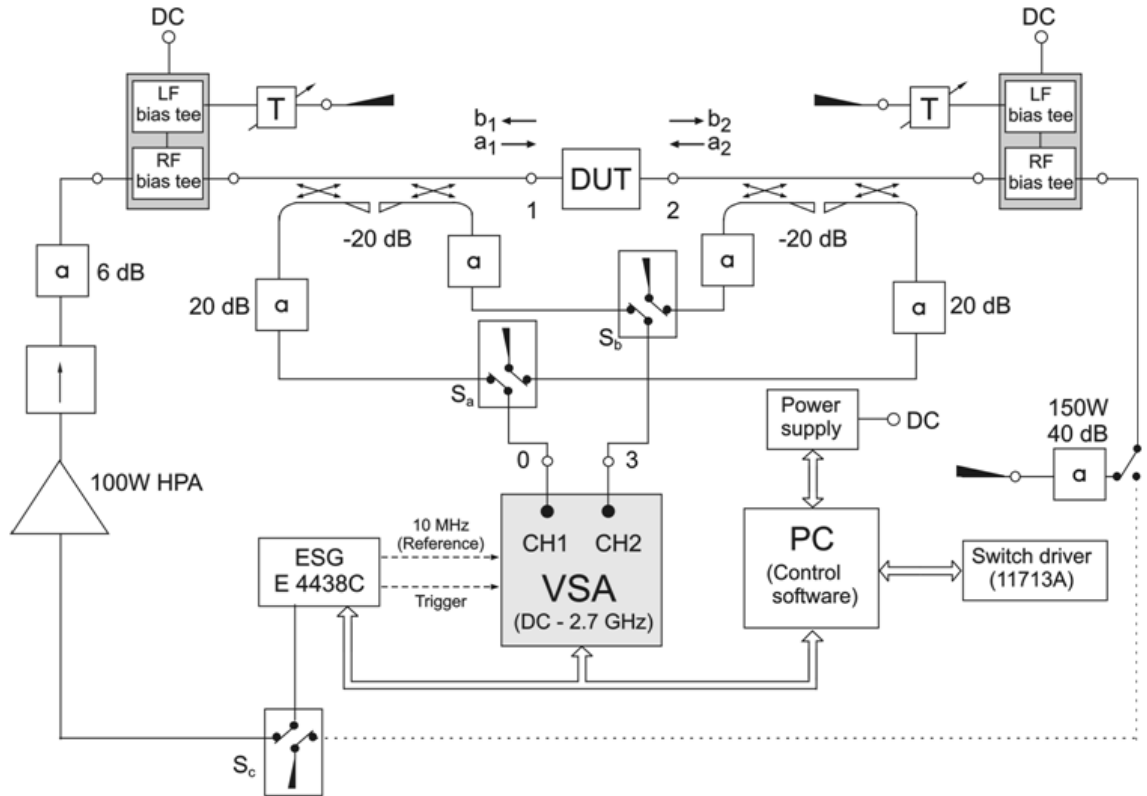


Figure 3.28 Large-signal frequency-domain measurement setup for distortion and envelope load-pull characterization proposed by Srinidhi *et al.* [71] applied for the two-tone device characterization used for model verification.

Chapter 4

Proposed Strategy for Small-Signal Modeling

In this thesis, the modeling strategy proposed is split in two stages, small and large-signal modeling. The developed models employ equivalent circuits and are measurement-based.

Parameters of the large-signal model related to the i_{DS} current are obtained from pulsed-DC IV measurements (as will be explained later in subchapter 6.2 of Chapter 6), but the small-signal parameters representing parasitic effects are employed too in the equivalent circuit of the large-signal model. Besides, intrinsic elements in the equivalent circuit of the large-signal model are calculated from elements of the small-signal equivalent circuit (as will be shown later in subchapter 6.4 of Chapter 6).

Thus, in this thesis, formulation and identification of the small-signal model are presented first, in the present chapter. The results of small-signal modeling are discussed in detail in the following Chapter 5.

Subchapter 4.1 introduces the equivalent circuit adopted for the small-signal model and discusses the physical meaning of the related model parameters (the circuit elements).

The calculation of parameters from measured data is commonly known as parameter extraction. Parameter extraction of the small-signal model was split in two parts: Extrinsic parameter extraction, treated in subchapter 4.2, and intrinsic parameter extraction, discussed in subchapter 4.3.

Subchapter 4.4 formulates the expected scalability of model parameters with respect to the number and unit width of the gate electrodes.

4.1 Small-Signal Electrical Equivalent Circuit

Most equivalent circuits for small-signal models of GaN devices use standard topologies inherited from models of GaAs FETs. In references [73-76], Jarndal and Kompa proposed the more comprehensive 22-element circuit shown in Figure 4.1. It features 12 extrinsic elements, in contrast

with the 9 extrinsic elements in standard equivalent circuits of GaAs FETs. In Figure 4.1, the intrinsic elements are enclosed in a dashed-line rectangle and the extrinsic elements are those that remain outside.

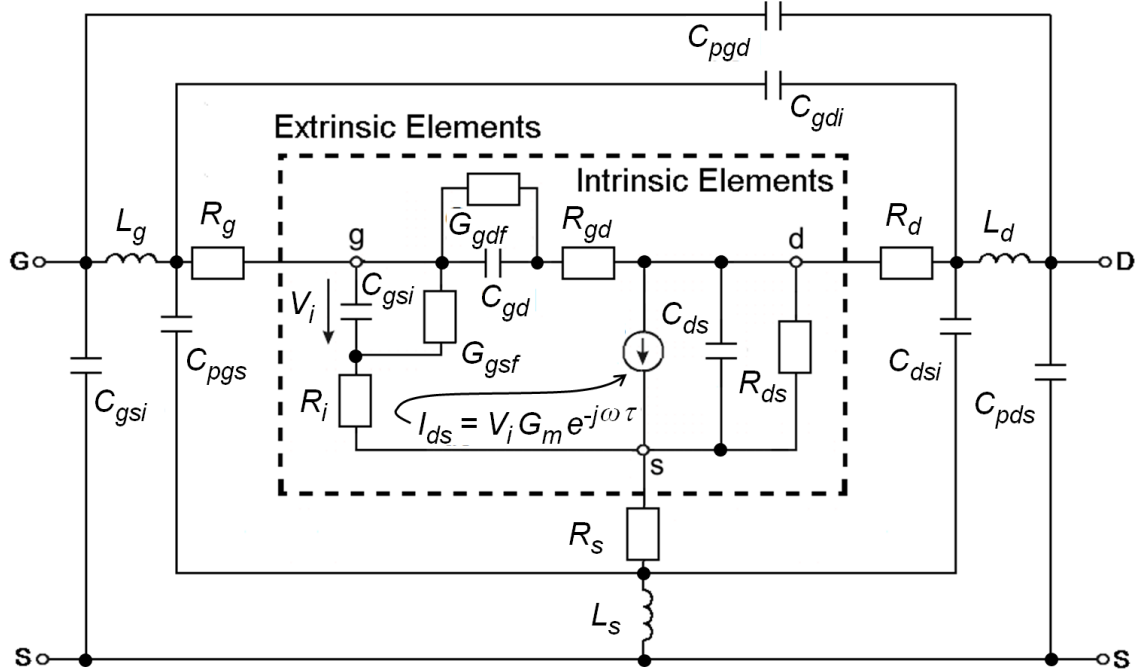


Figure 4.1 Small-signal electric equivalent circuit for GaN HEMTs used in this thesis.

The circuit of Figure 4.1 with its comprehensive extrinsic-element network is preferred over the standard circuit topologies with 9 extrinsic elements, e.g. [67, 77-81], because it represents better the parasitic effects expected in large-size GaN HEMTs, as described in the next sections 4.1.1 and 4.1.2. In consequence, circuit of Figure 4.1 is also more suitable to develop scalable models, as stated in [75].

The extrinsic parameters are related to parasitic effects and considered constant with respect to the frequency of the RF input signal and to the bias point. The intrinsic parameters are related to effects in the active layers and are generally considered dependent on the bias point but independent of the frequency of the RF input signal. The physical effects represented by the model parameters (circuit elements) are explained in sections 4.1.1 and 4.1.2, dedicating special attention in 4.1.2 to the comprehensive description of parasitic capacitive effects by the extrinsic capacitance parameters.

4.1.1 Physical Meaning of the Circuit Elements

The physical meanings of the elements in the electrical equivalent circuit of Figure 4.1 are expressed graphically with Figure 4.2 (except the

extrinsic capacitive effects, which are treated in the next section). The figure shows how the intrinsic elements are related to effects located in the active device layers, and how the extrinsic elements mainly represent effects located around the electrodes, electrode extensions and access regions from the electrodes to the active layers.

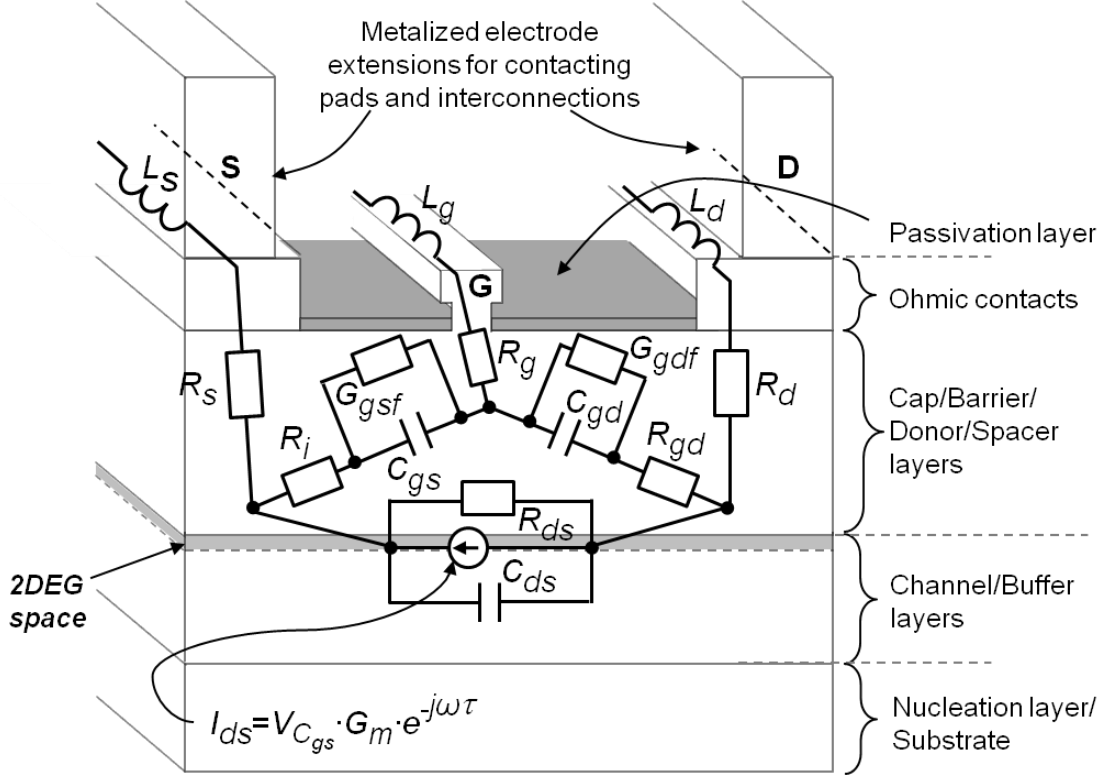


Figure 4.2 Illustration of the physical meaning of the electric equivalent circuit used for the small-signal model of GaN HEMTs (except extrinsic capacitive effects).

The parameters G_{gdf} and G_{gsf} denote conductances of the gate-drain and gate-source regions in the active layers related to effects of gate-current leakage, which are expected to appear when the diode-like effects of those regions are forward biased with $+V_{gd}$ and $+V_{gs}$. The intrinsic capacitance parameters C_{gs} and C_{gd} represent charge-storage effects in the gate-source and gate-drain regions between the gate electrode and the 2DEG.

The capacitive effects of C_{gs} and C_{gd} require finite times to set up, which are characterized by the time constants $R_i C_{gs}$ and $R_{gd} C_{gd}$. That is the physical origin of the intrinsic resistance parameters R_i and R_{gd} . In the adopted equivalent circuit, R_i and R_{gd} are cascaded to their corresponding capacitance and the conductance parameters, in contrast with other typical models that set them in series only with C_{gs} and C_{gd} , as presented in [80]. The position of R_i and R_{gd} the adopted circuit topology allows a direct consistency between the small-signal and large-signal equivalent circuits of

the intrinsic transistor. This will be demonstrated later in the large-signal model formulation regarding non-quasi-static effects of the gate charge, treated in subchapter 6.2.

The current flow in the 2DEG is described in the adopted small-signal equivalent circuit with the parameters I_{ds} and R_{ds} . The current source is controlled by the input voltage V_i (corresponding to the voltage across C_{gs}) and the current is proportional to the controlling voltage by a factor that is the device transconductance G_m . The current is delayed from the controlling voltage by the parameter τ that describes the propagation time of electrons in the 2DEG between the drain and source. The R_{ds} parameter (or its equivalent reciprocal $G_{ds} = 1/R_{ds}$) approximates the sheet resistance appearing around the 2DEG space, whereas C_{ds} describes the geometric capacitance related to this region.

The distributed inductive and resistive effects due to the electrodes behaving as transmission lines are represented by L_g , L_d and L_s , and R_g , R_d and R_s , for the gate, drain and source, respectively. The resistance parameters R_d and R_s also have components due to the ohmic contacts of the electrodes and due to the resistivity of the corresponding access regions between the contacts and the conduction channel.

4.1.2 Physical Meaning of the Extrinsic Capacitance Parameters

This section clarifies the physical meaning of the extrinsic capacitance parameters of the small-signal model: The “p” and “i”-subscripted capacitors of the circuit in Figure 4.1. These parameters are related with the electrodes and the metal layers of device. So first a short overview of the terminology is in order.

The metallic electrodes of the device, at the top of the semiconductor layer structure, are also known as fingers.

Besides, metalized extensions of the electrodes are laid out to form contacting surfaces, where the probe tips of measurement equipment or bonding wires can be placed for characterization or connection with other circuit elements.

The layout of these metalized electrode extensions is therefore known as finger layout.

Devices with more than two gate fingers use air bridges and bus bars. Air bridges are metallic overlays that connect contiguous fingers, as shown in Figure 4.3 (example photo from [82]). Bus bars connect the gate and drain contacting pads to the actual electrodes, as is also illustrated photographs of Figure 4.3.

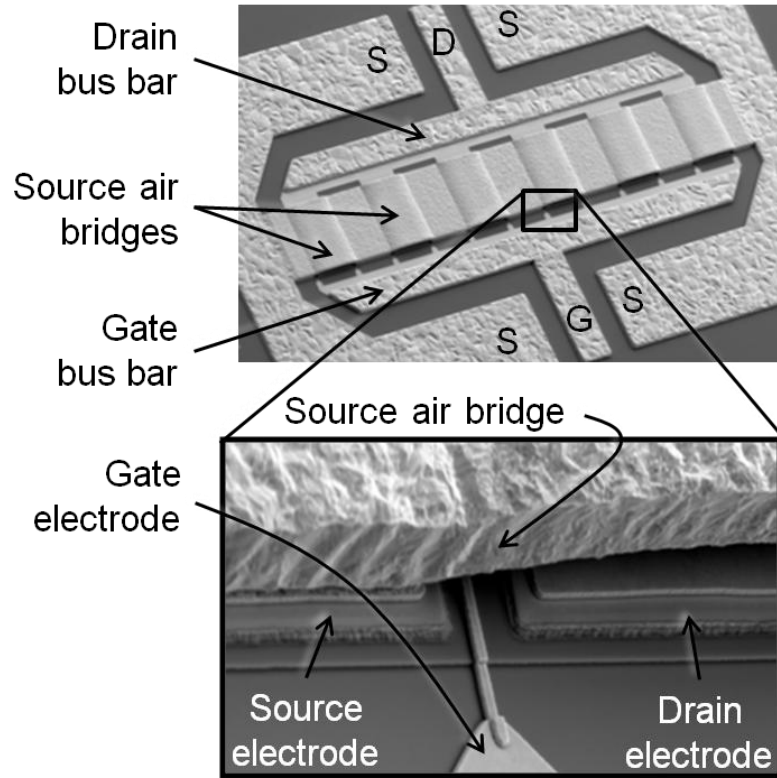


Figure 4.3 Photographs of a device shown in [82], highlighting air bridges and bus bars in transistor layouts with more than two gate electrodes (fingers).

The metalized extensions of the finger layout produce unwanted capacitive effects, which are accounted in the adopted model with the “p” and “i”-subscripted capacitors in the equivalent circuit of Figure 4.1. In this thesis work, approximated mathematical expressions for the charge storage effects related to these parameters are obtained using the well-known equation for the capacitance between two parallel metal plates: $C = \epsilon \cdot A / d$. The independent variables refer to the region where the considered charge storage effect occurs, ϵ is the dielectric constant, A the transversal area and d the distance between the metal surfaces.

- a) C_{pgs} represents the capacitance in the region from the contacting pad and bus bar of the gate to the metal under the substrate (ground plane), as illustrated in Figure 4.4 for a typical FET layout with two gate electrodes. C_{pgs} also accounts for capacitive effects due to the probe-tips. However, capacitive effects due to the probe-tips were considered

negligible in this thesis with respect to capacitive effects of contacting pads, bus bars and source air bridges. This consideration was supported by the high-quality air-coplanar probe-tips (model ACP40-GSG by Cascade Microtech[®]) employed for on-wafer characterization and also by the comparatively large area of contacting pads and bus bars with respect to the contact area of the probe-tips.

The approximated expression for C_{pgs} using $C = \epsilon \cdot A/d$ is

$$C_{pgs} \approx \epsilon_{lay} \cdot \frac{A_{p+bg}}{t_{lay}} \quad (4.1)$$

where ϵ_{lay} denotes the dielectric constant of the layer structure under the contacting pads and bus bars, and t_{lay} is the thickness of the same layer structure that represents the separation between the respective metal surfaces wherein the charge storage occurs.

In general A_{p+bg} represents the horizontal areas of the contacting pad and bus bar of the gate electrode. After inspection with the microscope, the horizontal area of the gate electrodes of the studied devices was considered negligible, and thus A_{p+bg} only represents the horizontal area of the contacting pad, as illustrated in Figure 4.4.

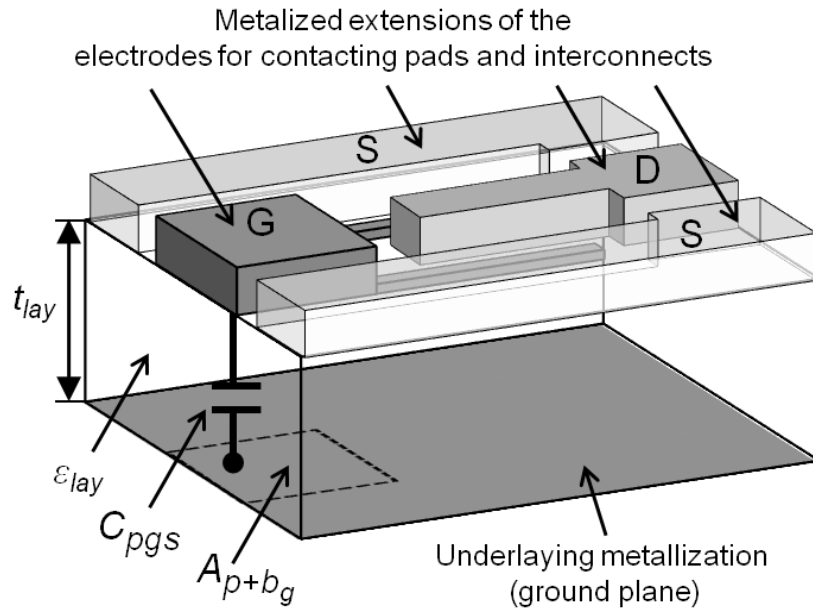


Figure 4.4 Illustration of the physical meaning of C_{pgs} .

- b) C_{pds} represents the capacitance between contacting pad and bus bar of the drain to the metal under the substrate (ground plane), as illustrated in Figure 4.5 for a typical FET layout with two gate electrodes. The approximated expression of C_{pds} using $C = \epsilon \cdot A/d$ is

$$C_{pds} \approx \epsilon_{lay} \cdot \frac{A_{p+b_d}}{t_{lay}}. \quad (4.2)$$

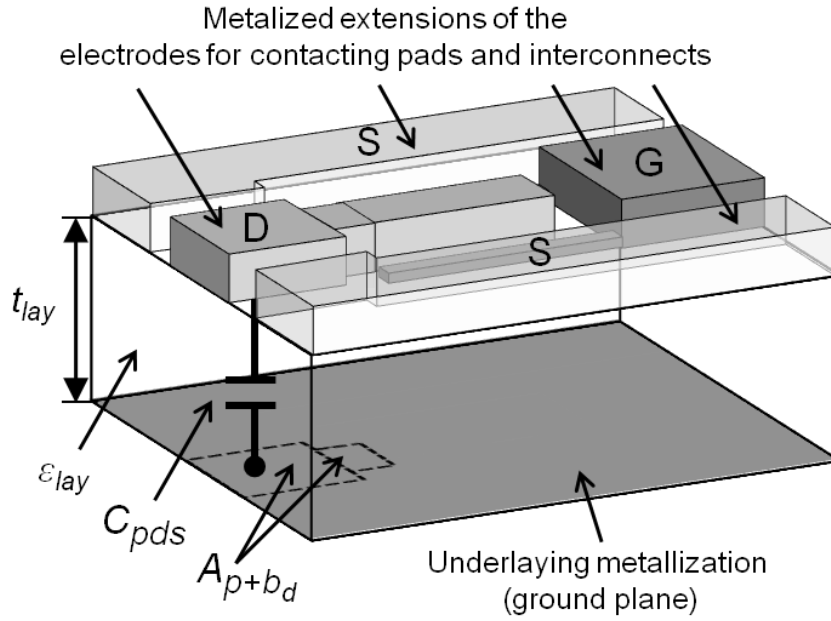


Figure 4.5 Illustration of the physical meaning of C_{pds} .

The terms ϵ_{lay} and t_{lay} have the same meaning as in the previous equation for C_{pgs} .

As illustrated in Figure 4.5, the metalized extension of the drain electrode is considered as composed by three segments, one for the contacting pad, the next for the bus bar and another for the length of the actual electrode. Then, A_{p+b_d} denotes an area with two components: (i) the horizontal area of the segment for the drain contacting pad and (ii) the horizontal for the drain bus bar.

If source air bridges exist, capacitance between them and the metal underneath them could be accounted as part of C_{pgs} or C_{pds} , with an extra summand in (4.1) or (4.2), depending on whether the bridges overpass over the drain or the gate electrodes.

- c) C_{pgd} represents the capacitive effect between the end of the drain electrode and the contacting pad (or the bus bar) of the gate, as it is illustrated in Figure 4.6. Then, the approximated expression for C_{pgd} using $C = \epsilon \cdot A/d$ is given by

$$C_{pgd} \approx n_{f_d} \cdot \epsilon_0 \cdot \frac{t_{bus_g} \cdot l_{f_d}}{d_{pgd}}. \quad (4.3)$$

The dielectric of the region of this effect is typically air. So $\epsilon_{air} = \epsilon_0$ has been considered in equation (4.3). The term d_{pgd} denotes the metal-to-metal distance in the region where this effect appears. The term t_{busg} represents the thickness of the contacting pad of the gate. The term l_{fd} stands for the length of the drain electrode. The factor n_{fd} is the number of drain electrodes and accounts for the repetition of the capacitive effect with each electrode.

A similar effect to C_{pgd} appears between the end of the gate electrodes and the contacting pad (or bus bar) of the drain, called here C_{pdg} and illustrated in Figure 4.6. C_{pdg} is usually negligible, but only under the following considerations:

- Thickness of the contacting pad or bus bar is significantly smaller for the gate than for the drain.
- Electrode length is noticeably smaller for the gate than for the drain.
- The metal-to-metal separation for C_{pdg} is notably larger than for C_{pgd} .

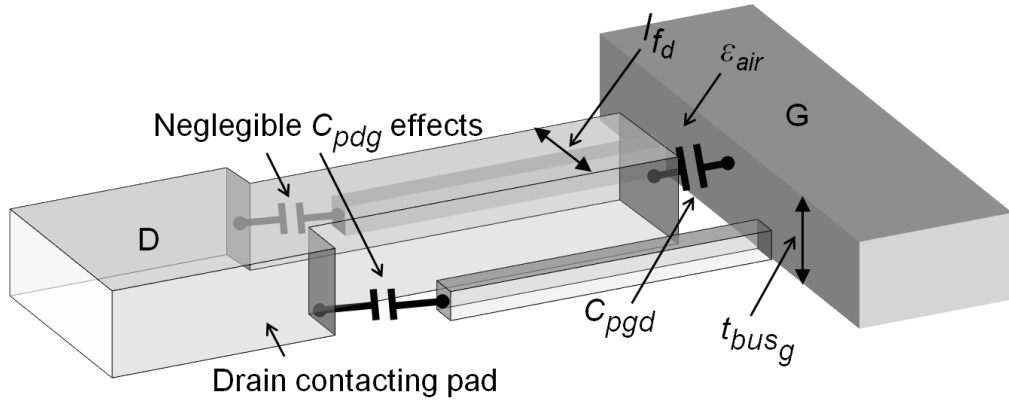


Figure 4.6 Illustration of the physical meaning of C_{pgd} .

- d) C_{gsi} represents the capacitive effect between the actual gate and source electrodes, as shown in Figure 4.7. The approximated expression for C_{gsi} using $C = \epsilon \cdot A/d$ is given by

$$C_{gsi} \approx n_{fg} \cdot \epsilon_{gsi} \cdot \frac{t_{fg} \cdot w_{fg}}{d_{gsi}}. \quad (4.4)$$

d_{gsi} is the distance between the lateral metal surfaces of contiguous gate and source electrodes and ϵ_{gsi} is the dielectric constant of that region. The terms t_{fg} and w_{fg} are dimensions related to such lateral metal surface of the gate electrode. The factor n_{fg} is the number of gate electrodes and accounts for the repetition of the capacitive effect for each electrode.

- e) C_{gdi} denotes the capacitive effect between the gate and drain electrodes, as depicted in Figure 4.7. The approximated expression for C_{gdi} is

$$C_{gdi} \approx n_{fg} \cdot \varepsilon_{gdi} \cdot \frac{t_{fg} \cdot w_{fg}}{d_{gdi}}. \quad (4.5)$$

d_{gdi} is the distance between the lateral metal surfaces of contiguous gate and drain electrodes and ε_{gdi} is the dielectric constant of that region. t_{fg} , n_{fg} and w_{fg} have the same meaning as in the equation for C_{gsi} .

- f) C_{dsi} represents the sum of two effects:

First, the capacitive effect between metalized extensions of the drain and source electrodes (at the layer of electroplated metal above the actual electrodes), as shown in Figure 4.7. This part of C_{dsi} is called here C_{dsi1} , and its approximated expression using $C = \varepsilon \cdot A/d$ is given by

$$C_{dsi1} \approx n_{fg} \cdot \varepsilon_0 \cdot \frac{t_{fd} \cdot w_{fg}}{d_{dsi}}. \quad (4.6)$$

The dielectric of the region related to this effect is usually air, so $\varepsilon_{air} = \varepsilon_0$ was considered in (4.6). The term d_{dsi} is the distance between metalized extensions of the drain and source electrodes. The terms t_{fg} , n_{fg} and w_{fg} have the same meaning than in the previous equation (4.4) for C_{gsi} .

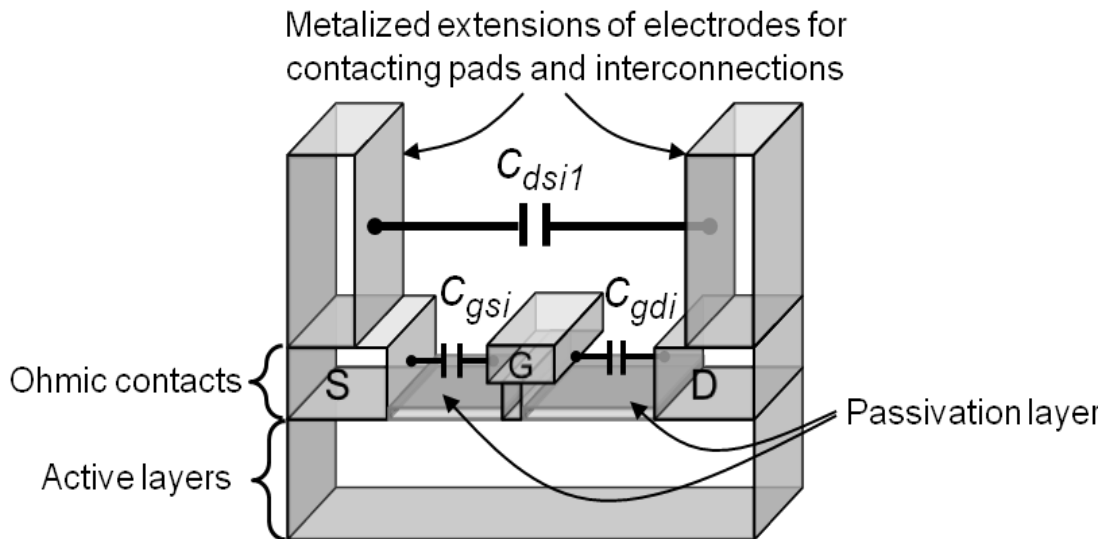


Figure 4.7 Illustration of the physical meaning of C_{gsi} , C_{gdi} and C_{dsi1} .

A second effect accounted by C_{dsi} , is the capacitive effect between the metalized extensions of the drain electrodes (the layer of electroplated metal that is above the actual electrode) and the metal under the

substrate (ground plane), as shown in Figure 4.8. This part of C_{dsi} is called here C_{dsi2} . An approximated expression for C_{dsi2} using $C = \epsilon \cdot A/d$ is given by

$$C_{dsi2} \approx n_{fd} \cdot \epsilon_{lay} \frac{A_{fd}}{t_{lay}} \quad (4.7)$$

where A_{fd} is the horizontal area of the drain electrode and n_{fd} is the number of drain electrodes, denoting the repetition of this effect for each electrode. The terms ϵ_{lay} and t_{lay} have the same meaning as in the previously shown equations (4.1) or (4.2), for C_{pgs} or C_{pds} .

As a result, an approximated expression for C_{dsi} is obtained summing up the equations (4.6) and (4.7), receiving the following expression,

$$C_{dsi} \approx n_{fg} \cdot \epsilon_0 \cdot \frac{t_{fd} \cdot w_{fg}}{d_{dsi}} + n_{fd} \cdot \epsilon_{lay} \cdot \frac{A_{fd}}{t_{lay}} \quad (4.8)$$

The number of gate fingers is generally twice the number of drain fingers, which means $n_{fg} = 2 \cdot n_{fd}$. Besides, the horizontal area A_{fd} is equal to the product of l_{fd} and w_{fd} . Moreover, the drain electrode width is typically the same as the gate electrode width, which means that w_{fd} and w_{fg} are equal. Therefore, equation (4.8) can be rearranged as follows:

$$C_{dsi} \approx n_{fg} \cdot \left(\frac{\epsilon_0 \cdot t_{fd}}{d_{dsi}} + \frac{1}{2} \cdot \frac{\epsilon_{lay} \cdot l_{fd}}{t_{lay}} \right) \cdot w_{fg} \quad (4.9)$$

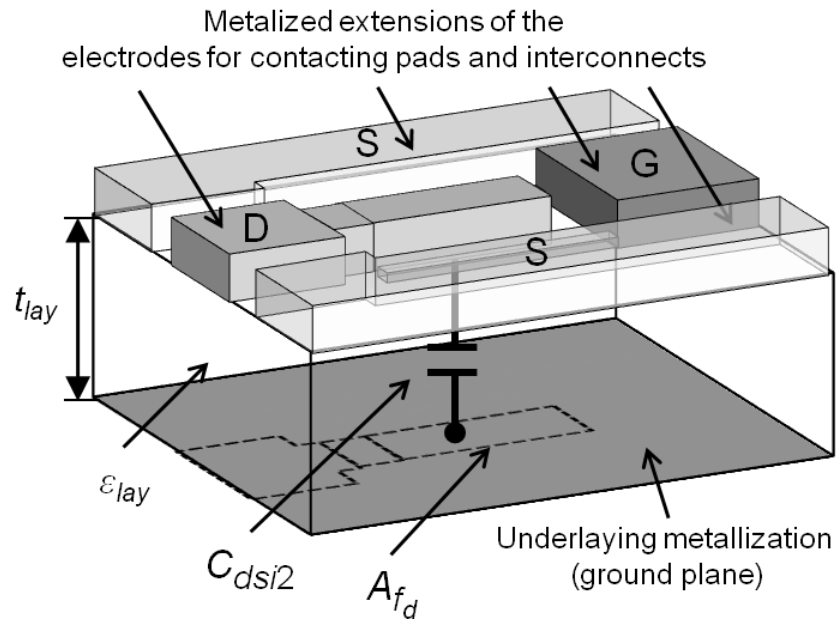


Figure 4.8 Illustration of the physical meaning of C_{dsi2} .

This section illustrated in detail the physical interpretation of the extrinsic capacitance parameters. At the same time, closed equations were given for the related capacitive effects in terms of features of the device finger layout. Those equations are exploited in subchapter 4.2 to analyze and generate adequate basic assumptions for extrinsic parameter extraction.

4.2 Extrinsic Parameter Extraction

References [74-76] proposed an algorithm of extrinsic parameter extraction for the adopted small-signal equivalent circuit, which featured technology-related empirical capacitance ratios (TECR). That algorithm represented the starting point to develop this thesis work and it will be called TECR algorithm further on in this text.

The TECR algorithm performed the extrinsic parameter extraction in an approach with two phases. The first and most important phase was a systematic search to find high-quality measurement-correlated starting values of the model parameters, as stated in [74]. The analytical parameter extraction performed in that phase was based on measured *cold pinch-off* and *cold forward* S-parameters.

In the second phase, the extracted values of extrinsic parameters were taken as starting point of a mathematical optimization process.

Figure 4.9, redrawn from [74], presents the flowchart of the systematic search to find high-quality measurement-correlated starting values of the model parameters. Figure 4.9 includes explanatory headlines of the key algorithm features besides sections of the present subchapter where the key features are discussed. Such guideline of the present subchapter is also stated in the following paragraphs.

The TECR algorithm featured assumed values of capacitance ratios, in an effort to calculate the extrinsic capacitance parameters of the model [74-76]. Those capacitance ratio values are a key aspect of the algorithm, and are analyzed in section 4.2.1.

Section 4.2.2 presents an improved generation of capacitance ratio values that pursues a parameter extraction that is more generally applicable and an increased reliability of the extracted values of extrinsic parameters.

The equation system that relates the measured *cold pinch-off* S-parameters with extrinsic capacitance parameters is set up in section 4.2.3.

Besides capacitance ratio values, sweeps of values on capacitance parameters are required to unequivocally solve the equation system set up in section 4.2.3. Such sweeps are proposed, discussed and exemplified in section 4.2.4. In the examples that will be presented, the proposed sweeps are applied with actual measured data of the studied large-size devices.

Section 4.2.5 presents the extraction of extrinsic resistance parameters based on a second measurement besides *cold pinch-off* S-parameters.

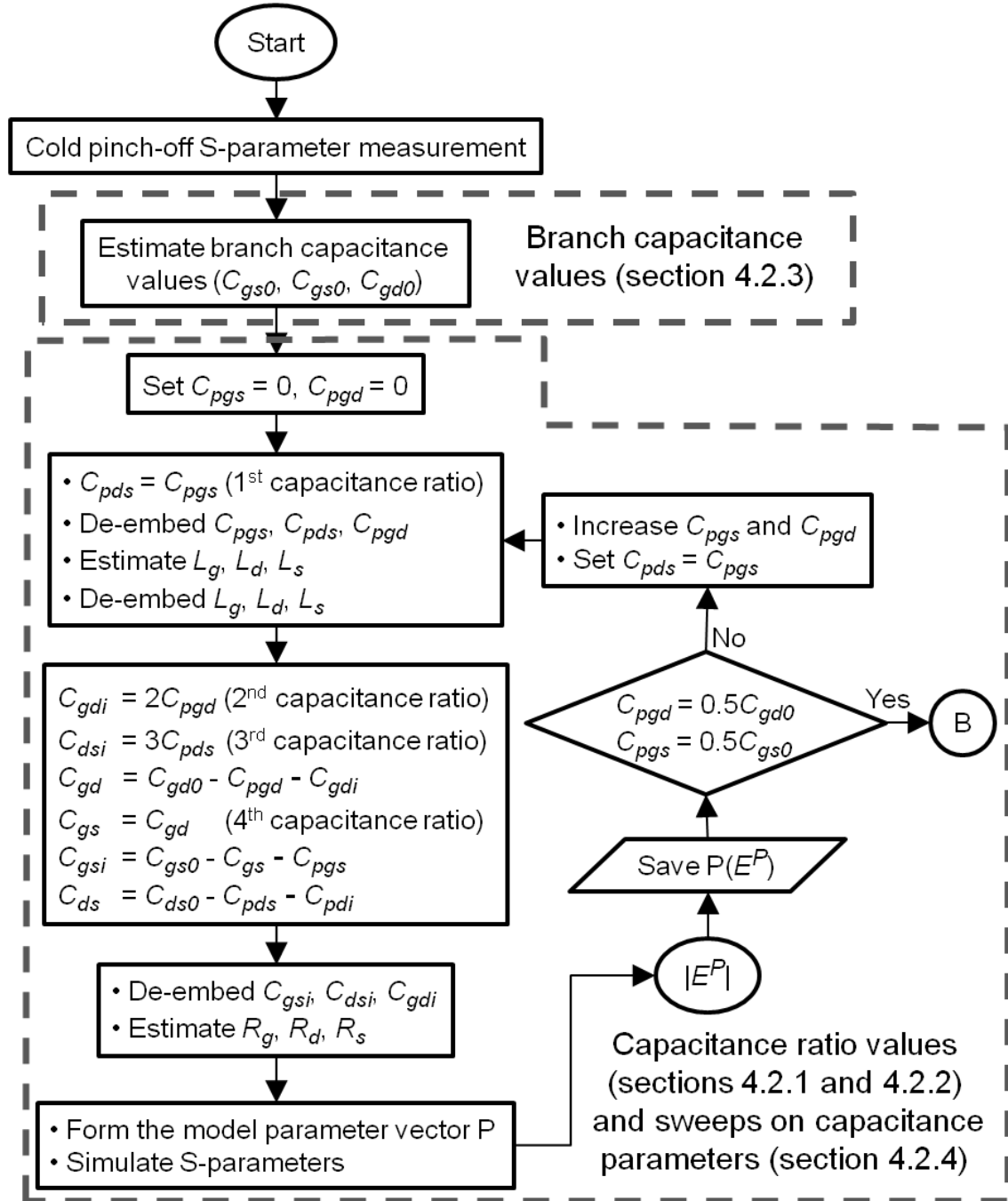


Figure 4.9 Flowchart of phase 1 of the TECR algorithm, redrawn from [74], indicating the sections of this thesis where each key aspect is treated (*continues*).

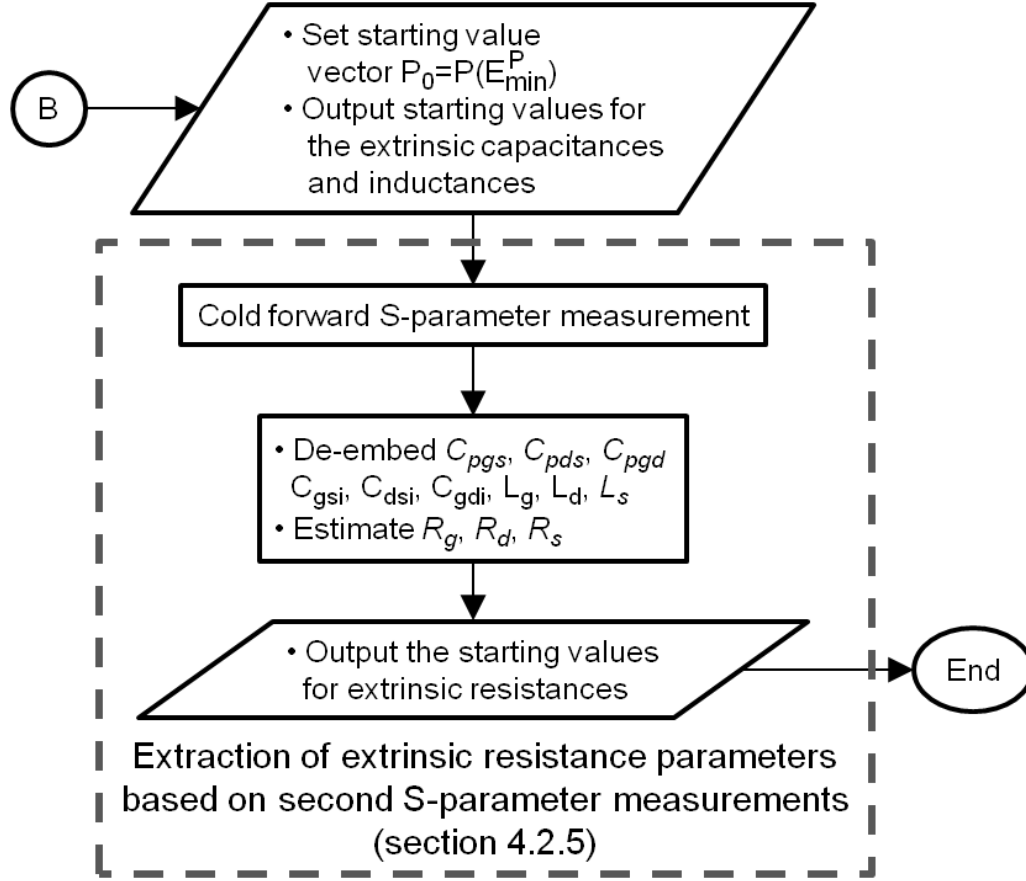


Figure 4.9 (continued).

4.2.1 Analysis of the Generation of Capacitance Ratio Values in the TECR Algorithm

The TECR algorithm proposed capacitance ratios values expressed by the next equations [74-76] (also indicated in the flowchart of Figure 4.9):

$$C_{pgs} \approx C_{pds}, \quad (4.10)$$

$$C_{gs} \approx C_{gd}, \quad (4.11)$$

$$C_{gdi} \approx 2 \cdot C_{pgd}, \quad (4.12)$$

$$C_{dsi} \approx 3 \cdot C_{pds}. \quad (4.13)$$

For the physical assumption behind (4.10) the TECR algorithm cited [83], where it was explained that $C_{pgs} \approx C_{pds}$ reflected similar gate and drain contacting pads of the devices studied in that work.

Quoting [75], the physical assumption behind (4.11) was that “*For symmetrical gate-source and gate-drain spacing, the depletion region will be uniform under pinch-off*”, and thus $C_{gs} \approx C_{gd}$.

In [75], the assumption behind (4.12) was that “*the gate-drain inter-electrode capacitance $[C_{gdi}]$ is twice the pad capacitance value $[2C_{pgd}]$* ”.

As for (4.13), reference [75] stated that: “ *$[C_{dsi}]$ is a significant part of the total drain-source capacitance. Therefore, the assumption $C_{dsi} \approx 3C_{pds}$ minimizes the error between simulated and measured S-parameters and reduces the risk of local minimum problems*”, for the device analyzed in that work.

Recently published works suggested that these capacitance ratio values are not general and that the parameter extraction could not be directly applied to different devices [67, 77]. Other works, like [84], reported diverse values of the same ratios and also used different capacitance ratios. Moreover, in [73] Jarndal stated that TECR algorithm “*required user intervention to assume suitable initial values for the inter-electrode capacitances*”, thus implying that setting suitable capacitance ratio values for different devices required the intervention of an experienced modeler.

The capacitance ratio values proposed by the TECR algorithm in [74] were analyzed in this thesis work. The analysis consisted of scanning values for the capacitance ratios C_{gs}/C_{gd} , C_{pgs}/C_{pds} , C_{gdi}/C_{pgd} and C_{dsi}/C_{pds} , to investigate the optimality of the values proposed in [74], from a heuristical (experience-based) perspective. For this analysis, the same measured data of the same AlGaIn/GaN HEMT was employed as in [74] (corresponding to a 0.1-mm device with two gate fingers and unit gate width of 50 μm).

The scanning was split in six tasks. In each task, two ratios were fixed in the values proposed in [74] (equations (4.10) to (4.13)) and the two other ratios were scanned from 0.01 to 100 (25 logarithmically-spaced steps).

Table 4.1 lists the combinations of fixed/scanned capacitance ratios (tasks) and the figure that contains the corresponding scanning results.

Table 4.1 Combinations of fixed/scanned ratios and figures with scanning results of the heuristical analysis made on the capacitance ratio values of the TECR algorithm.

Task	Fixed ratios	Scanned ratios	Scanning results reported in:
1	$C_{gs}/C_{gd} = 1$ and $C_{pgs}/C_{pds} = 1$	C_{gdi}/C_{pgd} and C_{dsi}/C_{pds}	Figure 4.10
2	$C_{gs}/C_{gd} = 1$ and $C_{gdi}/C_{pgd} = 2$	C_{dsi}/C_{pds} and C_{pgs}/C_{pds}	Figure 4.11
3	$C_{gdi}/C_{pgd} = 2$ and $C_{pgs}/C_{pds} = 1$	C_{gs}/C_{gd} and C_{dsi}/C_{pds}	Figure 4.12
4	$C_{gs}/C_{gd} = 1$ and $C_{dsi}/C_{pds} = 3$	C_{gdi}/C_{pgd} and C_{pgs}/C_{pds}	Figure 4.13
5	$C_{dsi}/C_{pds} = 3$ and $C_{pgs}/C_{pds} = 1$	C_{gs}/C_{gd} and C_{gdi}/C_{pgd}	Figure 4.14
6	$C_{gdi}/C_{pgd} = 2$ and $C_{dsi}/C_{pds} = 3$	C_{gs}/C_{gd} and C_{pgs}/C_{pds}	Figure 4.15

At each scanning step of each task, the four capacitance ratios had a value, e.g. in task 1: $C_{gs}/C_{gd} = 1$ (fixed), $C_{pgs}/C_{pds} = 1$ (fixed), $C_{gdi}/C_{pgd} = 0.1$ (first value of the 1st scan) and $C_{dsi}/C_{pds} = 0.1$ (first value of the 2nd scan). Then, the TECR algorithm was applied as in [74] (without optimization process), as described by the flowchart of Figure 4.9, but the capacitance ratio values of the scan step were used instead of those of [74]. As indicated by the flowchart, the results were values for all model parameters and an error function value denoted by E^P (the same error function was employed as defined in equation (33) of [74]).

In consequence, scanning results for each task were reported as follows: The related scanned ratios were mapped as X- and Y-axes of a 3D graph, and the error function value E^P corresponding to each scan step (each X-Y pair) was mapped as the Z-axis. In the surface of each task, a thick black dot is used to indicate the values proposed in [74] for the corresponding capacitance ratios.

The following indents (a) to (d) are key observations and conclusions obtained from the analysis of the figures with scanning results.

- (a) In the scanning results of the tasks 3, 5 and 6, where C_{gs}/C_{gd} was scanned (Figure 4.12, Figure 4.14 and Figure 4.15) there were recognizable valleys around the minimum error values, for C_{gs}/C_{gd} between 0.2 and 2. In all cases, that range contained the black dots of $C_{gs}/C_{gd} = 1$. Therefore, the presented analysis provided numerical support for this capacitance ratio value proposed in [74].

Regarding the physical meaning of $C_{gs}/C_{gd} = 1$, as mentioned before, it implies that the gate electrode of the device is located symmetrically between the source and the drain electrodes [74]. The centered location of the gate between source and drain is common in small FETs, for instance, in those modeled in [67, 74, 83]. However, for high-power applications, devices are often designed with larger gate-to-drain than gate-to-source extensions, so that $C_{gs}/C_{gd} > 1$. For example, in [84] a device was modeled with 0.7 μm between gate and source and 0.9 μm between gate a drain, and a corresponding C_{gs}/C_{gd} value of 1.3 ($\approx 0.9/0.7$) was proposed. Concerning the devices studied in this thesis work, photographs seem to indicate that the gate is located notably closer to the source than to the drain (although it was not possible to obtain reliable values of the gate-source and gate-drain distances).

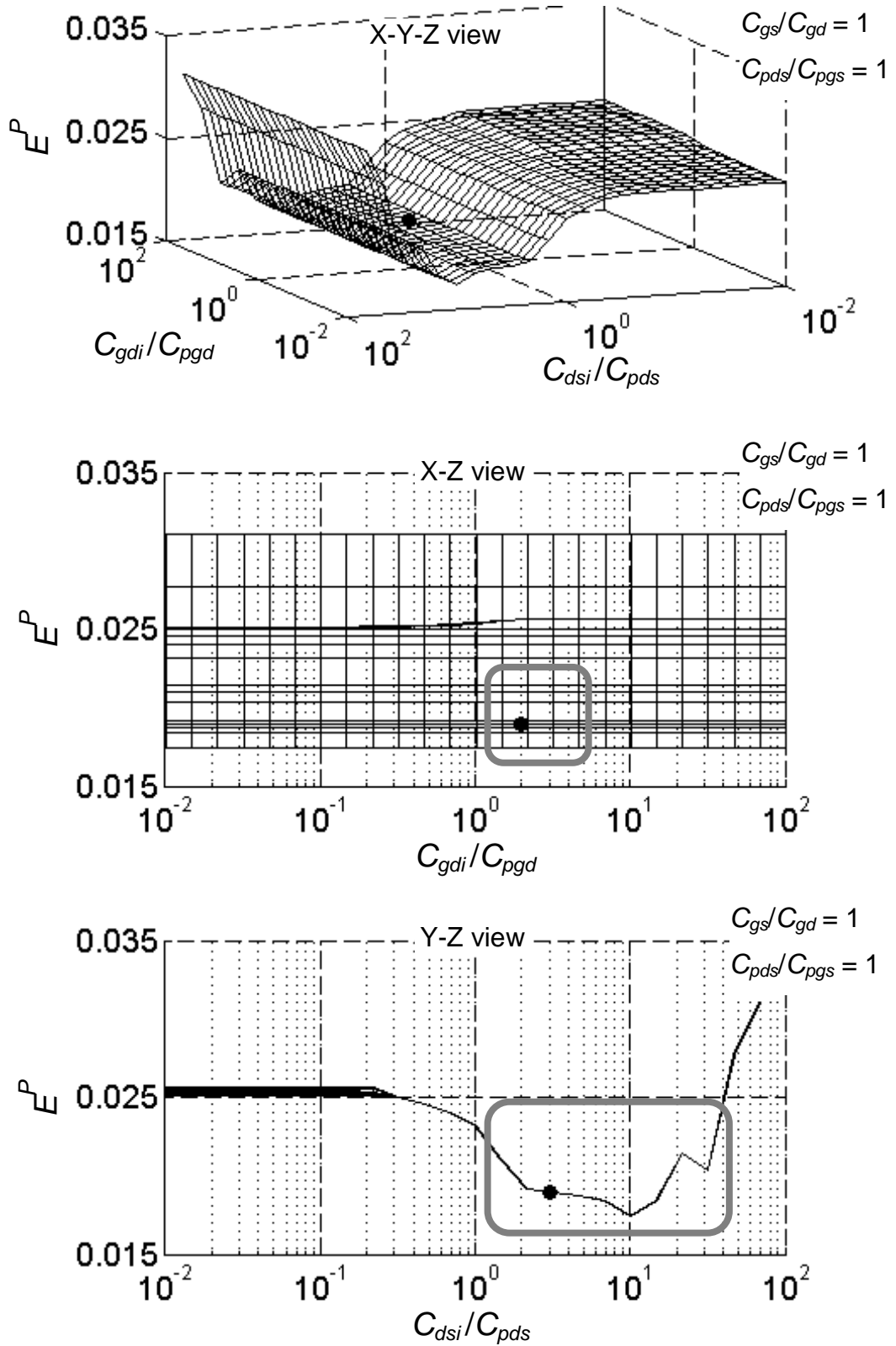


Figure 4.10 Scanning results of task 1 of the heuristical analysis made to capacitance ratio values of the TECR algorithm. C_{gs}/C_{gd} and C_{pds}/C_{pgs} are fixed in the values proposed in [74]. The scans on C_{gdi}/C_{pgd} and C_{dsi}/C_{pds} are mapped as the X- and Y-axes and the Z-axis corresponds to the E^P values obtained of applying the TECR algorithm with the capacitance ratio values of each scan step. The highlighted black dots indicate the C_{gdi}/C_{pgd} and C_{dsi}/C_{pds} values assumed in [74].

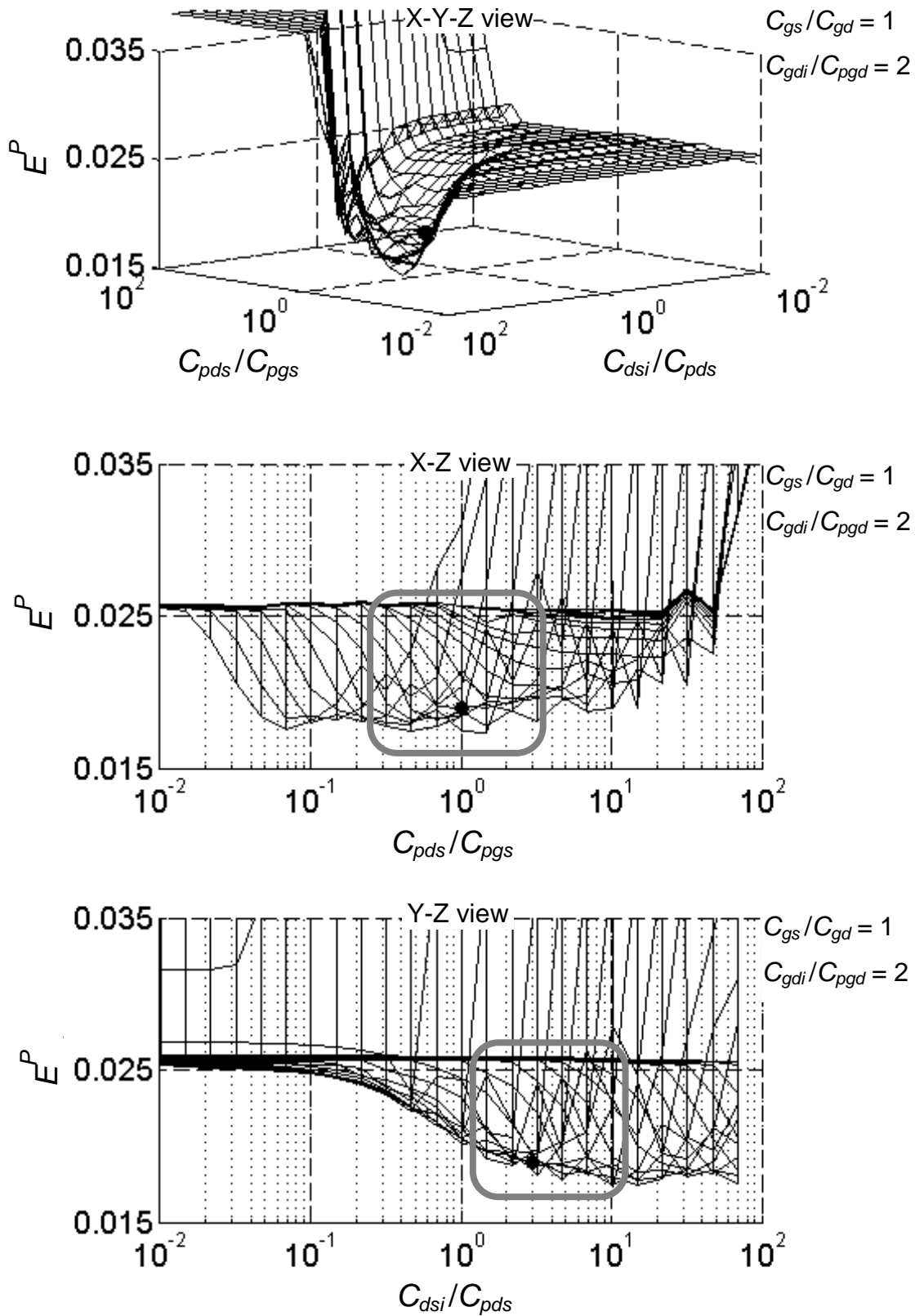


Figure 4.11 Scanning results of task 2 of the heuristical analysis made to capacitance ratio values of the TECR algorithm. C_{gs}/C_{gd} and C_{gdi}/C_{pgd} are fixed in the values proposed in [74]. The scans on C_{pds}/C_{pgs} and C_{dsi}/C_{pds} are mapped as the X- and Y-axes and the Z-axis corresponds to the E^p values obtained of applying the TECR algorithm with the capacitance ratio values of each scan step. The highlighted black dots indicate the C_{pds}/C_{pgs} and C_{dsi}/C_{pds} values assumed in [74].

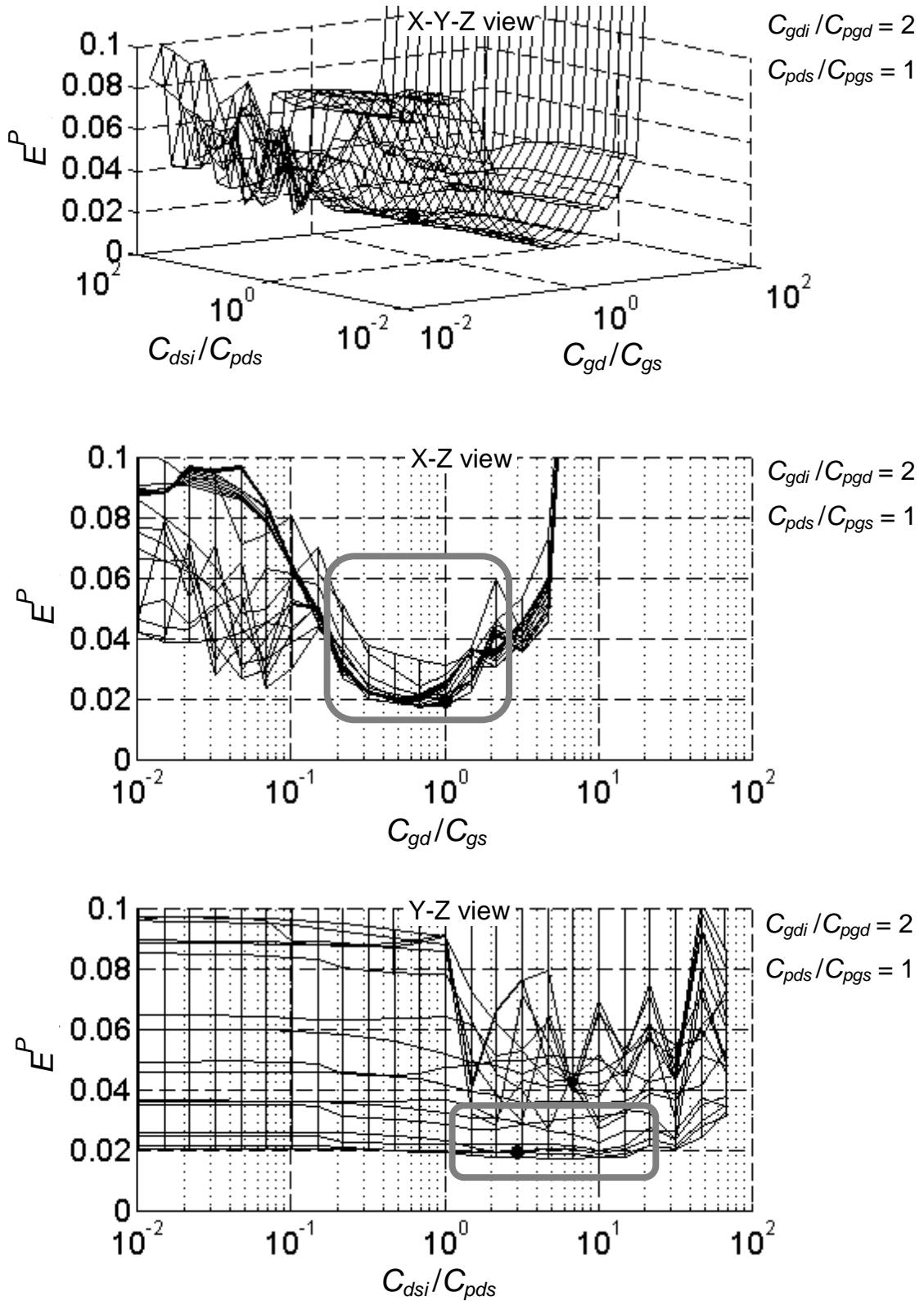


Figure 4.12 Scanning results of task 3 of the heuristical analysis made to capacitance ratio values of the TECR algorithm. C_{gdi}/C_{pgd} and C_{pds}/C_{pgs} are fixed in the values proposed in [74]. The scans on C_{gs}/C_{gd} and C_{dsi}/C_{pds} are mapped as the X- and Y-axes and the Z-axis corresponds to the E^P values obtained of applying the TECR algorithm with the capacitance ratio values of each scan step. The highlighted black dots indicate the C_{gdi}/C_{pgd} and C_{pds}/C_{pgs} values assumed in [74].

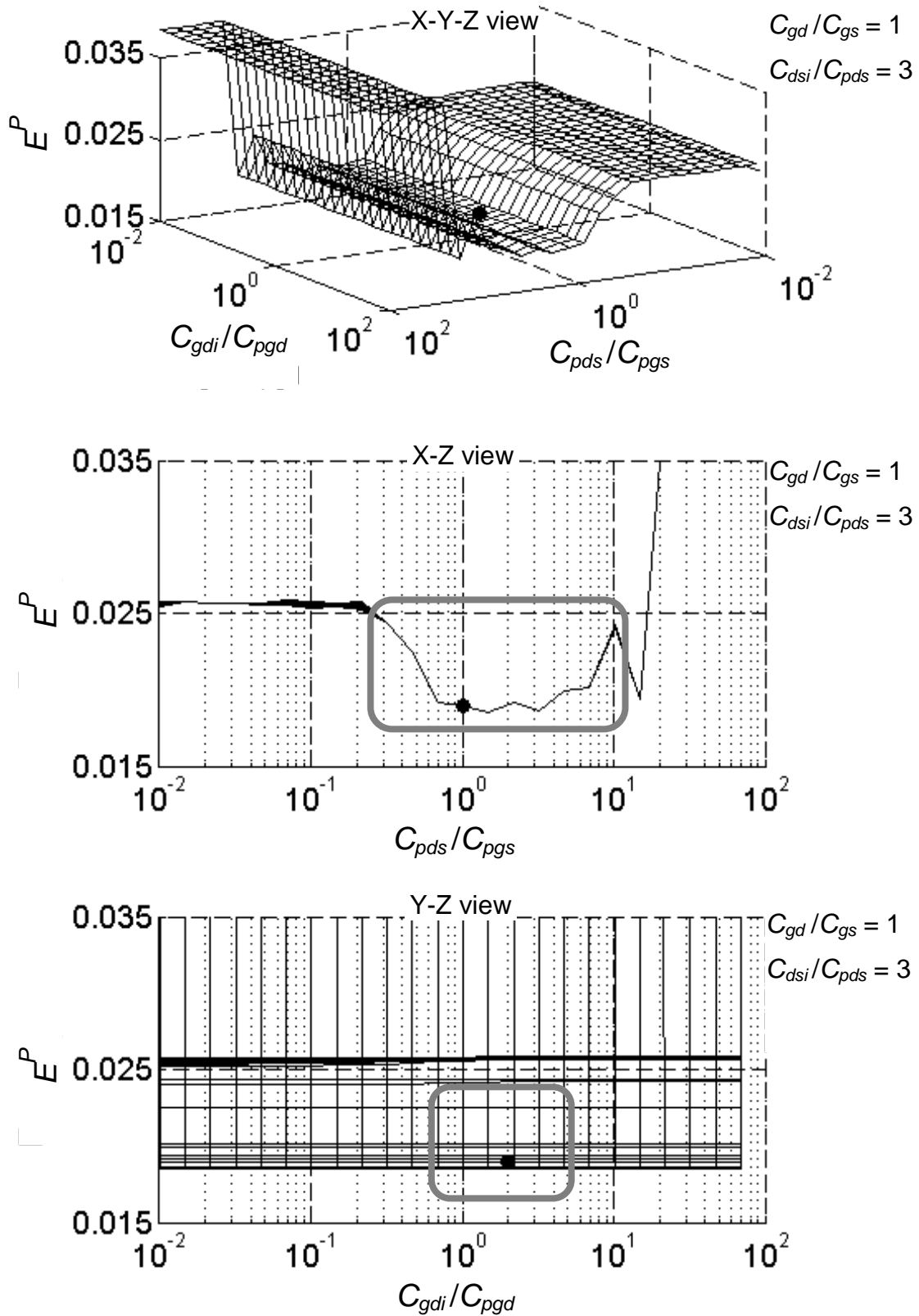


Figure 4.13 Scanning results of task 4 of the heuristical analysis made to capacitance ratio values of the TECR algorithm. C_{gs}/C_{gd} and C_{dsi}/C_{pds} are fixed in the values proposed in [74]. The scans on C_{pds}/C_{pgs} and C_{gdi}/C_{pgd} are mapped as the X- and Y-axes and the Z-axis corresponds to the E^P values obtained of applying the TECR algorithm with the capacitance ratio values of each scan step. The highlighted black dots indicate the C_{gs}/C_{gd} and C_{dsi}/C_{pds} values assumed in [74].

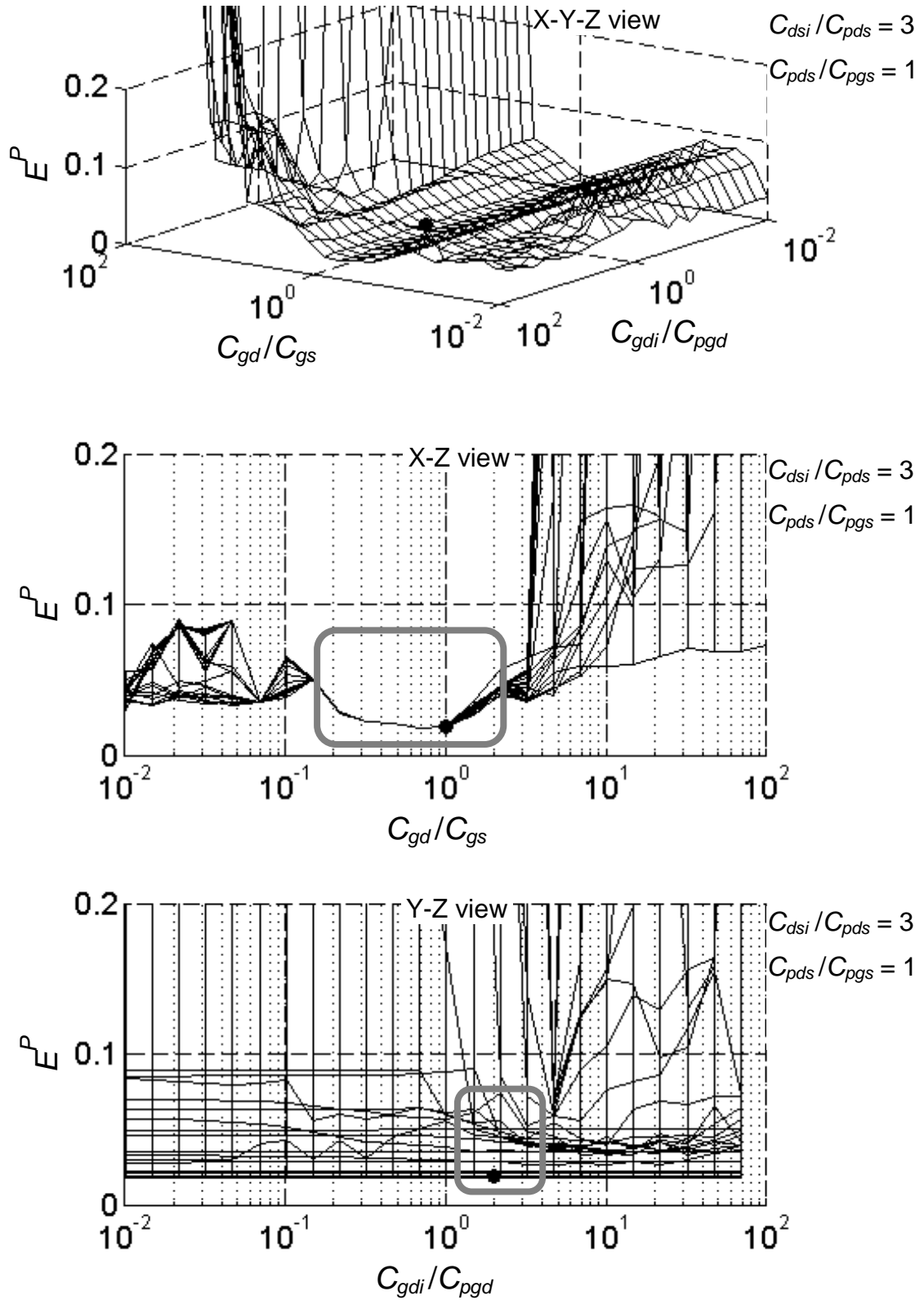


Figure 4.14 Scanning results of task 5 of the heuristical analysis made to capacitance ratio values of the TECR algorithm. C_{dsi}/C_{pds} and C_{pds}/C_{pgs} are fixed in the values proposed in [74]. The scans on C_{gs}/C_{gd} and C_{gdi}/C_{pgdi} are mapped as the X- and Y-axes and the Z-axis corresponds to the E^P values obtained of applying the TECR algorithm with the capacitance ratio values of each scan step. The highlighted black dots indicate the C_{dsi}/C_{pds} and C_{pds}/C_{pgs} values assumed in [74].

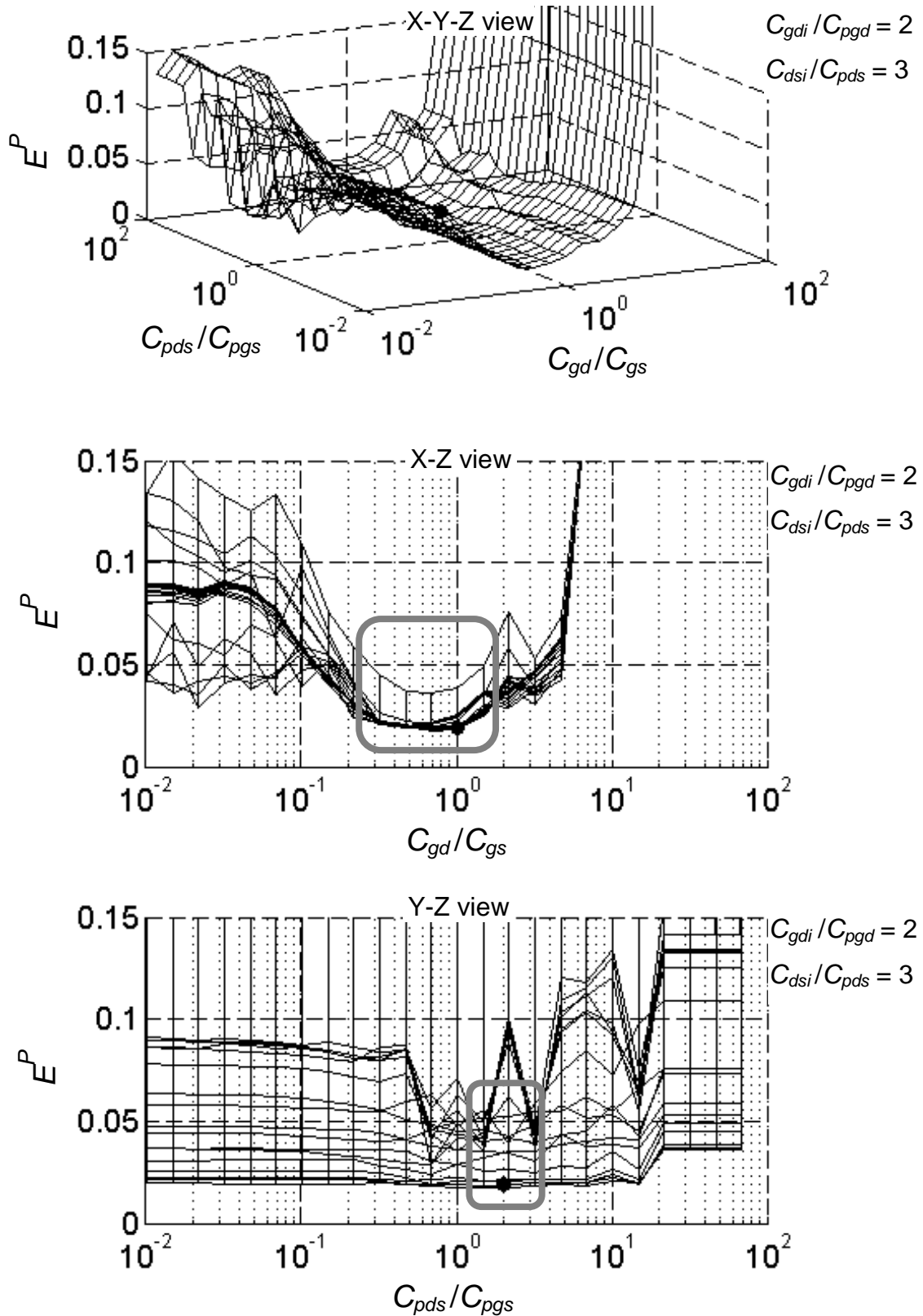


Figure 4.15 Scanning results of task 6 of the heuristical analysis made to capacitance ratio values of the TECR algorithm. C_{gdi}/C_{pgd} and C_{dsi}/C_{pds} are fixed in the values proposed in [74]. The scans on C_{gs}/C_{gd} and C_{pds}/C_{pgs} are mapped as the X- and Y-axes and the Z-axis corresponds to the E^p values obtained of applying the TECR algorithm with the capacitance ratio values of each scan step. The highlighted black dots indicate the C_{gdi}/C_{pgd} and C_{dsi}/C_{pds} values assumed in [74].

Moreover, different works documented that in modern GaN HEMTs C_{gd} and C_{gs} are influenced by charge-trapping effects and passivation layers [85-87] or by field-plate structures [40, 42, 88, 89]. For instance, in [85] two versions of the same 0.2-mm AlGaIn/GaN HEMT were studied, one version with a SiN passivation layer and another without it. Then, the reference states that for “*gate biases close to the pinch-off voltage, the C_{gs} values have obviously increased after passivation*”. The influence of field plates on C_{gd} and C_{gs} is illustrated in [89], which studied two versions of the same wide-bandgap device, one version with a source-connected field plate and another without it. Then, the reference states that “*The FP device has lower C_{gd} of 46.6 fF/mm in comparison with the value of 85.9 fF/mm for the non-FP device*”.

In consequence, charge-trapping effects, passivation layers and field-plate structures change the C_{gs}/C_{gd} values with respect to expectations based purely on the gate-drain and gate-source distances and their ratio. Even if with the gate centered between source and drain, assuming $C_{gs}/C_{gd} = 1$ without further technological data of the device provides only a rough approximation of this capacitance ratio value.

In conclusion, as already pointed out in [84], C_{gs}/C_{gd} must be carefully chosen with data of the device technology and construction. In anyway, it seems that $C_{gs}/C_{gd} = 1$ does not optimally match the situation of these capacitive effects appearing for high power GaN devices.

- (b) In the scanning results of tasks 1, 4 and 5, where C_{gdi}/C_{pgd} is scanned (Figure 4.10, Figure 4.13 and Figure 4.14), the error function values seem independent of this ratio. Then, $C_{gdi}/C_{pgd} = 2$ proposed by the TEQR algorithm in [74] cannot be contradicted or confirmed with the presented analysis.

Regarding the physical meaning of C_{gdi}/C_{pgd} in modern GaN HEMTs, recall the physical interpretation of C_{pgd} and C_{gdi} given in section 4.1.2, and their approximated expressions (4.3) and (4.5). Using those expressions the following equation for C_{gdi}/C_{pgd} is received,

$$\frac{C_{gdi}}{C_{pgd}} \approx \frac{n_{fg} \cdot \epsilon_{gdi} \cdot \frac{t_{fg} \cdot w_{fg}}{d_{gdi}}}{n_{fd} \cdot \epsilon_0 \cdot \frac{t_{busg} \cdot l_{fd}}{d_{pgd}}} \quad (4.14)$$

On another hand, field plates of modern GaN HEMTs change the distance between lateral metal surfaces of contiguous electrodes with respect to field-plate-free devices. For example, in gate-connected or dual field plates, the metal of the field plate alters the distance related to the term d_{gdi} of the equation (4.14), thus changing the capacitive effect denoted by C_{gdi} , and also the value of the ratio C_{gdi}/C_{pgd} with respect to any value assumed *a priori*, without taking into account the field-plate structures and their influence.

In conclusion, if it is suspected or known that the device has dual or gate-connected field plates, then, it is not possible to obtain a good first approximation of values for capacitance ratios that include C_{gdi} , such as C_{gdi}/C_{pgd} , without detailed data of the device technology.

In cases of field-plate-free devices, this thesis considers assumed values of C_{gdi}/C_{pgd} as physically sound if they are in accordance with the evaluation of (4.14).

- (c) In the scanning results of tasks 1, 2 and 3, where C_{dsi}/C_{pds} is scanned (Figure 4.10, Figure 4.11 and Figure 4.12), recognizable valleys exist around the minimum error value, for ratio values between 1 and 100. Then, the empirical motivation of [75] for $C_{dsi}/C_{pds} = 3$ is confirmed analyzing these sweeps, because the black dot falls around the minimum.

Concerning the physical meaning of C_{dsi}/C_{pds} in modern GaN HEMTs, keep in mind the physical interpretations of C_{dsi} and C_{pds} given in section 4.1.2, and their approximated expressions (4.2) and (4.9). Using those equations C_{dsi}/C_{pds} is received as

$$\frac{C_{dsi}}{C_{pds}} \approx \frac{n_{fg} \cdot \left(\frac{\epsilon_0 \cdot t_{fd}}{d_{dsi}} + \frac{1}{2} \cdot \frac{\epsilon_{lay} \cdot l_{fd}}{t_{lay}} \right) \cdot w_{fg}}{\epsilon_{lay} \cdot \frac{A_{p+bd}}{t_{lay}}} \quad (4.15)$$

Observe that the first summand between the parentheses in the denominator of this equation is due to C_{dsi1} and the second to C_{dsi2} . The approximated expressions corresponding to these two components of C_{dsi} were given in section 4.1.2, by equations (4.6) and (4.7).

On another hand, devices with more than two gate electrodes generally employ air bridges that can cause extra capacitive effects to be denoted

by C_{pds} , by an extra summand in the denominator of (4.15). This situation is exemplified by the device shown in Figure 4.3, where source air bridges pass above the drain electrode. Furthermore, dual, double or source-connected field plates of modern GaN HEMTs change the effective distance between the metalized electrode extensions of drain and source. In consequence, the metal of the field plates can notably decrease the distance actually related to the term d_{dsi} of (4.15), thus changing the capacitive effect denoted by C_{dsi1} and C_{dsi2} , and also the value of the ratio C_{dsi}/C_{pds} with respect to any value assumed *a priori*, without taking into account the field-plate structures and their influence.

In conclusion, if there are air bridges that cause significant capacitive effects between source and drain, then assuming values of capacitance ratios involving C_{pds} is not advisable. Neither is it advisable to assume values of capacitance ratios with C_{dsi} (or C_{dsi1}) if field plates are suspected or known. When none of these is the case, this thesis considers assumed values of C_{dsi}/C_{pds} as physically sound if they are in accordance with the evaluation of (4.15).

- (d) In the scanning results of tasks 2, 4 and 6, where C_{pds}/C_{pgs} is scanned (Figure 4.11, Figure 4.13 and Figure 4.15), regions with low error function values are clearly recognizable. Such regions present two or more points that possess similar error function values: $C_{pds}/C_{pgs} = 0.7$, 4 and 1 for Figure 4.11, $C_{pds}/C_{pgs} = 1.5$ and 3 for Figure 4.13, and the range of C_{pds}/C_{pgs} from 0.5 to 5 for Figure 4.15. Despite this apparent multiplicity, the black dot always falls near a point that could be taken as the minimum, which empirically confirms, with the analysis of the presented sweeps, the value of $C_{pds}/C_{pgs} = 1$ assumed within the TECR algorithm in [74].

Now regarding the physical meaning of C_{pds}/C_{pgs} in modern GaN HEMTs, recall the physical interpretations of C_{pgs} and C_{pds} given in section 4.1.2, and their approximated expressions (4.1) and (4.2). Using those equations, C_{pds}/C_{pgs} is received as

$$\frac{C_{pgs}}{C_{pds}} \approx \frac{A_{p+bg}}{A_{p+bd}} \quad (4.16)$$

On another hand, devices with more than two gate electrodes have air bridges that can cause capacitive effects and modify this equation.

In conclusion, if there are air bridges that cause significant capacitive effects, assuming values of capacitance ratios involving C_{pds} or C_{pgs} is not advisable. In other cases, this thesis considers assumed values of C_{pds}/C_{pgs} as physically sound if they are in accordance with the evaluation of (4.16).

The following Figure 4.16 is similar to the set from Figure 4.10 to Figure 4.15, but the error function values are taken after the optimization phase of the TECR algorithm. The regions near the minimum values have the same locations; it mainly shows differences on the overall values of the error function and on the smoothness of the surfaces.

As Figure 4.16 mainly serves as confirmation of the set from Figure 4.10 to Figure 4.15, thus it is presented in the following two pages, in a more condensed manner than the set.

The difficulty to generalize or adjust the capacitance ratios values proposed in [74-76] to each device of interest undermined the generality of application of the corresponding parameter extraction.

In consequence, the next section 4.2.2 discusses a new approach to generate capacitance ratio values.

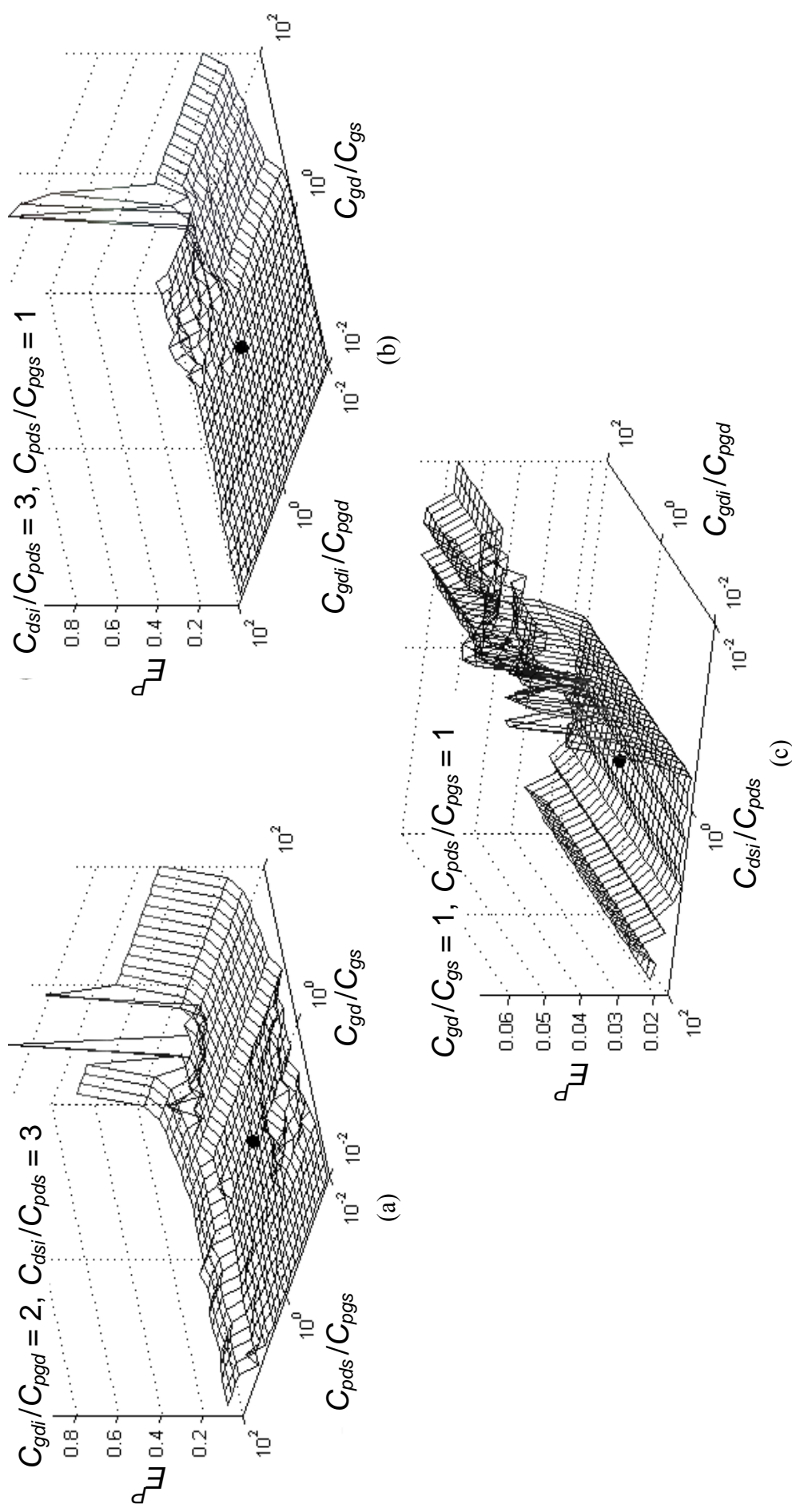


Figure 4.16 Sweeps of values on the capacitance ratios proposed by the TEQR algorithm: (a) C_{dsi}/C_{pds} and C_{gdi}/C_{pgd} , (b) C_{dsi}/C_{pds} and C_{pds}/C_{pgs} , (c) C_{dsi}/C_{pds} and C_{gs}/C_{gd} , (d) C_{gdi}/C_{pgd} and C_{pds}/C_{pgd} , (e) C_{gdi}/C_{pgd} and C_{gs}/C_{gd} , (f) C_{gdi}/C_{pgd} and C_{gs}/C_{gt} . Black dots mark values assumed in [74] (continues in the following page).

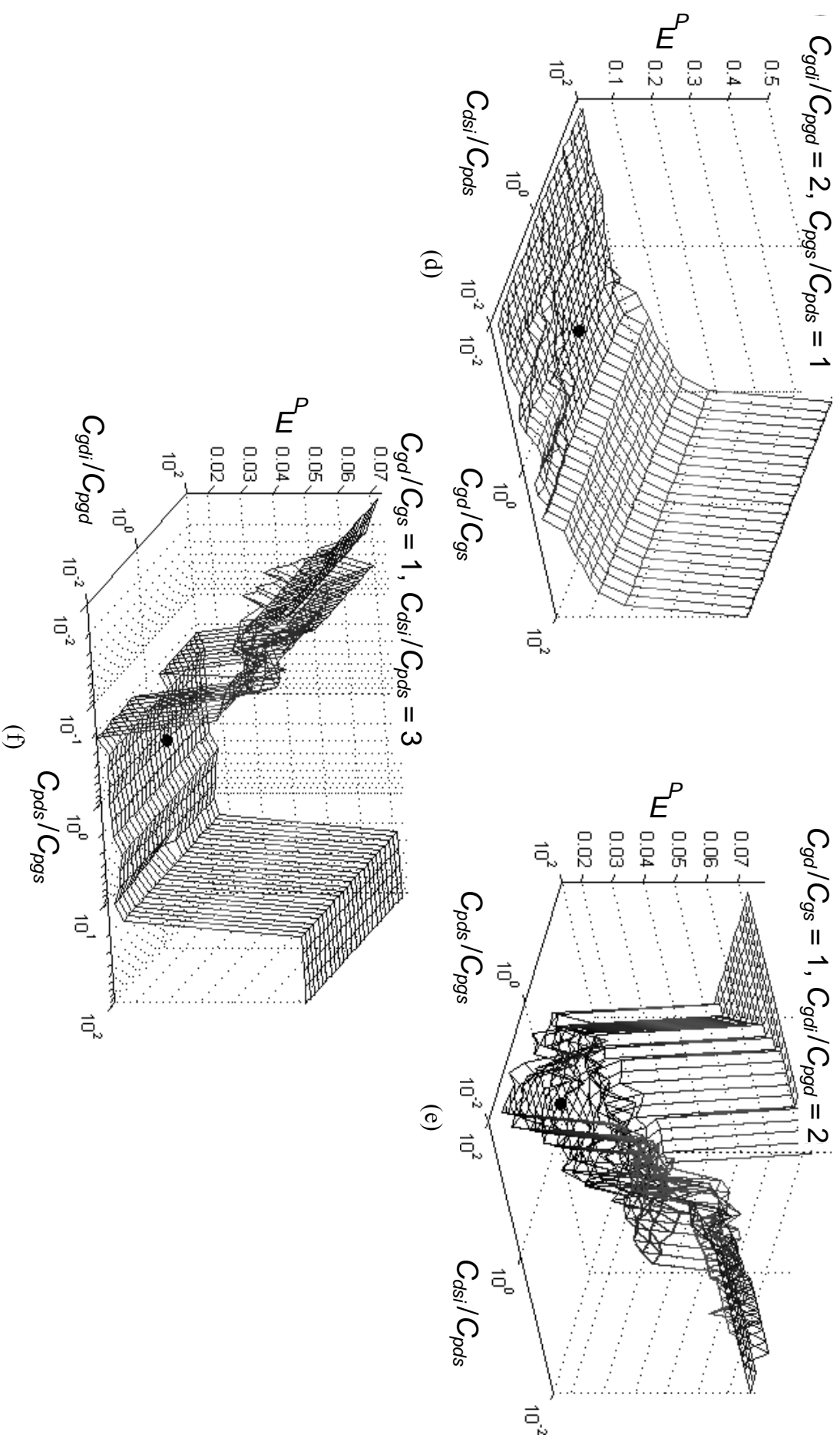


Figure 4.16 (continued).

4.2.2 Proposed Generation of Capacitance Ratio Values

An essential idea introduced by Jarndal and Kompa in [74] was setting up capacitance ratio values to solve the extrinsic parameter extraction of the 22-element model based on *cold*-FET S-parameter measurements.

This thesis also proposes to exploit that key idea. For that, this section proposes an approach to generate capacitance ratio values with the goal of establishing the required ratios with the highest generality of application and in the clearest way possible.

In this thesis work the model parameter extraction pursuit to employ as database only electrical measurements and data achievable within facilities of microwave device characterization or available in datasheets of commercial devices. In-depth data of the fabrication process (exact values of material properties and thickness of the layers, actual finger layout dimensions, etc.) must not be necessary. The goal was a parameter extraction with the highest generality of application possible.

According to equation (4.16) presented in the previous section 4.2.1 (in the paragraphs under the incise (d)), the value of C_{pgs}/C_{pds} is expressed by the ratio of two horizontal areas, A_{p+b_g}/A_{p+b_d} . These are the top-view areas related to the contacting pads and bus bars of the gate and of the drain electrodes, respectively. Such a ratio of areas is readily estimated with top-view or aerial images of the device finger layout, like the examples images presented in Figure 4.17 and Figure 4.18.

The photographs shown in Figure 4.17 were taken for this thesis with a generic commercial digital camera⁵ placed without zoom in front of the microscope eyepiece of the on-wafer probing station⁶. Similar images are also found in datasheets of commercial devices, like those shown in the following Figure 4.18.

A_{p+b_d}/A_{f_d} is another ratio of horizontal areas that can be obtained from images like those contained in Figure 4.17. Using the approximated expressions for C_{pds} and C_{dsi2} , given by equations (4.2) and (4.7) of section 4.1.2, the ratio C_{pds}/C_{dsi2} is related to A_{p+b_d}/A_{f_d} as follows:

⁵ Model IXUS 100 IS by Cannon®, with 12 megapixels, optical zoom of 4x and electrical zoom of 3x.

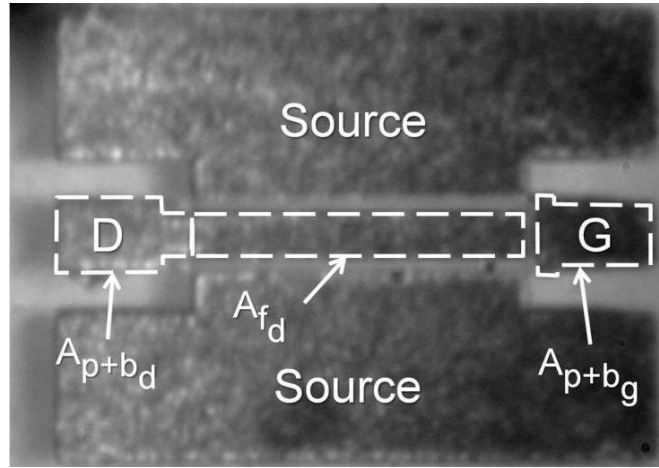
⁶ Probing station specified in the first paragraphs of Chapter 3 with a built-in microscope by Bausch & Lomb®. The eyepiece has fixed-magnification of 20x and variable zooming system of 1x to 7x.

$$\frac{C_{pds}}{C_{dsi2}} \approx \frac{A_{p+bd}}{n_{fd} \cdot A_{fd}}. \quad (4.17)$$

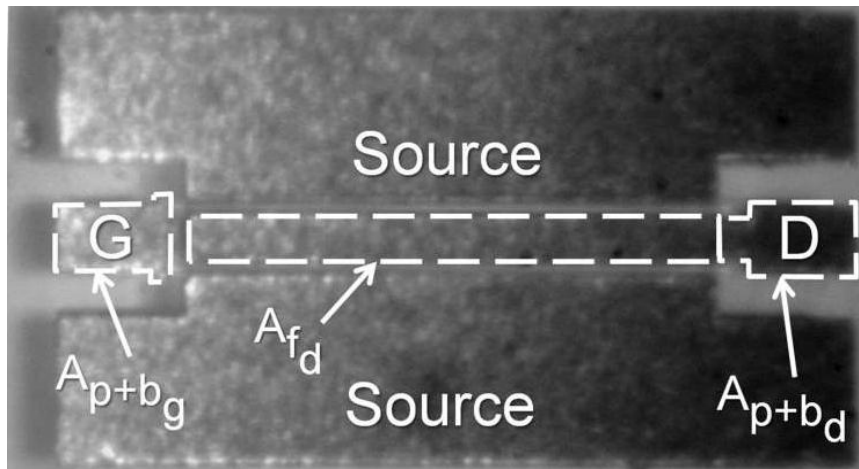
Figure 4.17 confirms the absence of air bridges. It is essential to note this, since it was a necessary condition given in section 4.2.1 to assume reliable values of C_{pgs}/C_{pds} . This condition applies for C_{pds}/C_{dsi2} as well.

As an opposed example, observe the photographs of Figure 4.19, where source air bridges of the finger layouts are highlighted. Using those images to evaluate C_{pgs}/C_{pds} was considered unreliable, because the influence on C_{pgs} from capacitive effects produced by the source air bridges cannot be estimated, and therefore, equation (4.16) for C_{pgs}/C_{pds} cannot be used.

C_{pds} is unrelated to the source air bridges highlighted in the photographs of Figure 4.19, thus A_{p+bd}/A_{fd} and C_{pds}/C_{dsi2} are reliably evaluated with those top-view images.

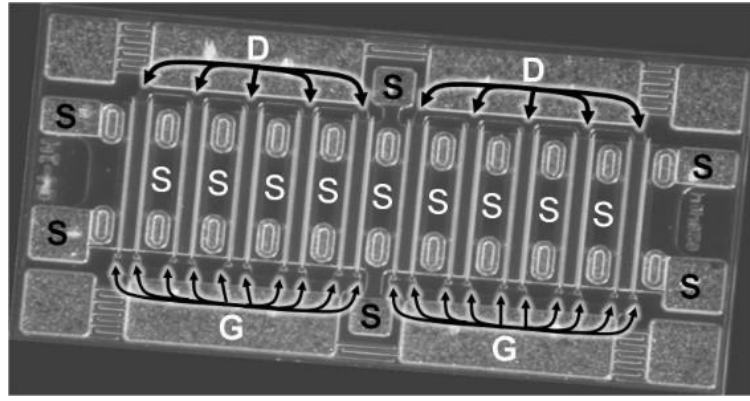


(a)

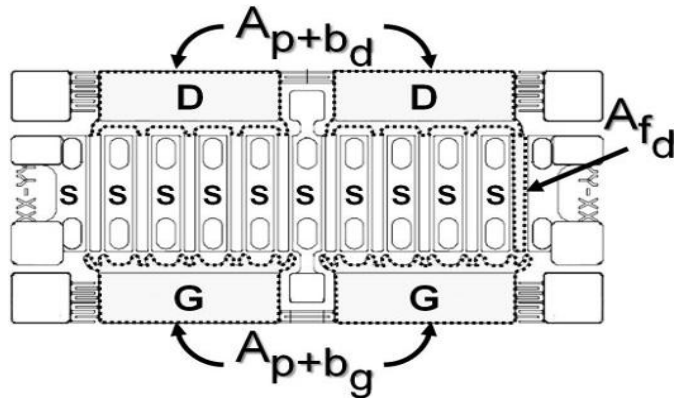


(b)

Figure 4.17 Example top-view photographs taken for this thesis useful to evaluate A_{p+bg}/A_{p+bd} and A_{p+bd}/A_{fd} , thus C_{pgs}/C_{pds} and C_{pds}/C_{dsi2} . They are of IAF devices with two gate fingers and with gate peripheries of (a) 0.5 mm and (b) 0.8 mm.



(a)



(b)

Figure 4.18 Example top-view images that can be found in datasheets of a commercial GaN HEMT, (a) photograph and (b) technical drawing, which would be useful to evaluate C_{pgs}/C_{pds} and C_{pds}/C_{dsi2} [62].

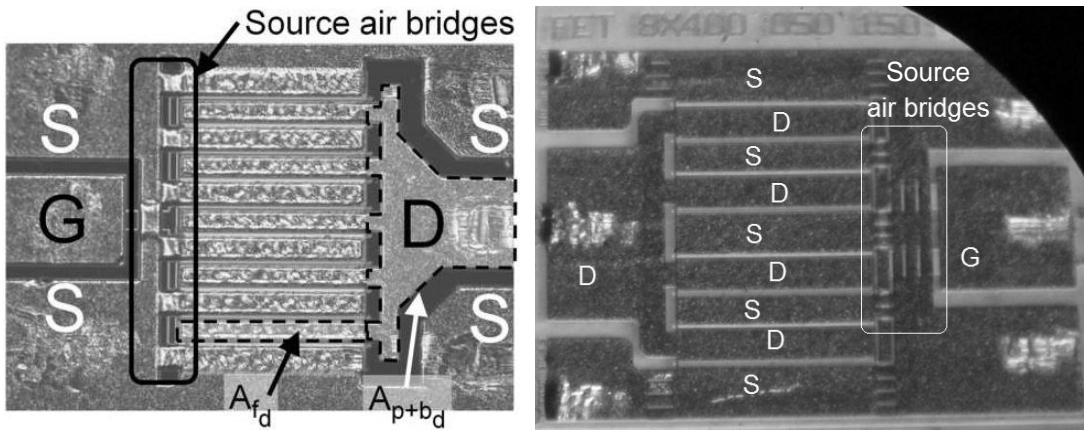


Figure 4.19 Example top-view photographs taken for this thesis, which are not useful to evaluate C_{pgs}/C_{pds} due to the source air bridges. They are of (left) the 2-mm Nitronex[®] device and of (right) the 3.2-mm IAF device

The photographs shown in Figure 4.19 were obtained in the same way described for those in Figure 4.17.

It is possible to employ further top-view images to obtain additional useful ratios, observe the photographs of Figure 4.20.

The ratios w_{fg}/l_{fd} and d_{pgd}/d_{dsi} are estimated from these images, which were taken similarly to those of Figure 4.17, applying additionally the zooming factor of the commercial camera and a tripod for stability. The usefulness of w_{fg}/l_{fd} and d_{pgd}/d_{dsi} is explained as follows. Recall the approximated expressions for C_{pgd} and C_{dsil} , given by equations (4.3) and (4.6), their combination in form of ratio results in the following equation:

$$\frac{C_{dsil}}{C_{pgd}} \approx \frac{n_{fg} \cdot \epsilon_0 \cdot \frac{t_{fd} \cdot w_{fg}}{d_{dsi}}}{n_{fd} \cdot \epsilon_0 \cdot \frac{t_{bus_g} \cdot l_{fd}}{d_{pgd}}} \quad (4.18)$$

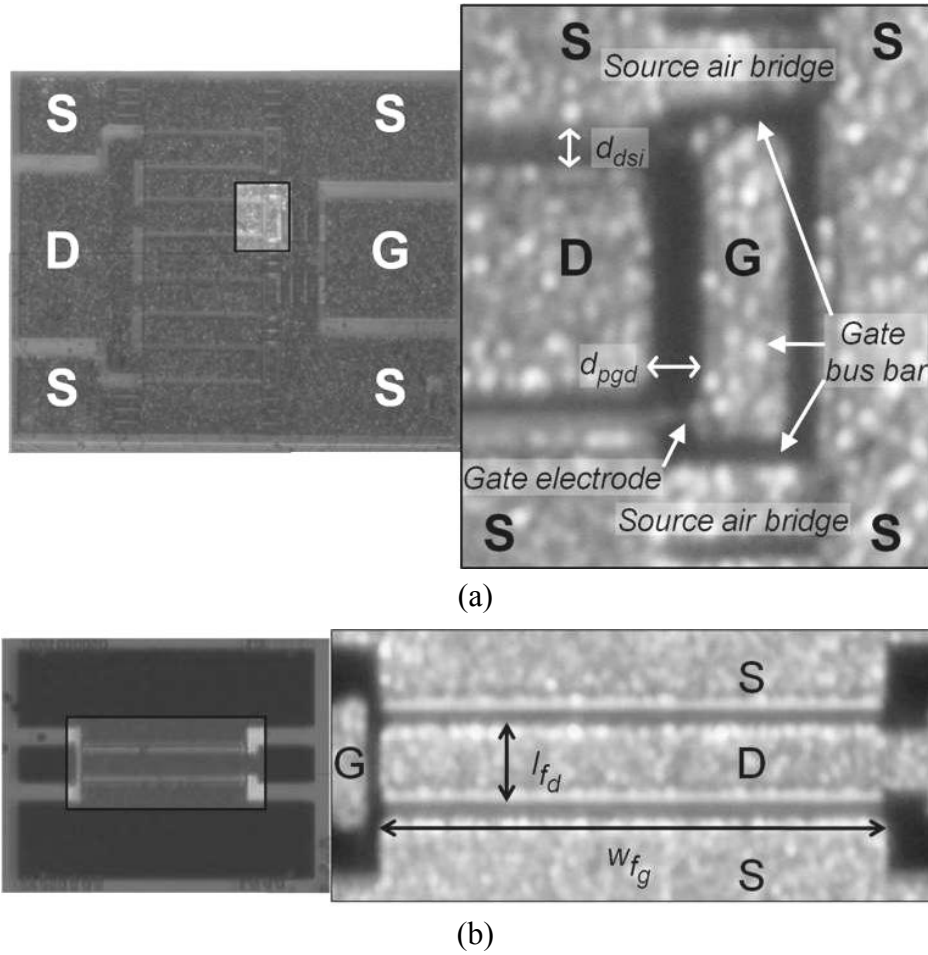


Figure 4.20 Example top-view photographs taken for this thesis using a commercial camera with zooming factor applied, which are useful to evaluate C_{dsil}/C_{pgd} . They are of IAF devices with unit gate width of 0.25 mm and: (a) 8 gate fingers, (b) 2 gate fingers.

For finger layouts like those shown in Figure 4.17 and Figure 4.19, equation (4.18) reduces itself to the following expression, considering that the condition $t_{fd} \approx t_{bus_g}$ stands,

$$\frac{C_{dsil}}{C_{pgd}} \approx \frac{n_{fg}}{n_{fd}} \cdot \frac{w_{fg}}{l_{fd}} \cdot \frac{d_{pgd}}{d_{dsi}} \quad (4.19)$$

Thus, the ratios d_{pgd}/d_{dsi} and w_{fg}/l_{fd} are useful to evaluate C_{dsil}/C_{pgd} of GaN HEMTs without field plates. n_{fg}/n_{fd} is equal to two, because layouts typically have twice as many electrodes for the drain than for the gate. Noting the absence of field plates is vital, because it is a necessary condition given in section 4.2.1 to assume reliable values involving C_{dsil} .

A higher zooming factor was obtained using another microscope⁷ that captures images known as micrographs. Figure 4.21 shows top-view micrographs of two devices, this type of images allow the estimation of the ratio of distances d_{gdi}/d_{gsi} , which are illustrated in part (a) of that figure.

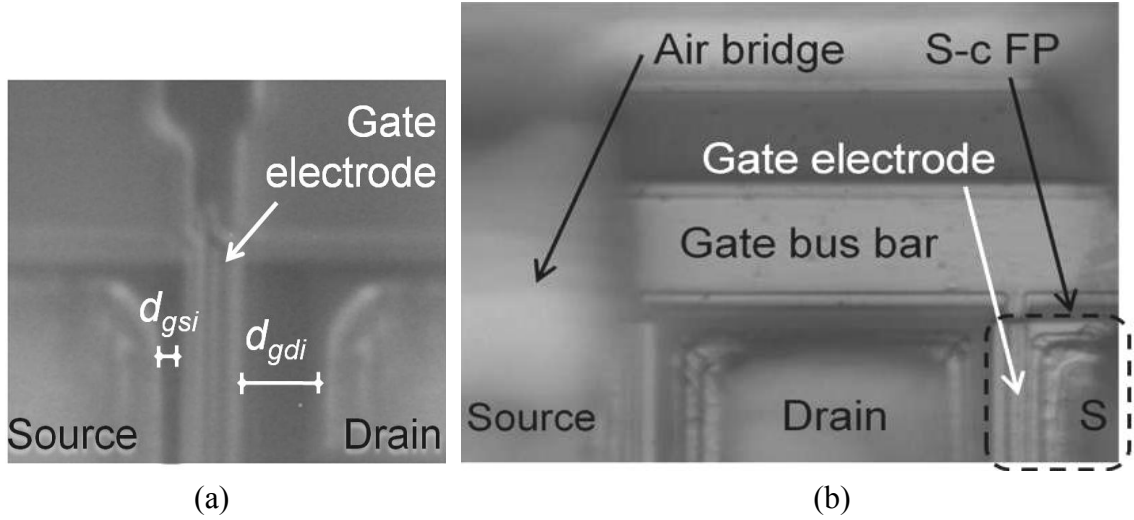


Figure 4.21 Top-view micrographs of two GaN HEMTs, (a) of a 3.2-mm IAF device, which is useful to evaluate C_{gsi}/C_{gdi} , and (b) of a 2-mm Nitronex[®] device, which shows a field plate and thus is not useful to evaluate C_{gsi}/C_{gdi} .

The usefulness of the ratio d_{gsi}/d_{gdi} is explained as follows. Recall the approximated expressions given in section 4.2.1 for C_{gsi} and C_{gdi} , equations (4.4) and (4.5). The combination of these equations as a ratio produces

$$\frac{C_{gsi}}{C_{gdi}} \approx \frac{n_{fg} \cdot \epsilon_{gsi} \frac{t_{fg} \cdot w_{fg}}{d_{gsi}}}{n_{fg} \cdot \epsilon_{gdi} \frac{t_{fg} \cdot w_{fg}}{d_{gdi}}} \approx \frac{\epsilon_{gsi}}{\epsilon_{gdi}} \cdot \frac{d_{gdi}}{d_{gsi}} \quad (4.20)$$

⁷ Leica[®] DMR microscope with fixed-magnification eyepiece of 10x, objective zooming factors of 5x, 10x 20x, 50x and 100x, and built-in Leica[®] Defocus-Controlled 300 Photo Camera

For the device depicted in Figure 4.21(b) the ratio d_{gdi}/d_{gsi} is not useful due to the field-plate structure shown in the micrograph (highlighted inside a dashed-line), because the absence of field plates is a necessary condition given in section 4.2.1 to assume values of capacitance ratios involving C_{gdi} .

On the other hand, for the device shown in Figure 4.21(a), d_{gdi}/d_{gsi} is useful to evaluate C_{gsi}/C_{gdi} with equation (4.20), considering ϵ_{gdi} and ϵ_{gsi} equal.

This section has shown an approach to generate capacitance ratio values from top-view images. The approach is able to be generalized, but only assures physically sound ratio values under specific conditions about the existence of source air bridges or field plates. Table 4.2 summarizes those conditions as questions that must be answered from the knowledge of the studied device. According to the answers, the table indicates which capacitance ratios are reliably evaluated from top-view images.

Table 4.2 Summary of capacitance ratios whose values are assumed reliably depending on the absence or presence of field plates or air bridges in the device finger layout.

	Source air bridges?					
	No		Yes (gate side)		Yes (drain side)	
	Field-plate structures?		Field-plate structures?		Field-plate structures?	
	No	Yes	No	Yes	No	Yes
Capacitance ratios reliably evaluated from top-view images	$\frac{C_{pds}}{C_{pgs}}, \frac{C_{pds}}{C_{dsi2}}, \frac{C_{dsi1}}{C_{pgd}}, \frac{C_{gsi}}{C_{gdi}}$	$\frac{C_{pds}}{C_{pgs}}, \frac{C_{pds}}{C_{dsi2}}$	$\frac{C_{dsi1}}{C_{pgd}}, \frac{C_{pds}}{C_{dsi2}}, \frac{C_{gsi}}{C_{gdi}}$	$\frac{C_{pds}}{C_{dsi2}}$	$\frac{C_{dsi1}}{C_{pgd}}, \frac{C_{gsi}}{C_{gdi}}$	<i>None</i>

The method to generate capacitance ratio values that has been introduced in the present section employs photographs with increasing zooming factor as follows:

- Taken with a commercial digital camera and the built-in microscope of the on-wafer probing station, allowing the approximate calculation of A_{p+b_g}/A_{p+b_d} and A_{p+b_d}/A_{f_d} .
- Same as above applying the zooming factor of the commercial camera, allowing the approximate calculation of d_{pgd}/d_{dsi} and w_{f_g}/l_{f_d} .
- Micrographs made with another microscope that has higher zooming factor, allowing the approximate calculation of d_{gdi}/d_{gsi} .

$$\text{Im}[Y_{11}^p - Y_{12}^p] = \omega C_{gs0} = \omega \cdot (C_{pgs} + C_{gsi} + C_{gs}) \quad (4.21)$$

$$-\text{Im}[Y_{12}^p] = -\text{Im}[Y_{21}^p] = \omega C_{gd0} = \omega \cdot (C_{pgd} + C_{gdi} + C_{gd}) \quad (4.22)$$

$$\text{Im}[Y_{22}^p - Y_{12}^p] = \omega C_{ds0} = \omega \cdot (C_{pds} + C_{dsi} + C_{ds}) \quad (4.23)$$

where C_{gs0} , C_{ds0} and C_{gd0} represent the sum of capacitance parameters in each equivalent circuit branch, the gate-source, drain-source and gate-drain branch, respectively. They are called total branch capacitances in this thesis (referred to as effective branch capacitances in [90]).

Figure 4.24 and Figure 4.23 show the extracted total branch capacitance values and the measured low-frequency Y-parameters for their extraction.

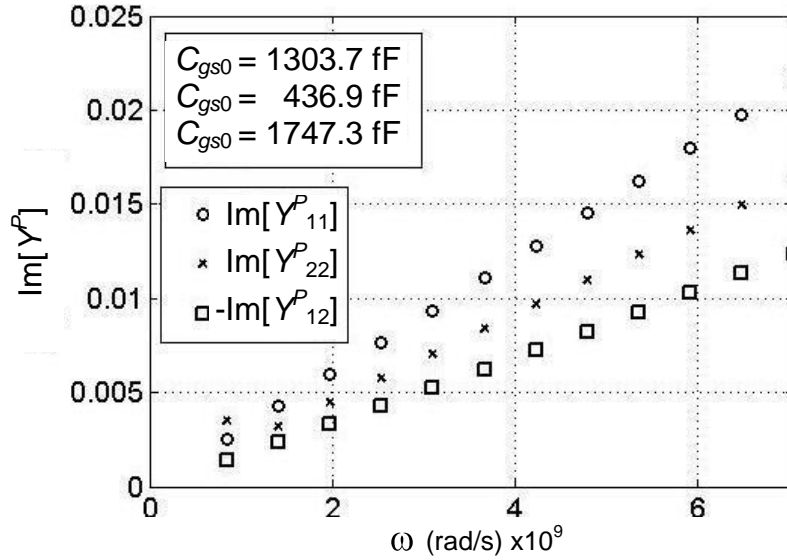


Figure 4.23 Y-parameters from *cold pinch-off* measurements in the low-frequency range and the extracted values of branch capacitances for the 2-mm device.

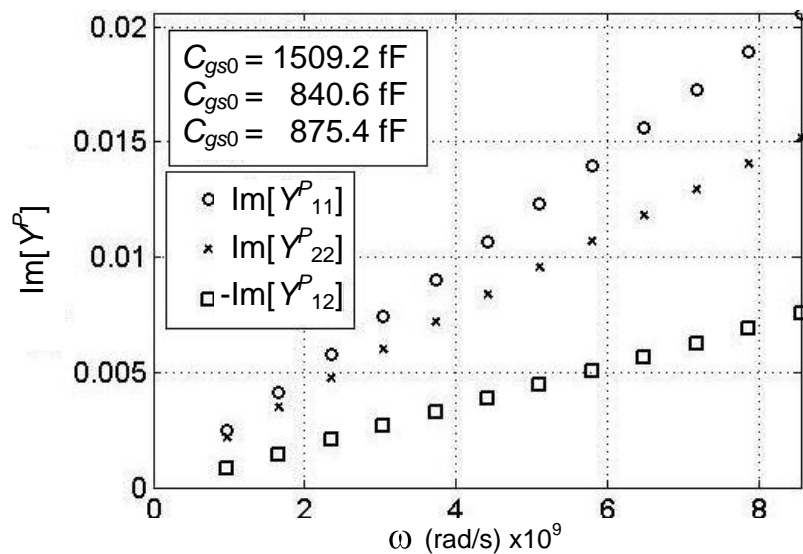


Figure 4.24 Y-parameters from *cold pinch-off* measurements in the low-frequency range and extracted values of branch capacitances for the 3.2-mm device.

4.2.4 Sweeps of Values on Capacitance Parameters

In [74] the TECR algorithm scanned values of capacitance parameters to complement the assumed capacitance ratios values and solve the equation system formed by (4.21) to (4.23). This sweeping or scanning process is described in the flowchart of Figure 4.9 by the feedback loop.

If no capacitance ratios values are assumed, the system formed by (4.21) to (4.23) requires sweeps on six capacitance parameters, but this number decreases with each generated capacitance ratio value.

In this thesis, the solution of the system formed by (4.21) to (4.23) obtained at each sweep step is called a solution candidate. A solution candidate gives values for all capacitance parameters of the model in *cold pinch-off* conditions (the unknowns of the equation system), but it also leads to the calculation of all other parameters of the model for this bias condition, with the appropriate extraction procedures shown in [74-76].

The parameter extractions of extrinsic inductance and resistance parameters that were applied in this thesis work were developed and explained in the reference publications of the TECR algorithm [74-76], and are illustrated in the following Figure 4.25 and Figure 4.26.

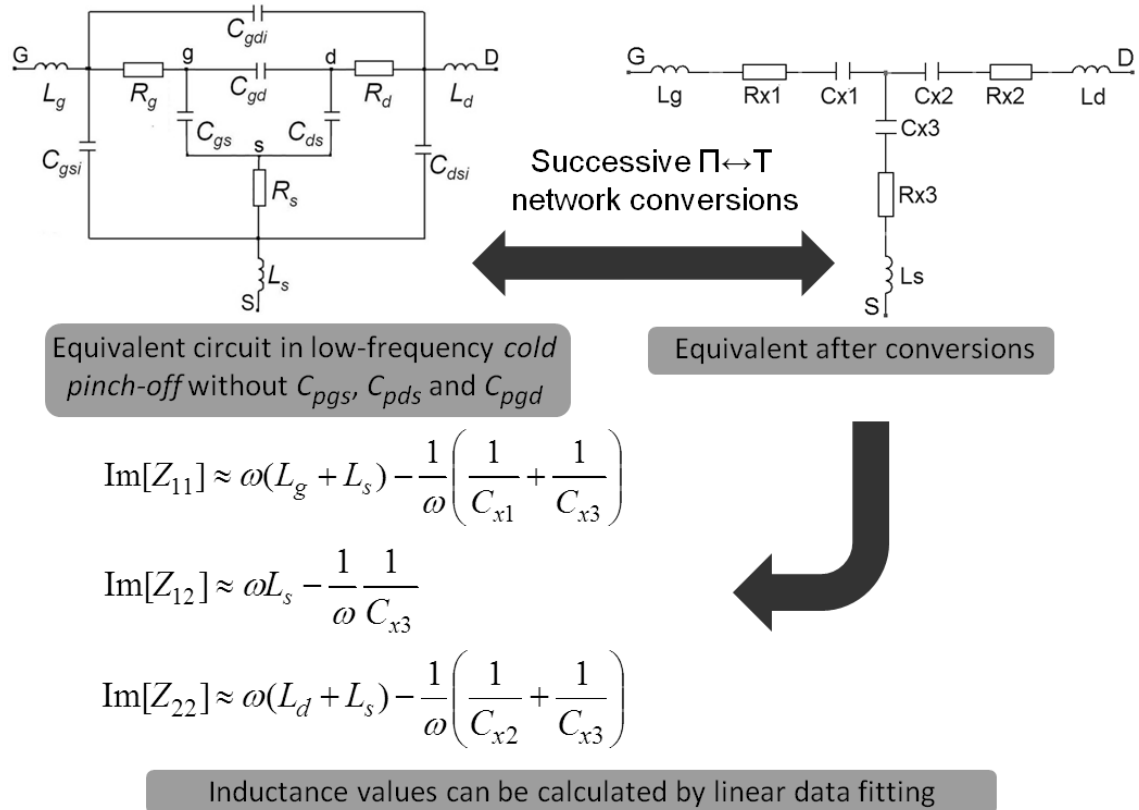


Figure 4.25 Illustration of extrinsic inductance parameter extraction used in this thesis work (drawn from the procedures described in the TECR algorithm [74-76]).

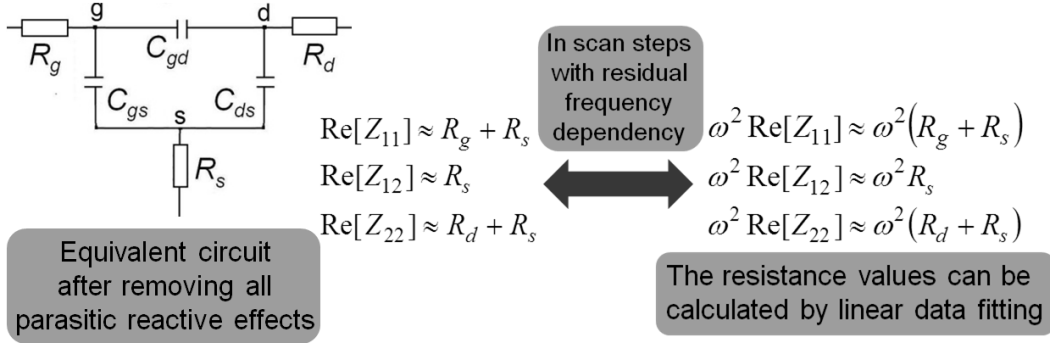


Figure 4.26 Illustration of extrinsic resistance parameter extraction used in this thesis work (drawn from the procedures described in the TECR algorithm [74-76]).

The intrinsic parameters extraction employed in this thesis work was developed and explained in the reference publications of the TECR algorithm [74-76]. It is restated in the later subchapter 4.3 of this thesis. The S-parameters constructed with the model parameter values obtained from a solution candidate are compared with measurements, using the error function formulated in [74-76] expressed by the following equation:

$$E^P = \sqrt{(E_S^2 + E_K^2 + E_G^2)/3} \quad (4.24)$$

The three components of this function refer to the S-parameters, the stability factor and the gain, respectively. They are defined in the bullet points below as in [74-76]. The equation of gain for E_G follows the definition proposed in [91], called *maximally-efficient gain* G_{EM} .

- $E_S = \frac{1}{N} \sum_{n=1}^N \frac{1}{4} \sum_{i,j=1}^2 \frac{|\text{Re}(S_{ij,n}^{\text{model}} - S_{ij,n}^{\text{meas}})| + |\text{Im}(S_{ij,n}^{\text{model}} - S_{ij,n}^{\text{meas}})|}{W_{ij}}$
- $E_G = \frac{1}{N} \sum_{n=1}^N \left| \frac{|S_{21}^{\text{meas}}|^2 - 1}{\ln|S_{21}^{\text{meas}}|^2} - \frac{|S_{21}^{\text{model}}|^2 - 1}{\ln|S_{21}^{\text{model}}|^2} \right|$
- $E_K = \frac{1}{N} \sum_{n=1}^N \left| \frac{1 - |S_{22}^{\text{meas}}|^2}{|S_{22}^{\text{meas}} - S_{11}^{\text{meas}*} \Delta S| + |S_{21}^{\text{meas}} S_{12}^{\text{meas}}|} - \frac{1 - |S_{22}^{\text{model}}|^2}{|S_{22}^{\text{model}} - S_{11}^{\text{model}*} \Delta S| + |S_{21}^{\text{model}} S_{12}^{\text{model}}|} \right|$
- The weighting factors of E_S are $W_{ij} = \max/S_{ij}/$, for S_{12} and S_{21} and $W_{ii} = 1 + \max/S_{ii}/$ for S_{11} and S_{22} .

- N is the number of frequency points measured.
- S^* is the complex conjugate.
- ΔS is the determinant of the correspondent S-parameter matrix at each frequency.

The error function gives a value to the solution candidate, which is denoted in the following with the term E^P .

This error function is specifically oriented to compare modeled S-parameters and measurements in pinch-off conditions by the usage of weighting factors W_{ij} , which balance the high reflection and the low transmission coefficients typical of such measurements [74]. This specific orientation of the error function explains the employed superscript “ P ”: It refers to the term pinch-off.

In this thesis work, sweeps of values on more than five capacitance parameters have proven to be slow and unpractical. For example, the sweeps on six parameters realized to obtain Figure 4.10 and Figure 4.16 took several hours of computing time. Besides, visual inspection of the minimum value in a 6D space is not straightforward. Thus, this thesis work proposes to employ a maximum of four sweeps.

If the capacitance ratios reliably evaluated are less than two, more than four sweeps would be needed. Then, this thesis proposes to omit one or two capacitance parameters in the model, to perform a maximum of four sweeps. Omitted parameters must be reasonably expected to have minor effects, so as to take them as equal to zero. For instance, C_{pgd} can be omitted making $C_{pgd} = 0$, for devices whose physical structure enhances capacitive effects related to C_{gd} and C_{gdi} so that their values dominate C_{gd0} .

In the following pages of the present section, sweeps of values on four capacitance parameters are applied with measurements of the 3.2-mm and 2-mm GaN HEMTs. The total branch capacitances are initial upper limit values of the sweeps and were calculated and reported in section 4.2.3.

Source air bridges in the gate side of the finger layout of the 2-mm device were shown in Figure 4.19. Source-connected field plates that this device possesses were depicted in Figure 3.2. Therefore, only C_{pds}/C_{dsi2} can be reliably evaluated, according to Table 4.2.

The top-view photo of Figure 4.19 is used to evaluate C_{pds}/C_{dsi2} with eq. (4.17). The calculated value of A_{p+b_d}/A_{f_d} is 1.1, and thus, $C_{pds}/C_{dsi2} \approx 1.1$.

C_{pgd} and C_{gdi} are omitted, taking them as zero, to perform four sweeps of values, on C_{gsi} , C_{dsi} , C_{ds} and on the ratio C_{gs}/C_{gd} . The values of C_{gsi} , C_{dsi} , C_{ds} and C_{gs}/C_{gd} of each sweep step, together with the generated value of C_{pds}/C_{dsi2} , solve the equation system of (4.21) to (4.23), allowing the calculation of all capacitance parameters as follows:

$$C_{gd} = C_{gd0} \quad (4.25a)$$

$$C_{gs} = (C_{gs}/C_{gd}) \cdot C_{gd} \quad (4.25b)$$

$$C_{pgs} = C_{gs0} - C_{gsi} - C_{gs}, \quad (4.25c)$$

$$C_{pds} = C_{ds0} - C_{dsi} - C_{ds} \quad (4.25d)$$

$$C_{dsi2} = C_{pds}/(C_{pds}/C_{dsi2}) \quad (4.25e)$$

$$C_{dsi1} = C_{dsi} - C_{dsi2} \quad (4.25f)$$

Sweep steps that give negative capacitance values are discarded.

The results of the sweeps are E^P values varying in terms of the capacitance parameters whose values were swept, which means that a four-variable function is obtained: $E^P(C_{gsi}, C_{dsi}, C_{ds}, C_{gs}/C_{gd})$.

Figure 4.27 and Figure 4.28 illustrate the results of the four sweeps of values applied to the measurements of the 2-mm device. In these figures, the four-variable function $E^P(C_{gsi}, C_{dsi}, C_{ds}, C_{gs}/C_{gd})$ is mapped using three 3D graphs and one 2D plot as explained in the following paragraphs.

First, fixing the value of C_{gs}/C_{gd} (e.g. $C_{gs}/C_{gd} = 1$) reduces the dimension of E^P to a three-variable function, $E^P(C_{gsi}, C_{dsi}, C_{ds})$ that can be illustrated as a parameterized stack of surfaces (3D graphs). The surfaces must be mapped on a plane formed by two variables and it must be parameterized by the third variable. If the parametrical variable is alternated between the three available, then three distinct stacks of surfaces are obtained. For the results of the sweeps applied to measurements of the 2-mm device, the three stacks of surfaces are shown in Figure 4.27 and Figure 4.28(a).

- In Figure 4.27(a), $E^P(C_{gsi}, C_{dsi}, C_{ds})$ is mapped over the plane formed by C_{ds} and C_{gsi} and the parametrical component is C_{dsi} .
- In Figure 4.27(b), $E^P(C_{gsi}, C_{dsi}, C_{ds})$ is mapped over the plane formed by C_{dsi} and C_{gsi} and the parametrical component is C_{ds} .
- In Figure 4.28(a), $E^P(C_{gsi}, C_{dsi}, C_{ds})$ is mapped over the plane formed by C_{ds} and C_{dsi} and the parametrical component is C_{gsi} .

As reference, the regions around the minimum E^P values are highlighted with a rounded rectangle in each graph of Figure 4.27 and Figure 4.28.

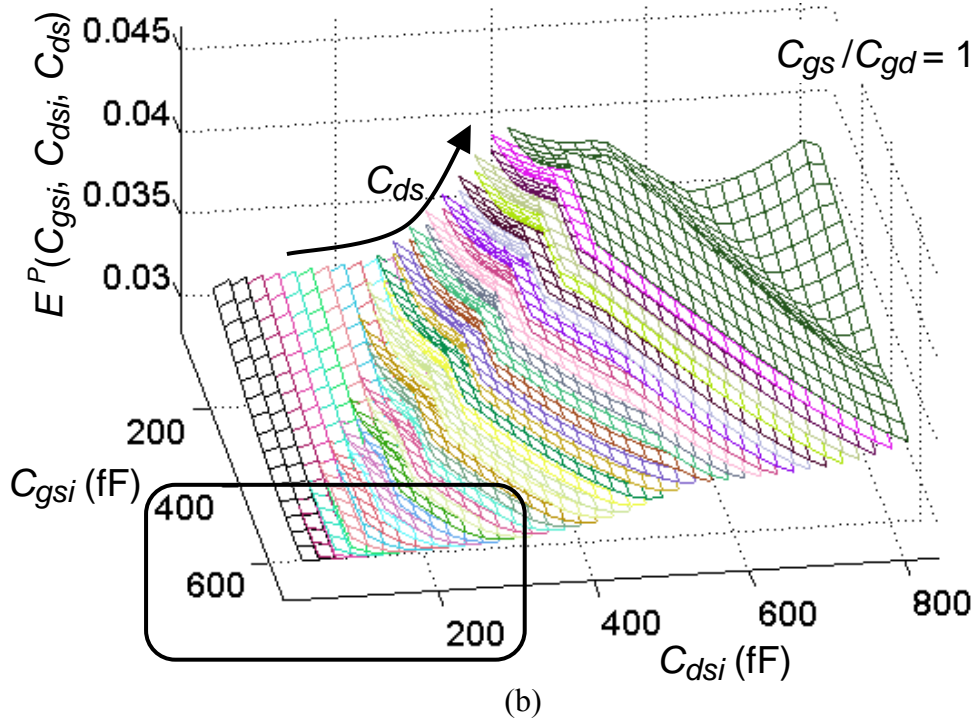
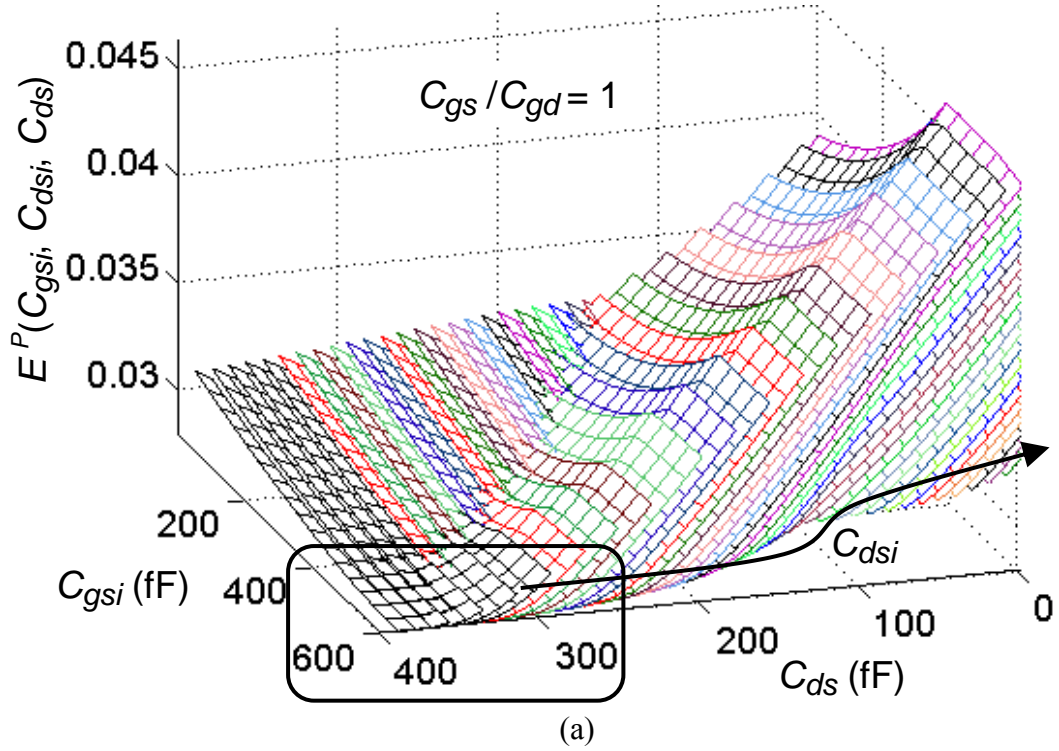


Figure 4.27 First set of graphs resulting from applying the sweeps of values on four capacitance parameters using *cold pinch-off* S-parameters measurements of the 2-mm device: Sweep results of $E^P(C_{gsi}, C_{ds}, C_{dsi})$ values mapped on the planes of (a) C_{gsi} versus C_{ds} and (b) C_{gsi} versus C_{dsi} .

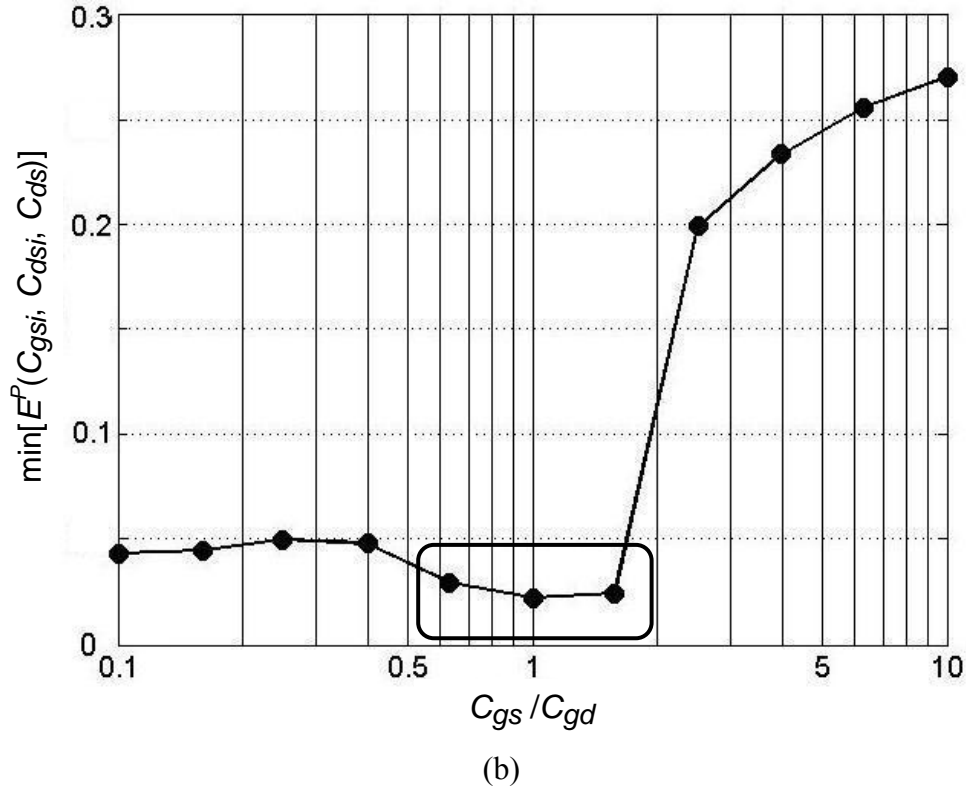
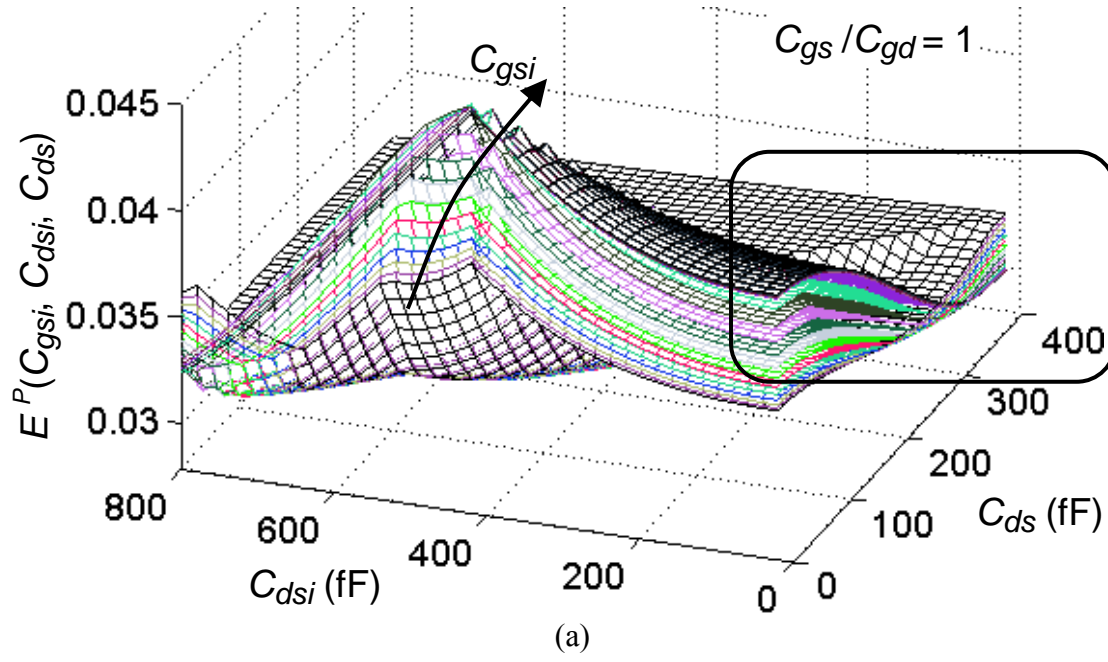


Figure 4.28 Second set of graphs resulting from applying the sweeps of values on four capacitance parameters using *cold pinch-off* S-parameters measurements of the 2-mm device. (a) Sweep results of $E^P(C_{gsi}, C_{ds}, C_{dsi})$ values mapped on the plane of C_{ds} versus C_{dsi} , and (b) $\min[E^P(C_{gsi}, C_{ds}, C_{dsi})]$ plotted with respect to C_{gs}/C_{gd} .

A different four-variable function $E^P(C_{gsi}, C_{dsi}, C_{ds})$, i.e. a different parameterized stack of surfaces (3D graphs), is obtained with each value swept on C_{gs}/C_{gd} . Then, the minimum value of each stack of surfaces, $\min[E^P(C_{gsi}, C_{ds}, C_{dsi})]$, can be mapped in a 2D plot with respect to the

different values swept on C_{gs}/C_{gd} . The point with the lowest value in such 2D plot is related to the specific values of C_{dsi} , C_{ds} , C_{gsi} and C_{gs}/C_{gd} that correspond to the best solution candidate. For the sweep results with measured data of the 2-mm device, that 2D plot is shown in Figure 4.28(b) and the best solution candidate found is listed in Table 4.3.

Table 4.3 Model parameter values related to the best solution candidate found with the four-parameter sweep using *cold pinch-off* S-parameter measurements of the 2-mm device.

Best solution candidate (fF)										
C_{pgs}	C_{gsi}	C_{gs}	C_{pds}	C_{dsi}	C_{ds}	C_{dsi1}	C_{dsi2}	C_{pgd}	C_{gdi}	C_{gd}
190.60	442.74	875.42	157.02	329.75	353.29	187.01	142.74	0.00	0.00	875.42
Extrinsic inductance (pH) and resistance (Ω) parameters							Intrinsic resistance (Ω) parameters			
L_g	L_d	L_s	R_g	R_d	R_s	R_i		R_{gd}		
42.38	77.19	17.12	2.33	2.91	0.21	0.53		0.00		

The sweeps of values applied to the measured data of the 3.2-mm device are discussed in the following paragraphs of the section.

Source air bridges in the gate side of the finger layout of such device were depicted previously in Figure 4.19. As demonstrated in Figure 4.21, the studied device does not have source-connected field plates. Therefore, the ratios C_{dsi1}/C_{pgd} , C_{pds}/C_{dsi2} and C_{gsi}/C_{gdi} can be reliably evaluated, according to Table 4.2.

The top-view photograph in Figure 4.19 is employed to evaluate C_{pds}/C_{dsi2} with equation (4.17). The estimated value of A_{p+b_d}/A_{f_d} is 1.02 and thus $C_{pds}/C_{dsi2} \approx 1.02$.

The top-view photograph in Figure 4.21 is used to evaluate C_{gsi}/C_{gdi} with equation (4.20). The estimated value of d_{gdi}/d_{gsi} is 4.25 and thus $C_{gsi}/C_{gdi} \approx 4.25$.

The top-view photograph in Figure 4.20 is used to evaluate C_{dsi1}/C_{pgd} with equation (4.19). The estimated values of d_{pgd}/d_{dsi} and w_{f_g}/l_{f_d} are 1.28 and 7.04, with $n_{f_g}/n_{f_d} = 2$, thus $C_{dsi1}/C_{pgd} \approx 18.03$.

The two capacitance parameters omitted for the 2-mm device (C_{pgd} , C_{gdi}) do not have to be omitted for the 3.2-mm device to perform a maximum of 4 sweeps of values, because for this device two capacitance ratio values are generated more than for the 2-mm device. The same four sweeps are proposed as previously, on C_{gsi} , C_{dsi} , C_{ds} and the ratio C_{gs}/C_{gd} . The values of C_{gsi} , C_{dsi} , C_{ds} and C_{gs}/C_{gd} of each sweep step, together with

the generated values of C_{pds}/C_{dsi2} , C_{dsi1}/C_{pgd} and C_{gsi}/C_{gdi} solve the equation system of (4.21) to (4.23), given all the capacitance parameters as follows:

$$C_{pds} = C_{ds0} - C_{dsi} - C_{ds} \quad (4.26a)$$

$$C_{dsi2} = C_{pds}/(C_{pds}/C_{dsi2}) \quad (4.26b)$$

$$C_{dsi1} = C_{dsi} - C_{dsi2} \quad (4.26c)$$

$$C_{pgd} = C_{dsi1}/(C_{dsi1}/C_{pgd}) \quad (4.26d)$$

$$C_{gdi} = C_{gsi}/(C_{gsi}/C_{gdi}) \quad (4.26e)$$

$$C_{gd} = C_{gd0} - C_{gdi} - C_{pgd} \quad (4.26f)$$

$$C_{gs} = (C_{gs}/C_{gd}) \cdot C_{gd} \quad (4.26g)$$

$$C_{pgs} = C_{gs0} - C_{gsi} - C_{gs} \quad (4.26h)$$

As mentioned before, solution candidates lead to the extraction of all model parameters in *cold pinch-off* conditions. For this, the applied extractions of intrinsic parameters and of extrinsic inductance and resistance parameters are the same as those used for the 2-mm device. The error function applied to find the E^P value of the solution candidates is also the same as in the sweep for the 2-mm device, given by equation (4.24).

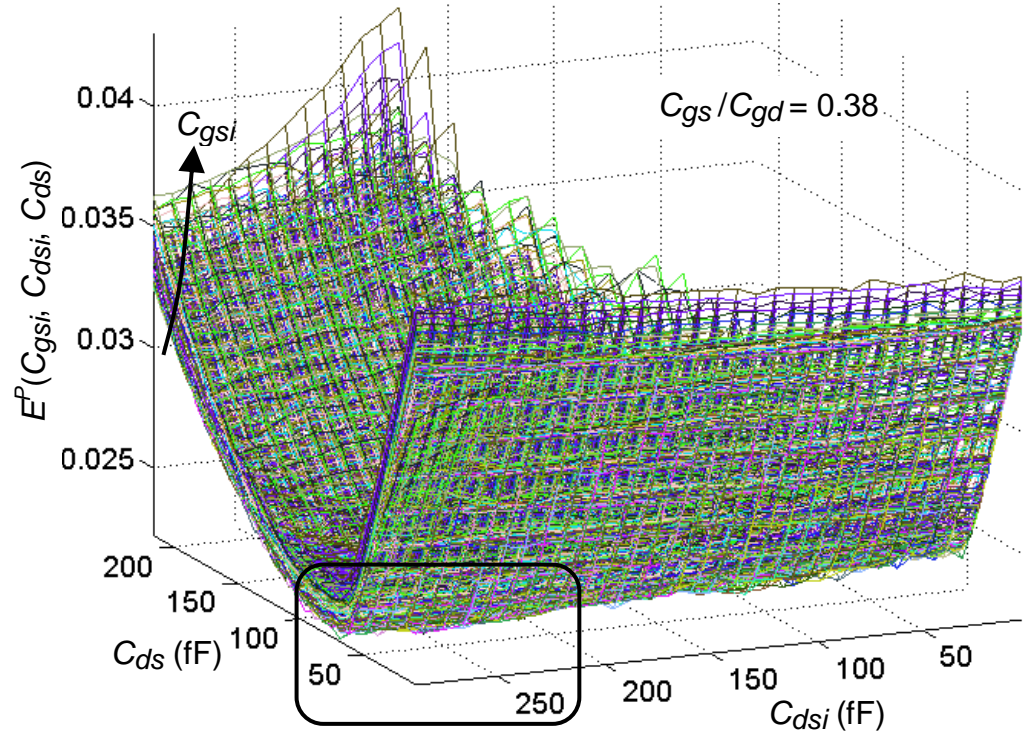
Similarly as for the 2-mm device, the result of the applying the sweeps of values to the measured data of the 3.2-mm device is a four-variable function of E^P values: $E^P(C_{gsi}, C_{dsi}, C_{ds}, C_{gs}/C_{gd})$.

Figure 4.29 and Figure 4.30 illustrate $E^P(C_{gsi}, C_{dsi}, C_{ds}, C_{gs}/C_{gd})$ using three 3D graphs and one 2D plot in the same way as it was done in Figure 4.27 and Figure 4.28 for the 2-mm device.

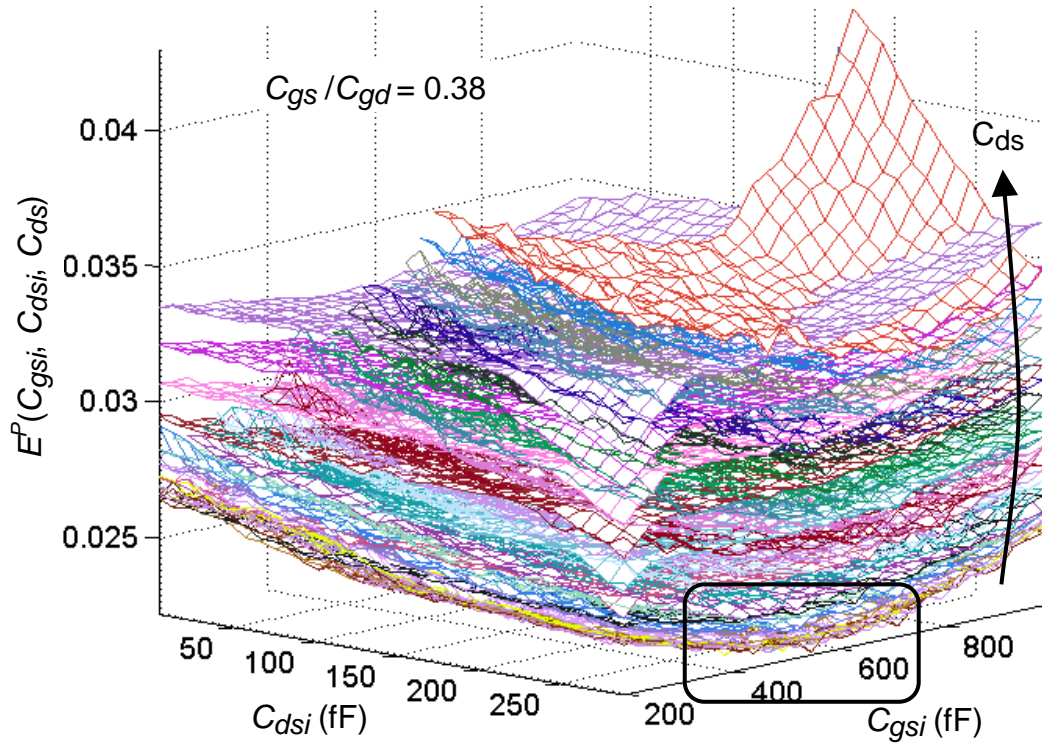
The first step to illustrate this four-variable function is fixing the value of C_{gs}/C_{gd} (e.g. $C_{gs}/C_{gd} = 0.38$) to obtain a three-variable function $E^P(C_{gsi}, C_{dsi}, C_{ds})$, which can be portrayed as a parameterized stack of 3D graphs. The parametrical variable is alternated between the three available and the received stacks of surfaces are shown in Figure 4.29 and Figure 4.30(a).

- In Figure 4.29(a), $E^P(C_{gsi}, C_{dsi}, C_{ds})$ is mapped over the plane formed by C_{ds} and C_{dsi} and the parametrical component is C_{gsi} .
- In Figure 4.29(b), $E^P(C_{gsi}, C_{dsi}, C_{ds})$ is mapped over the plane formed by C_{dsi} and C_{gsi} and the parametrical component is C_{ds} .
- In Figure 4.30(a), $E^P(C_{gsi}, C_{dsi}, C_{ds})$ is mapped over the plane formed by C_{ds} and C_{gsi} and the parametrical component is C_{dsi} .

As reference, the regions around the minimum E^P values are highlighted with a rounded rectangle in each graph of Figure 4.29 and Figure 4.30.



(a)



(b)

Figure 4.29 First set of graphs resulting from applying the sweeps of values on four capacitance parameters using *cold pinch-off* S-parameters measurements of the 3.2-mm device. Sweep results of $E^P(C_{gsi}, C_{ds}, C_{dsi})$ values mapped on the planes of (a) C_{dsi} versus C_{ds} and (b) C_{gsi} versus C_{dsi} .

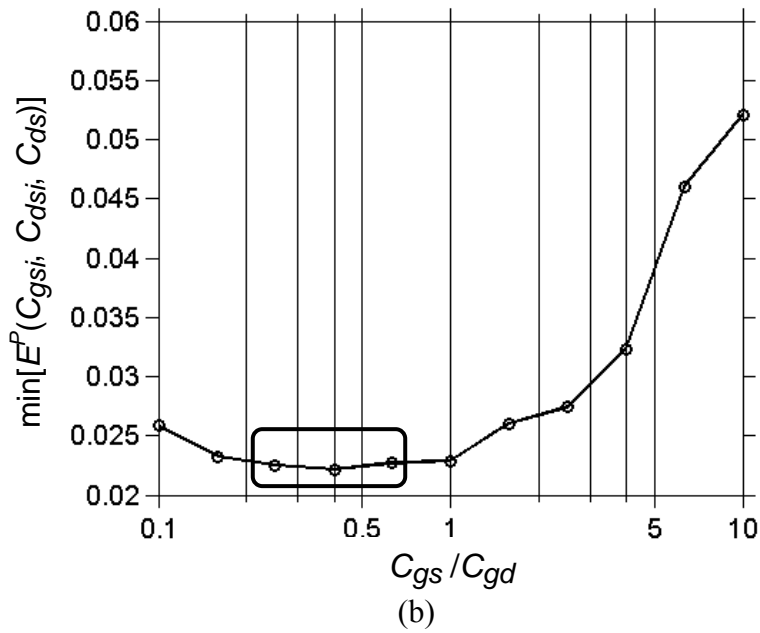
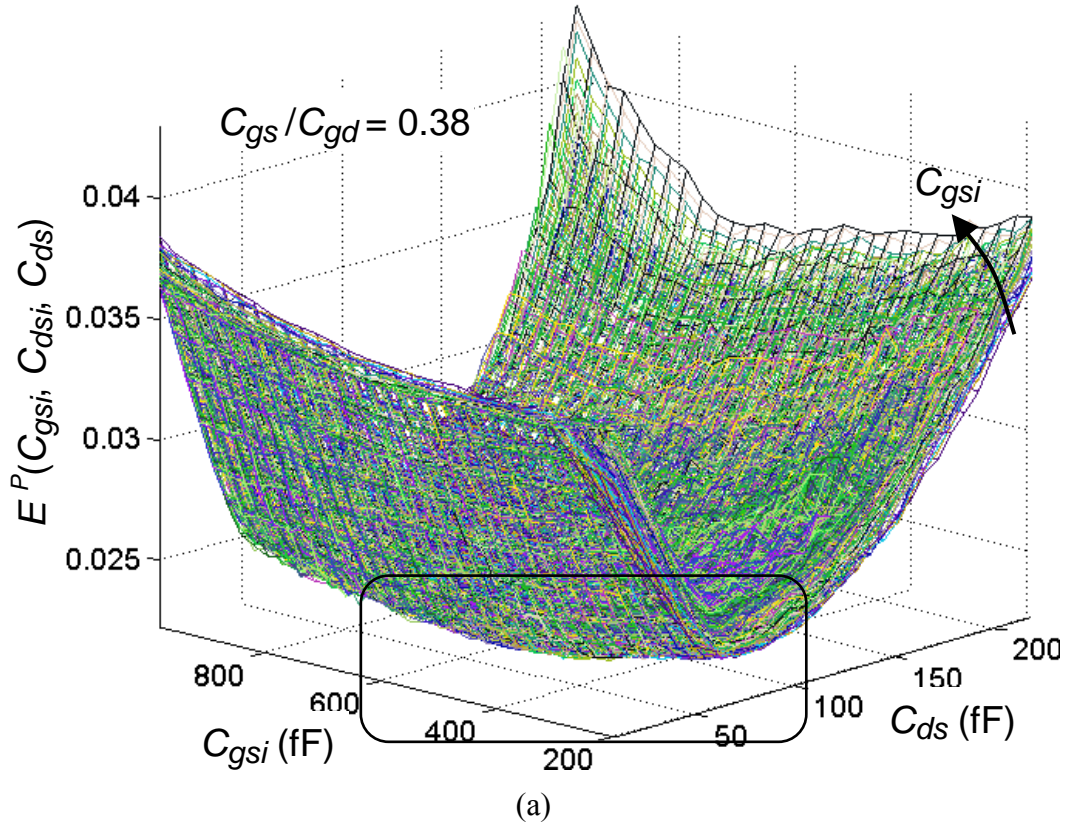


Figure 4.30 Second set of graphs resulting from applying the sweeps of values on four capacitance parameters using *cold pinch-off* S-parameters measurements of 3.2-mm device. (a) Sweep results of $E^P(C_{gsi}, C_{ds}, C_{dsi})$ values mapped on the plane of C_{ds} versus C_{gsi} , and (b) $\min[E^P(C_{gsi}, C_{ds}, C_{dsi})]$ plotted with respect to C_{gs}/C_{gd} .

Different three-variable functions $E^P(C_{gsi}, C_{dsi}, C_{ds})$, i.e. parameterized stack of surfaces, are obtained with each value swept on C_{gs}/C_{gd} . The minimum value of each stack of surfaces, $\min[E^P(C_{gsi}, C_{ds}, C_{dsi})]$, can be mapped in a 2D plot with respect to the different values swept on C_{gs}/C_{gd} .

That is shown in Figure 4.30(b) for the sweeps applied to the measured data of the 3.2-mm device. The point with the lowest value in such 2D plot is related to the specific values of C_{dsi} , C_{ds} , C_{gsi} and C_{gs}/C_{gd} that correspond to the best solution candidate. The best solution candidate found with the proposed sweeps for the 3.2-mm device is listed in Table 4.3.

Table 4.4 Model parameter values related to the best solution candidate found with the four-parameter sweep and *cold pinch-off* S-parameters of the 3.2-mm device.

Best solution candidate (fF)										
C_{pgs}	C_{gsi}	C_{gs}	C_{pds}	C_{dsi}	C_{ds}	C_{dsi1}	C_{dsi2}	C_{pgd}	C_{gdi}	C_{gd}
201.38	523.17	579.14	99.74	259.33	77.89	161.55	97.78	8.96	123.10	1614.98
Extrinsic inductance (pH) and resistance (Ω) parameters							Intrinsic resistance (Ω) parameters			
L_g	L_d	L_s	R_g	R_d	R_s		R_i	R_{gd}		
90.10	187.27	0.59	3.79	1.43	0.41		0.00	0.00		

In sweeps of values on three capacitance parameters, the result is a three-variable function for the E^P values that can be shown as a single stack of surfaces. Then, the lowest point in the stack would be linked to best solution candidate.

Visual inspection of the best solution candidate for sweeps of values on fewer capacitance parameters than three becomes thus a trivial problem.

4.2.5 Extraction of Extrinsic Resistance Parameters

The TEQR algorithm used *cold forward* S-parameters for the extraction of extrinsic resistance parameters [74]. Measurements on that bias point were first proposed in [80] and are used in several works [67-69, 74, 78, 80, 92-94], where under consideration that extraction of extrinsic resistance parameter from *cold pinch-off* S-parameters is problematic or unreliable.

According to [78], *cold forward* S-parameters measurements useful to extract extrinsic resistance parameters are characterized by: (i) $V_{DS} = 0V$ and a positive V_{GS} value, (ii) a high value of I_{GS} , and (iii) a positive imaginary part of S_{11} in the entire frequency range measured.

Experiments of the author of this thesis with different GaN HEMTs showed that the $+V_{GS}$ value required to produce predominant inductive behavior of S_{11} is generally higher than the values applied usually for GaAs devices. Such an observation coincides with the findings published in other works of GaN device modeling [80, 94], where this was explained by the higher differential resistance of the gate that is typical of GaN transistors.

Further experiments with similar GaN devices of different manufacturers demonstrated that the gate differential resistance (and thus the positive V_{GS} value needed to produce dominant inductive behavior of S_{11}) varies greatly among devices of different fabrication processes, as illustrated with the experimental results reported in Figure 4.31.

Figure 4.31(a) presents measurements of S_{11} corresponding to a 0.1-mm AlGaIn/GaN HEMT fabricated by the *Ferdinand-Braun Institut für Höchstfrequenztechnik*, (FBH), in Berlin, Germany. The S_{11} measurements exhibit a decreasing capacitive behavior with increasing V_{GS} values ($V_{DS} = 0V$), until inductive behavior is considered dominant at $V_{GS} = +1.74V$.

In contrast, Figure 4.31(b) depicts S_{11} measurements of 0.1-mm AlGaIn/GaN HEMT that was manufactured the *Institut d'électronique de microélectronique et de nanotechnologie*, (IEMN), Université Lille Nord de France. In those measurements, the decrease of capacitive behavior with increasing V_{GS} values is less pronounced than in the measurements depicted in Figure 4.31(a). Even with $V_{GS} = +2V$ ($V_{DS} = 0V$), the measured S_{11} of the IEMN device does not exhibit a dominant inductive behavior comparable to the one shown in Figure 4.31(a) at $V_{GS} = +1.74V$.

S-parameter measurements of these two devices were performed in similar ranges of frequency and voltage and the device size is the same, so the difference in V_{GS} value needed to produce dominant inductive behavior of S_{11} is attributed to differences in the fabrication processes of the devices.

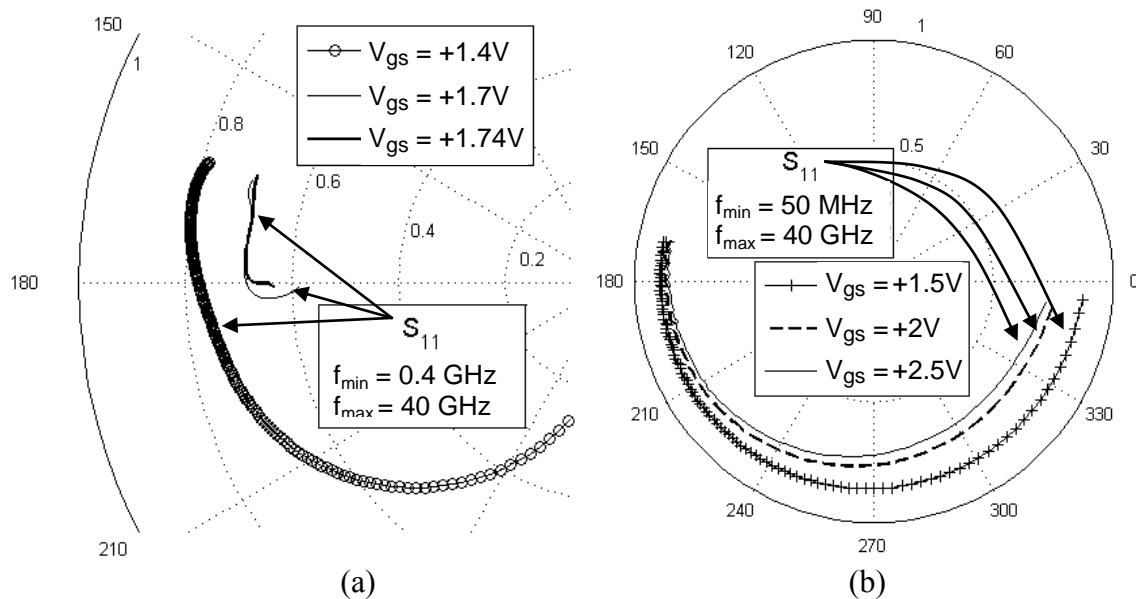


Figure 4.31 Variation between GaN devices of different manufacturers of the positive V_{GS} value needed to produce dominant inductive behavior of S_{11} ($V_{DS} = 0V$). The related transistors have the same size (0.1 mm) but were fabricated by (a) FBH and (b) IEMN.

Moreover, reference [68] showed that the positive V_{GS} value required to produce predominant inductive behavior of S_{11} , and the related high I_{GS} could damage or destroy the Schottky contact of the gate, causing long-term or irreversible harm to the device response. Instead of *cold forward*, that work proposed an alternative bias condition for the extraction of extrinsic resistance parameters, a condition known as *cold reverse* [68, 92], characterized by $V_{DS} = 0V$, V_{GS} between $V_{pinch-off}$ and $0V$, and $I_{GS} = 0A$.

When the device is biased with $V_{DS} = 0V$ and the extrinsic capacitances and inductances effects have been subtracted, the remaining device effects are represented by the Z-parameters matrix given by equation (4.27) [67, 69, 81, 92, 94, 95], which is called $[Z^{Rcold}]$ in this thesis.

$$[Z^{Rcold}] = \begin{bmatrix} R_s + R_g + Z_{gg} + \alpha Z_{ch} & R_s + \beta Z_{ch} \\ R_s + \beta Z_{ch} & R_s + R_d + Z_{ch} \end{bmatrix} \quad (4.27)$$

where Z_{ch} and Z_g represent the impedances of the conduction channel and of the gate Schottky contact, respectively,

$$Z_{ch} = \frac{R_{ch}}{1 + j\omega C_{ch} R_{ch}} = \frac{R_{ch}}{1 + \omega^2 C_{ch}^2 R_{ch}^2} + j \cdot \frac{-\omega C_{ch} R_{ch}^2}{1 + \omega^2 C_{ch}^2 R_{ch}^2}, \quad (4.28)$$

$$Z_{gg} = \frac{R_{gg}}{1 + j\omega C_{gg} R_{gg}} = \frac{R_{gg}}{1 + \omega^2 C_{gg}^2 R_{gg}^2} + j \cdot \frac{-\omega C_{gg} R_{gg}^2}{1 + \omega^2 C_{gg}^2 R_{gg}^2}. \quad (4.29)$$

Z_{ch} is represented as a distributed effect by the constants α and β .

Biasing the transistor with $V_{GS} \geq 0V$ and with $V_{GS} \leq V_{Pinch-off}$ are the two extreme cases of *cold* bias conditions ($V_{DS} = 0V$).

In the case with $V_{GS} \geq 0V$, the channel resistance is minimized, causing the frequency-varying term in (4.28) to rapidly vanish in the GHz region, reducing (4.27) to $R_s + R_g + \alpha R_{ch}$, $R_s + \beta R_{ch}$ and $R_s + R_d + R_{ch}$. A drawback of this bias condition for resistance parameter extraction is that the above three terms are easily affected either by the frequency dependency of the channel resistance that occurs in devices prone to dispersive behavior, or by the bias dependency of the channel resistance that appears for small fluctuations of V_{DS} and V_{GS} (in mV) from the nominal values supplied.

In the case with $V_{GS} \leq V_{Pinch-off}$, the channel resistance is maximized, reducing the imaginary parts of (4.28) to capacitive effects and causing large frequency-varying terms in the real parts of (4.27). A drawback of

this bias condition, for the resistance parameter extraction, is that those large frequency-varying terms typically mask the effects of R_g , R_s and R_d .

In *cold reverse* bias conditions, with V_{GS} less negative than $V_{Pinch-off}$, the channel resistance is decreased from its highest values and this allows the effects of R_g , R_s and R_d to be clearly visible in certain frequency ranges. At the same time, the related R_{ch} is not low enough to make the term $\omega^2 C_{ch}^2 R_{ch}^2$ negligible with respect to unity, and therefore *cold reverse* bias conditions maintain the effect of C_{ch} in (4.28). Keeping the effect of C_{ch} reduces the variations of the real parts of (4.27) due to dependencies of the channel resistance that are not considered in the present small-signal circuit (e.g. frequency or bias dependencies or temperature-related effects).

The problem of the *cold reverse* condition is formulating the parameter extraction to find the values of α , β , R_{ch} , C_{ch} , R_{gg} and C_{gg} , in order to separate the frequency-varying terms in (4.27) from the values of R_g , R_s and R_d . The required formulation is explained in the following paragraphs.

First, in the *cold reverse* condition the diode-like effect of the gate Schottky contact is reverse biased, so its conductance is negligible, which means that R_{gg} is expected to be large as has been reported in [67, 77] (in the order of $k\Omega$ or $M\Omega$). Therefore, Z_{gg} of equation (4.29) is reduced to $-1/(\omega C_{gg})$, as in the models described in [68, 95], then real and imaginary parts of (4.27) are expressed by the following expressions:

$$\text{Re}[Z_{11}^{Rcold}] \approx R_g + R_s + \alpha \cdot \frac{R_{ch}}{1 + \omega^2 C_{ch}^2 R_{ch}^2} \quad (4.30)$$

$$\text{Re}[Z_{12}^{Rcold}] = R_s + \beta \cdot \frac{R_{ch}}{1 + \omega^2 C_{ch}^2 R_{ch}^2} \quad (4.31)$$

$$\text{Re}[Z_{22}^{Rcold}] = R_d + R_s + \frac{R_{ch}}{1 + \omega^2 C_{ch}^2 R_{ch}^2} \quad (4.32)$$

$$\text{Im}[Z_{11}^{Rcold}] \approx -\frac{1}{\omega C_{gg}} - \alpha \cdot \frac{\omega C_{ch} R_{ch}^2}{1 + \omega^2 C_{ch}^2 R_{ch}^2} \quad (4.33)$$

$$\text{Im}[Z_{12}^{Rcold}] = -\beta \cdot \frac{\omega C_{ch} R_{ch}^2}{1 + \omega^2 C_{ch}^2 R_{ch}^2} \quad (4.34)$$

$$\text{Im}[Z_{22}^{Rcold}] = -\frac{\omega C_{ch} R_{ch}^2}{1 + \omega^2 C_{ch}^2 R_{ch}^2} \quad (4.35)$$

Hereby it is assumed that the values of extrinsic capacitance and inductance parameters are known from the *cold pinch-off* S-parameters measurements, for instance for a solution candidate generated by sweeps of values discussed in section 4.2.4.

Then, those reactive effects are subtracted of the measured *cold reverse* S-parameters with the following equation (4.36), derived by matrix manipulation similar to that presented in [81]. This equation gives the measured data that corresponds to $[Z^{Rcold}]$.

$$[Z^{Rcold}] = \left\langle \left(([Y^{cr}] - [C^{ext-p}])^{-1} - [L^{ext}] \right)^{-1} - [C^{ext-i}] \right\rangle^{-1} \quad (4.36)$$

where $[Y^{cr}]$ is obtained from *cold reverse* S-parameters measurements by the formulae of S- to Y-parameter conversion. The other matrixes are

$$[C^{ext-i}] = j\omega \begin{bmatrix} C_{gsi} + C_{gdi} & -C_{gdi} \\ -C_{gdi} & C_{dsi} + C_{gdi} \end{bmatrix}, \quad (4.37)$$

$$[L^{ext}] = j\omega \begin{bmatrix} L_g + L_s & L_s \\ L_s & L_d + L_s \end{bmatrix}, \quad (4.38)$$

$$[C^{ext-p}] = j\omega \begin{bmatrix} C_{pgs} + C_{pgd} & -C_{pgd} \\ -C_{pgd} & C_{pds} + C_{pgd} \end{bmatrix}. \quad (4.39)$$

Now, note that equation (4.32) is written in terms of equation (4.35) as follows:

$$\text{Re}[Z_{22}^{Rcold}] = R_d + R_s + \frac{-\text{Im}[Z_{22}^{Rcold}]}{\omega} \cdot \frac{1}{C_{ch} R_{ch}} \quad (4.40)$$

Multiplying by $\omega/\text{Im}[Z_{22}^{Rcold}]$ the following equation is received:

$$\frac{\text{Re}[Z_{22}^{Rcold}]}{\text{Im}[Z_{22}^{Rcold}]} \cdot \omega = \frac{-1}{C_{ch} R_{ch}} + \frac{\omega}{\text{Im}[Z_{22}^{Rcold}]} \cdot (R_d + R_s) \quad (4.41)$$

And then, the sum $R_s + R_d$ is obtained as the slope of the linear approximation to the plot of $\omega \text{Re}[Z_{22}^{Rcold}]/\text{Im}[Z_{22}^{Rcold}]$ in terms of $\omega/\text{Im}[Z_{22}^{Rcold}]$.

The sum R_s+R_g and the value of R_s are found in similar way, using respectively $\text{Re}[Z_{11}^{Rcold}]$ and $\text{Re}[Z_{12}^{Rcold}]$ instead of $\text{Re}[Z_{22}^{Rcold}]$.

Figure 4.32 and Figure 4.33 show the results of applying the extraction of extrinsic resistance parameters with measured *cold reverse* S-parameters of the 2-mm device and of the 3.2-mm device. The values of extrinsic reactive parameters removed of the measured data to obtain $[Z^{Rcold}]$ of each device were listed previously in Table 4.3 and Table 4.4. The V_{GS} voltages used for the *cold reverse* bias condition were $V_{GS} = -1.6\text{V}$ and $V_{GS} = -3.6\text{V}$, respectively (both with $V_{DS} = 0\text{V}$).

The values of extrinsic resistance parameters extracted from *cold reverse* S-parameter measurements with described method are summarized in Table 4.5, for the studied large-size devices.

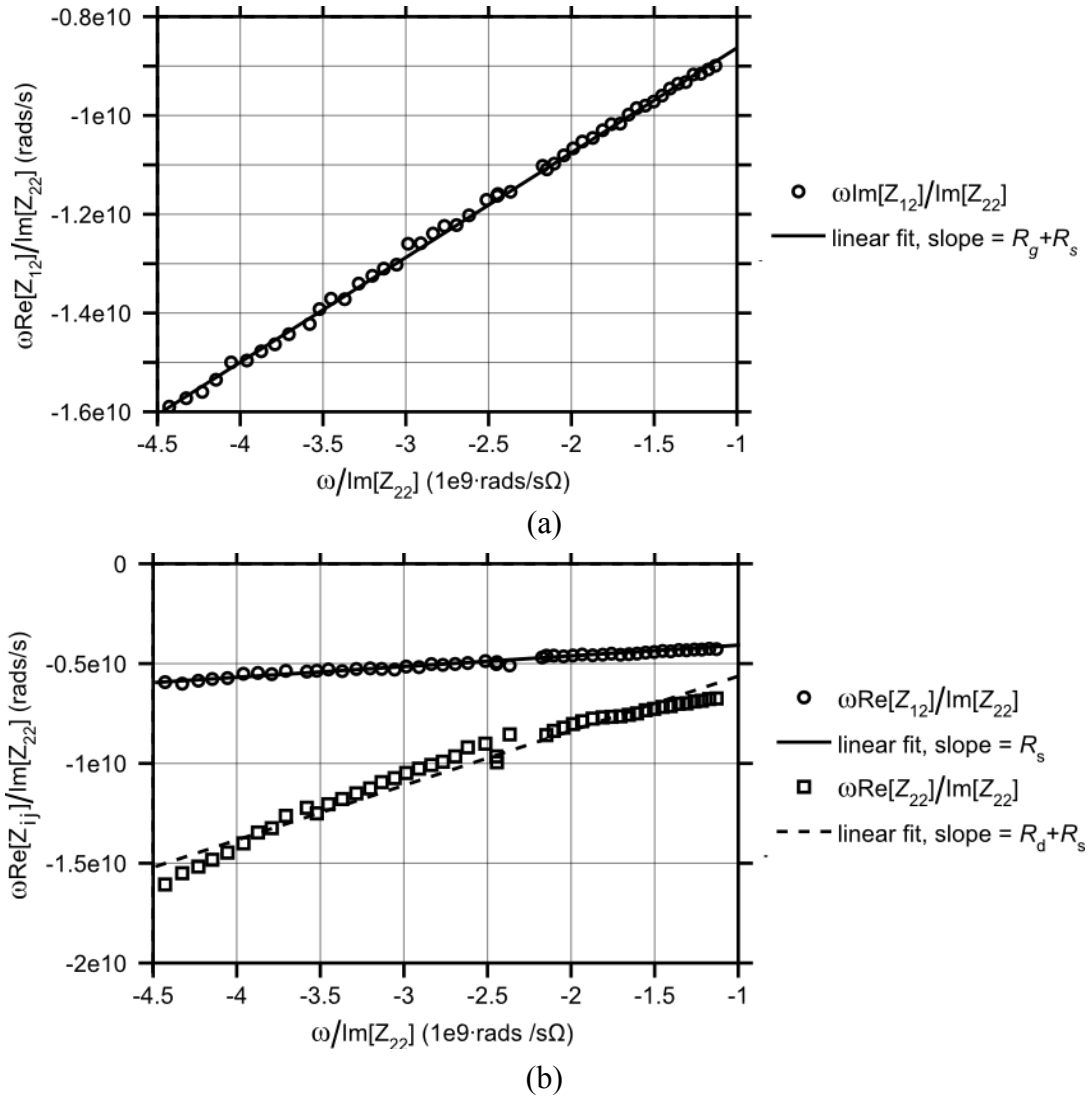


Figure 4.32 Illustration of the extraction of extrinsic resistance parameters from *cold reverse* S-parameters measurements of the 3.2-mm device. Extraction of (a) R_g+R_s and of (b) R_d+R_s and R_s .

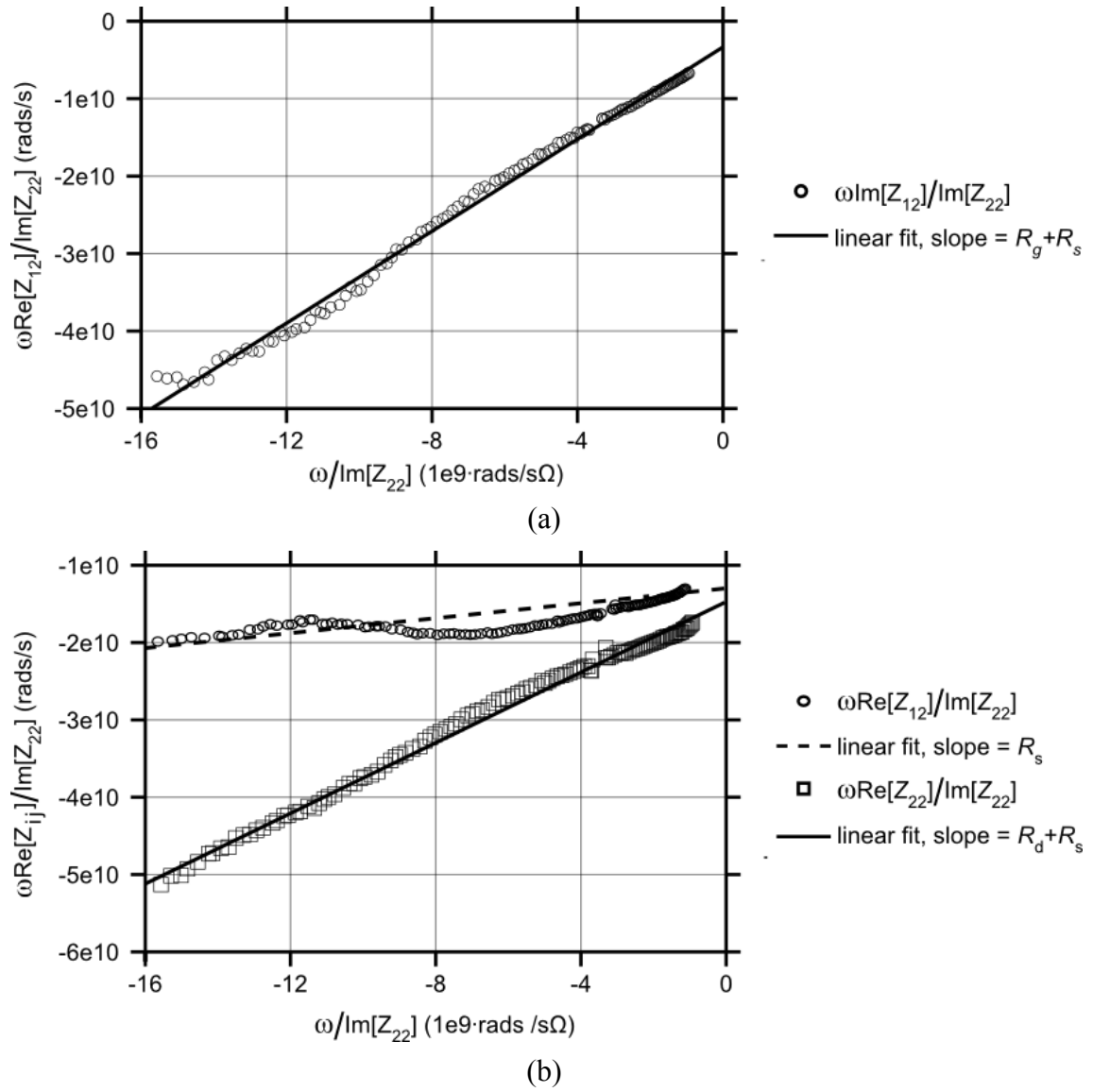


Figure 4.33 Illustration of the extrinsic resistance extraction from *cold reverse* S-parameters measurements applied to the 2-mm device. Extraction of (a) $R_g + R_s$ and of (b) $R_d + R_s$ and R_s .

Table 4.5 Values of the extrinsic resistance parameters obtained using the *cold reverse* S-parameters measurements of the studied large-size devices.

3.2-mm device			2-mm device		
R_g (Ω)	R_d (Ω)	R_s (Ω)	R_g (Ω)	R_d (Ω)	R_s (Ω)
1.69	2.21	0.50	2.58	1.86	0.39

The sections of this subchapter have presented the extrinsic parameter extraction of this thesis. The key aspects to find the capacitance parameter values (the best solution candidate) related to the basic assumptions (the capacitance ratio values) and to the searching method (the sweeps of values) have been explained in detail and have been consistently exemplified with measured data of the studied large-size devices.

4.3 Intrinsic Parameter Extraction

This subchapter explains the parameter extraction for the bias-dependent intrinsic parameters of the small-signal model (the circuit shown in Figure 4.1, p. 63).

After calculating the extrinsic parameter values, their effects are subtracted from S-parameters measurements at each bias point of interest, to obtain the Y-parameters matrix of the intrinsic transistor, which is called here $[Y^{Int}]$. The subtraction process, known also as de-embedding, is carried out using the following equation:

$$[Y^{total}] = \left\langle \left\{ ([Y^{Int}]^{-1} + [R^{ext}])^{-1} + [C^{ext-i}] \right\}^{-1} + [L^{ext}]^{-1} \right\rangle^{-1} + [C^{ext-p}] \quad (4.42)$$

Where $[Y^{total}]$ is obtained from the measured S-parameters by the formulae of S- to Y-parameter conversion, the matrixes $[C^{ext-i}]$, $[L^{ext}]$ and $[C^{ext-p}]$ were given in equations (4.37) to (4.39) of the previous section, and the matrix $[R^{ext}]$ is expressed by the following equation.

$$R^{ext} = \begin{bmatrix} R_g + R_s & R_s \\ R_s & R_d + R_s \end{bmatrix} \quad (4.43)$$

The intrinsic transistor is formulated as four branch admittances: Y_{gs} , Y_{gd} , Y_{gm} and Y_{ds} , with the electric circuit shown in Figure 4.34.

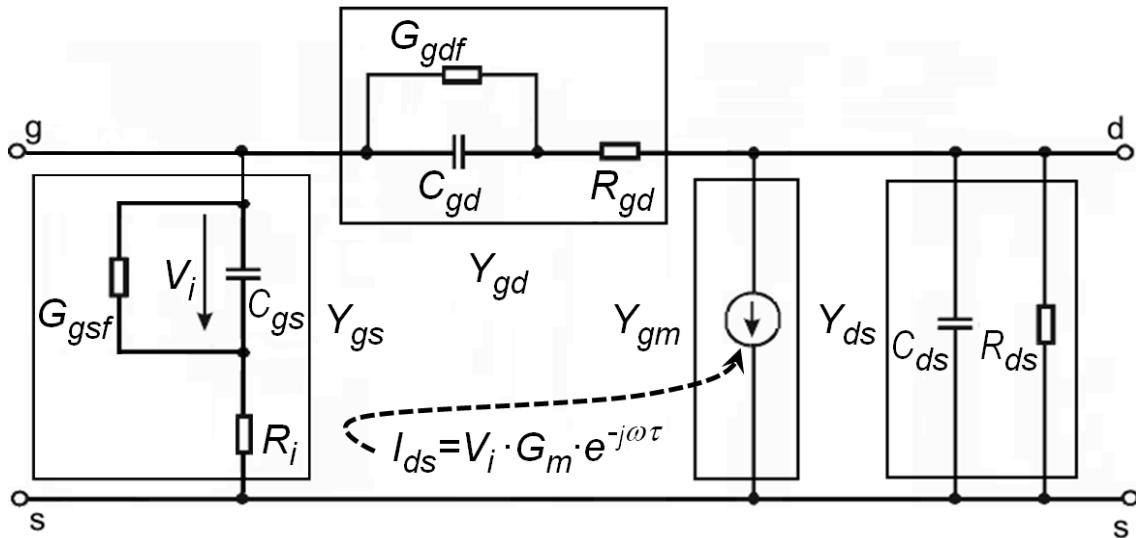


Figure 4.34 Intrinsic transistor equivalent circuit formulated with admittance branches.

These branch admittances of this equivalent circuit are related to the intrinsic admittance matrix $[Y^{Int}]$ and the circuit elements as follows:

$$Y_{gs} = Y_{11}^{Int} + Y_{12}^{Int} = \frac{G_{gsf} + j\omega C_{gs}}{1 + R_i G_{gsf} + j\omega R_i C_{gs}} \quad (4.44)$$

$$Y_{gd} = -Y_{12}^{Int} = \frac{G_{gdf} + j\omega C_{gd}}{1 + R_{gd} G_{gdf} + j\omega R_{gd} C_{gd}} \quad (4.45)$$

$$Y_{gm} = Y_{21}^{Int} - Y_{12}^{Int} = \frac{G_m e^{-j\omega \tau}}{1 + R_i G_{gsf} + j\omega R_i C_{gs}} \quad (4.46)$$

$$Y_{ds} = Y_{22}^{Int} + Y_{12}^{Int} = G_{ds} + j\omega C_{ds} \quad (4.47)$$

The intrinsic parameter extraction presented in [74] for the equivalent circuit adopted in this thesis work has defined a variable D , as

$$D \equiv \frac{|Y_{gs}|^2}{\text{Im}[Y_{gs}]} \approx \frac{G_{gsf}^2}{\omega C_{gs}} + \omega C_{gs} \quad (4.48)$$

Equation (4.48) for D is based on (4.44). The is defined in [74] to obtain C_{gs} by linear data-fitting of ωD in terms ω^2 . However, the expression for D is an approximation. In order to find the conditions of validity of this approximation, equation (4.42) is stated as follows, separating its real and imaginary parts:

$$Y_{gs} = \frac{G_{gsf} (1 + R_i G_{gsf}) + (\omega C_{gs})^2 R_i}{(1 + R_i G_{gsf})^2 + (\omega R_i C_{gs})^2} + j \frac{\omega C_{gs}}{(1 + R_i G_{gsf})^2 + (\omega R_i C_{gs})^2} \quad (4.44a)$$

Then, direct substitution of (4.42a) on the definition of D gives:

$$\begin{aligned} \frac{|Y_{gs}|^2}{\text{Im}[Y_{gs}]} &= \frac{(\text{Re}[Y_{gs}])^2 + (\text{Im}[Y_{gs}])^2}{\text{Im}[Y_{gs}]} = \frac{(\text{Re}[Y_{gs}])^2}{\text{Im}[Y_{gs}]} + \text{Im}[Y_{gs}] \\ &= \frac{[G_{gsf} (1 + R_i G_{gsf}) + (\omega C_{gs})^2 R_i]^2}{\omega C_{gs} [(1 + R_i G_{gsf})^2 + (\omega R_i C_{gs})^2]} + \text{Im}[Y_{gs}] \\ &= \frac{[G_{gsf} (1 + R_i G_{gsf}) + (\omega C_{gs})^2 R_i]^2 + (\omega C_{gs})^2}{\omega C_{gs} [(1 + R_i G_{gsf})^2 + (\omega R_i C_{gs})^2]} \end{aligned} \quad (4.49)$$

Equation (4.49) becomes (4.48) when $R_i G_{gsf} \ll 1$ and $(\omega C_{gs} R_i)^2 \ll 1$, as deduced by visual inspection. Under those considerations, equation (4.48) can be reliably fitted with a straight line (ωD versus ω^2) and C_{gs} is obtained as the slope, as demonstrated by Figure 4.35 taken from [74].

Note that the frequency range of the linear data-fitting shown in Figure 4.35 is 0.32 to 0.47 MHz (ω^2 ranges from 4.25×10^{12} to 8.9×10^{12} rad²/s²). Besides, the corresponding bias point is $V_{DS} = 20V$ and $V_{GS} = -2V$, where the gate-source diode effect is reverse biased and the related conductance G_{gsf} is considered negligible.

Therefore, the conditions $R_i G_{gsf} \ll 1$ and $(\omega C_{gs} R_i)^2 \ll 1$ are satisfied and equation (4.48) is valid to obtain C_{gs} using linear data-fitting.

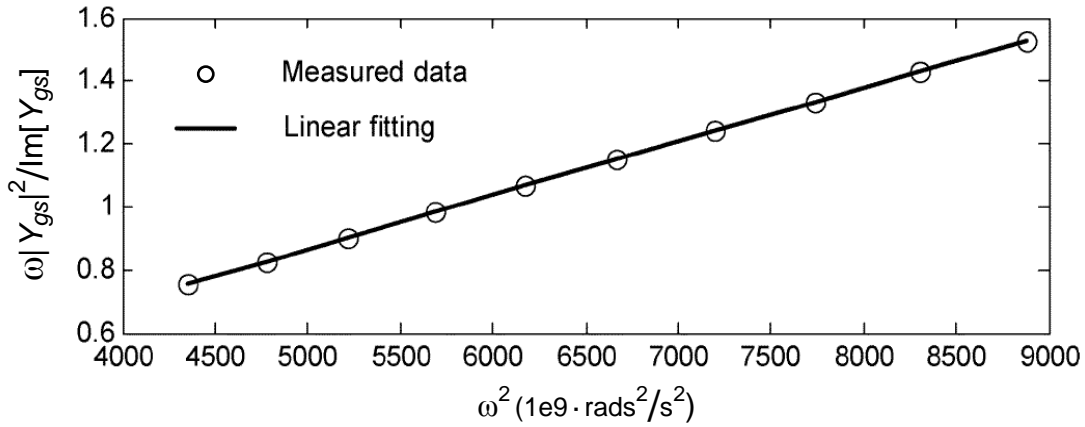


Figure 4.35 Linear data fitting of the measured data for the defined variable D ($V_{DS} = 20V$, $V_{GS} = -2V$), taken from [74]. It supports the use of D to obtain C_{gs} from the slope.

A similar equation to (4.48) is formulated in terms of Y_{gd} , C_{gd} and G_{gdf} as follows:

$$\omega \frac{|Y_{gd}|^2}{\text{Im}[Y_{gd}]} = \frac{G_{gdf}^2}{C_{gd}} + \omega^2 C_{gd} \quad (4.50)$$

With the considerations that $R_{gd} G_{gdf} \ll 1$ and $(\omega C_{gd} R_{gd})^2 \ll 1$, C_{gd} is obtained by linear data-fitting of equation (4.50).

The following two equations are deduced from (4.44) and (4.45) by direct substitution of the corresponding real and imaginary parts, without any specific assumption.

$$\omega \frac{\text{Re}[Y_{gs}]}{\text{Im}[Y_{gs}]} = \frac{G_{gsf} (1 + R_i G_{gsf})}{C_{gs}} + \omega^2 C_{gs} R_i \quad (4.51)$$

$$\omega \frac{\text{Re}[Y_{gd}]}{\text{Im}[Y_{gd}]} = \frac{G_{gdf}(1 + R_{gd}G_{gdf})}{C_{gd}} + \omega^2 C_{gd} R_{gd} \quad (4.52)$$

The linear approximation of measured data for (4.51) with respect to $\omega^2 C_{gs}$ gives the value of R_i as the slope. The value of R_{gd} is obtained similarly with the measured data of equation (4.52) with respect to $\omega^2 C_{gd}$.

According to equations (4.44) and (4.45), the real parts of Y_{gs} and Y_{gd} are expressed as follows:

$$\text{Re}[Y_{gs}] = \frac{G_{gsf}(1 + R_i G_{gsf}) + \omega^2 C_{gs}^2 R_i}{(1 + R_i G_{gsf})^2 + \omega^2 C_{gs}^2 R_i^2} \quad (4.53)$$

$$\text{Re}[Y_{gd}] = \frac{G_{gdf}(1 + R_{gd} G_{gdf}) + \omega^2 C_{gd}^2 R_{gd}}{(1 + R_{gd} G_{gdf})^2 + \omega^2 C_{gd}^2 R_{gd}^2} \quad (4.54)$$

The values of G_{gsf} and G_{gdf} are obtained using the calculated values of R_i and R_{gd} and the data of $\text{Re}[Y_{gs}]$ and $\text{Re}[Y_{gd}]$ at low frequencies, typically in the 100-MHz range or below, where the frequency varying terms vanish.

The following two equations are deduced from combinations of equations (4.44) and (4.46) without any specific assumption:

$$\left| \frac{Y_{gs}}{Y_{gm}} \right|^2 = \left(\frac{G_{gsf}}{G_m} \right)^2 + \left(\frac{1}{G_m} \right)^2 \omega^2 C_{gs}^2 \quad (4.55)$$

$$\text{phase} \left\{ j\omega C_{gs} \frac{Y_{gs}}{Y_{gm}} \right\} = -j\omega \tau \quad (4.56)$$

Then, the value of G_m is given by the slope of the linear approximation of the measured data related to equation (4.55) with respect to $\omega^2 C_{gs}^2$. The value of τ is obtained as the slope of the linear approximation of the measured data related to equation (4.56) with respect to ω .

Equation (4.47) indicates that C_{ds} is given by the slope of the linear approximation of the measured data related to $\text{Im}[Y_{ds}]$ with respect to ω . Also from that equation, G_{ds} is obtained from the real part of $[Y_{ds}]$ ($G_{ds} = 1/R_{ds}$).

4.4 Scalability of the Small-Signal Model

In measurement-based models, scalability is an important tool to model large-size devices, whose power/current/voltage limits overcome the limits of the measurement equipment employed for database acquisition.

The increase of device size seeks to enhance the power performance by either increasing the gate electrode width w_{f_g} , the number of these electrodes n_{f_g} , or both. Therefore, in this thesis work the scaling of small-signal parameters is formulated with a rule in terms of w_{f_g} and another rule in terms of n_{f_g} . The next approaches are proposed to verify the small-signal model scalability:

1. Generation of a scaled model for a device using the scaling rules in terms of w_{f_g} and comparison of model simulations with simulations of a model extracted directly from measurements.
2. Generation of a scaled model for a device using the scaling rules in terms of n_{f_g} and comparison of model simulations with simulations of a model extracted directly from measurements.
3. Generation of a scaled model for a device size using both scaling rules and comparison of model simulations of with simulations of a model extracted directly from measurements.

4.4.1 Scaling Rules in Terms of the Gate Electrode Width

The following scaling rules assume that, except for the scaling of w_{f_g} , the finger layout has been preserved. In this thesis work, finger layouts are considered preserved if they retain the following features:

- Length and number of the gate, drain and source electrodes.
- Top-view areas of the bus bars and contacting pads.
- Number, location and dimensions of the air bridges.
- Type and length dimension of the field-plate structures.

Effects of the scaling of w_{f_g} on the finger layout can be illustrated by comparing the photos shown in (a) and (b) of Figure 4.17. In the two devices depicted on those images the finger layout is considered preserved.

The physical meanings of C_{pgd} , C_{pds} and C_{pgs} considered in this thesis work indicate that these parameters do not vary with the scaling of w_{fg} , because they denote capacitive effects related to features that are retained when the finger layout is preserved. The parameter τ is also thought to remain constant with respect to the scaling of w_{fg} .

According to their physical interpretation, the remaining capacitance parameters C_{gdi} , C_{gsi} , C_{dsi} , C_{gd} , C_{gs} and C_{ds} , the inductance parameters L_g , L_s , L_d , the extrinsic resistance parameter R_g and the transconductance G_m are expected to scale in direct proportion to the scaling of w_{fg} .

On another hand, the extrinsic resistance parameters R_s and R_d are considered to scale in inverse proportion to the scaling of w_{fg} , which means, that their reciprocals $1/R_s$ and $1/R_d$ do scale in direct proportion.

In consequence, the scaling rule in terms of w_{fg} applicable to the small-signal model parameters is expressed by

$$f(\text{scaled } w_{fg}) \approx f(\text{initial } w_{fg}) \frac{\text{scaled } w_{fg}}{\text{initial } w_{fg}} \quad (4.57)$$

where f represents C_{gdi} , C_{gsi} , C_{dsi} , C_{gd} , C_{gs} , C_{ds} , L_g , L_s , L_d , G_m , R_g , $1/R_s$ or $1/R_d$.

Note that R_g does not follow the same scaling rule in terms of w_{fg} as the other extrinsic resistance parameters R_s and R_d . The reason is that the parasitic resistance effect denoted by R_g increases with extension of the metal strip from the gate contacting pad to the gate electrode end [8, 64, 76, 96, 97], i.e. with the increase of w_{fg} . This is opposite to the contact- and bulk-resistivity effects denoted by R_s and R_d that decrease with the increase of w_{fg} .

4.4.2 Scaling Rules in Terms of the Gate Electrode Number

Effects of the scaling of n_{fg} on the finger layout can be illustrated by comparing the photographs shown Figure 4.36. The one at the top corresponds to a 2-finger device and the one at the bottom to an 8-finger, but in both cases w_{fg} is the same (as highlighted in the figure) and both

devices are from the same manufacturer and fabrication process. So the marked in the finger layout are due to scaling of n_{f_g} .

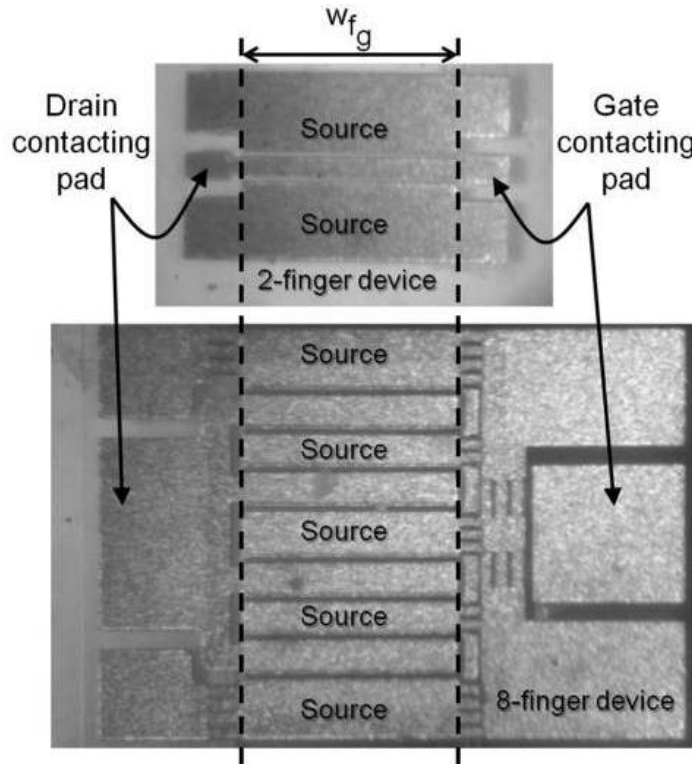


Figure 4.36 Example of change of the finger layout due to the scaling of n_{f_g} from (top image) 2 fingers to (bottom image) 8 fingers. Both are IAF devices with $w_{f_g} = 0.4$ mm from the same wafer fragment, i.e. same fabrication process.

Source air bridges, bus bars and contacting pads are finger layout features that change with the scaling of n_{f_g} . However, extrinsic parameters denoting parasitic effects due to those features, C_{pds} and C_{pgs} , are not related directly to n_{f_g} in their approximate expressions, equations (4.1) and (4.2), which were presented in section 4.1.2.

The scaling of n_{f_g} originates changes of the horizontal areas of the finger layout, like A_{p+b_g} and A_{p+b_d} , and then, these changes are what actually modifies the parasitic capacitive effects related to and the extracted values of C_{pds} and C_{pgs} .

C_{pgs} and C_{pds} depend on top-view areas with three components: (i) air bridges, (ii) contacting pads, and (iii) bus bars. The proportionality of these area components with respect to n_{f_g} is case-specific, especially if the scaling of n_{f_g} starts from two electrodes, as in the example shown in Figure 4.36, from two to eight electrodes.

Thus, the indirect and case-specific relation, inhibits the setting up of straightforward scaling rules for C_{pds} and C_{pgs} in terms of the scaling of n_{fg} , in the form of $f(\text{scaled}) = f(\text{initial}) \cdot \text{ratio}_{\text{scaling}}$, as the rules formulated in the previous section in terms of w_{fg} .

On another hand, C_{pgd} is directly proportional with the number of drain electrodes n_{fd} , as explicitly given in equation (4.3) of section 4.1.2. Since n_{fg} is typically $2 \cdot n_{fd}$, C_{pgd} is expected to scale in direct proportion to the scaling of n_{fg} .

Based on their physical meanings, the remaining capacitance parameters of the model C_{gdi} , C_{gsi} , C_{dsi} , C_{gd} , C_{gs} , C_{ds} , the inductance parameters L_g , L_s , L_d , and the transconductance parameter G_m are expected to scale in direct proportion to the scaling of n_{fg} .

On another hand, the physical meanings of the extrinsic and intrinsic resistance parameters indicate that they scale in inverse proportion to the scaling of n_{fg} , and thus, their reciprocals scale in direct proportion.

In consequence, the scaling rule in terms of n_{fg} applicable to the small-signal model parameters is expressed by

$$f(\text{scaled } n_{fg}) \approx f(\text{initial } n_{fg}) \frac{\text{scaled } n_{fg}}{\text{initial } n_{fg}} \quad (4.58)$$

where f represents C_{pgd} , C_{gdi} , C_{gsi} , C_{dsi} , C_{gd} , C_{gs} , C_{ds} , L_g , L_s , L_d , G_m , $1/R_g$, $1/R_s$ or $1/R_d$.

The parameter τ is considered constant with respect to the scaling of n_{fg} .

Chapter 5

Results of Small-Signal Modeling

The small-signal model was implemented in Matlab[®] for the verification tests with S-parameters presented here. The matrix of S-parameters of the complete model is constructed from the Y-parameter matrix $[Y^{total}]$, applying the formulae for conversion from Y- to S-parameters. That matrix is calculated using equation (4.42) of the previous chapter when all the model parameters are known.

5.1 Results of Extrinsic Parameter Extraction

5.1.1 Optimal Frequency Range of the Extraction

In reference [76], the extrinsic parameter extraction of the adopted small-signal model was applied reliably with a frequency range of S-parameter measurements that depended on the device size, i.e. on the gate periphery. The relation between optimal frequency range of extraction and gate periphery found in [76] is depicted in Figure 5.1.

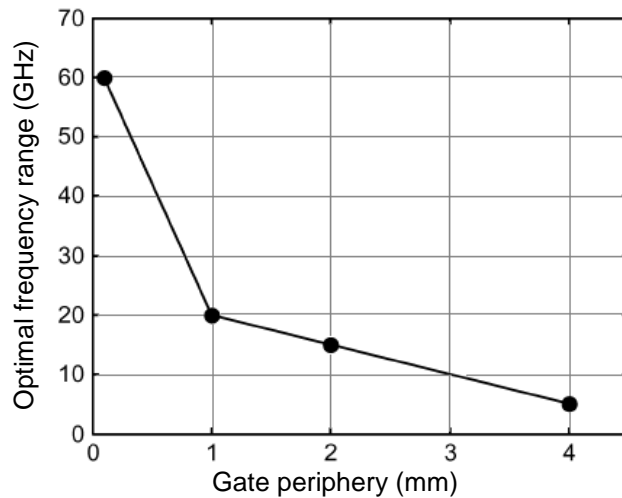


Figure 5.1 Optimal frequency range of S-parameter measurements, for their usage to extract extrinsic parameters of the adopted small-signal model, in terms of the gate periphery of the modeled device, as given in [76].

The extrinsic parameter extraction of this thesis was expected to exhibit a similar relation between optimal frequency range and device size. To verify this, the extraction was applied with different frequency ranges of the S-parameters measurements.

The resulting extracted values of drain-source and gate-source capacitance parameters with respect to the frequency range of extraction are shown in Figure 5.3 for the 3.2-mm device and in Figure 5.3 for the 2-mm device.

These results indicate that the optimal frequency ranges are between 8 and 10 GHz and between 14 and 17 GHz, respectively, for the studied large-size devices. These frequency ranges agree well with the values that could be expected from the inspection of Figure 5.1.

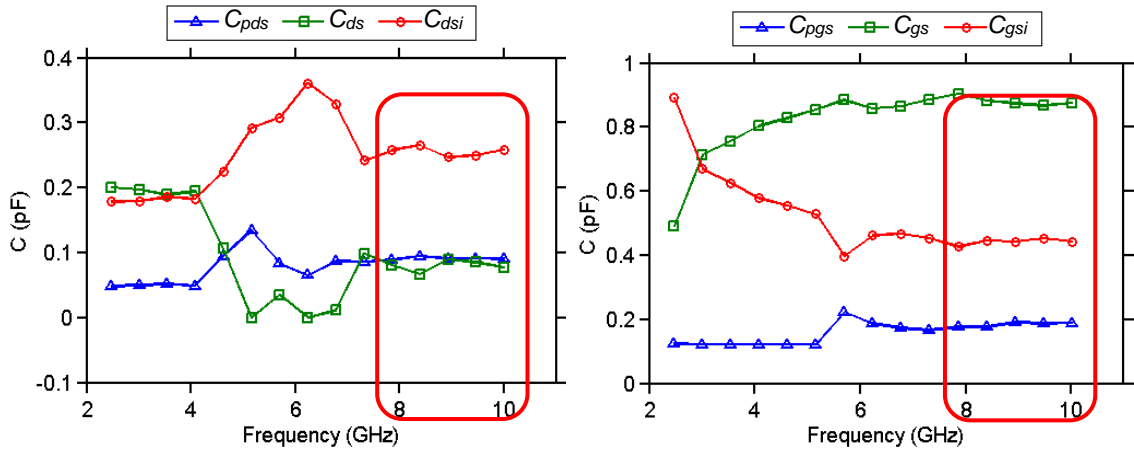


Figure 5.2 Values of drain-source (left) and gate-source (right) capacitance parameters extracted for the model of the 3.2-mm device with different frequency ranges of the S-parameters data. The optimal frequency range is highlighted

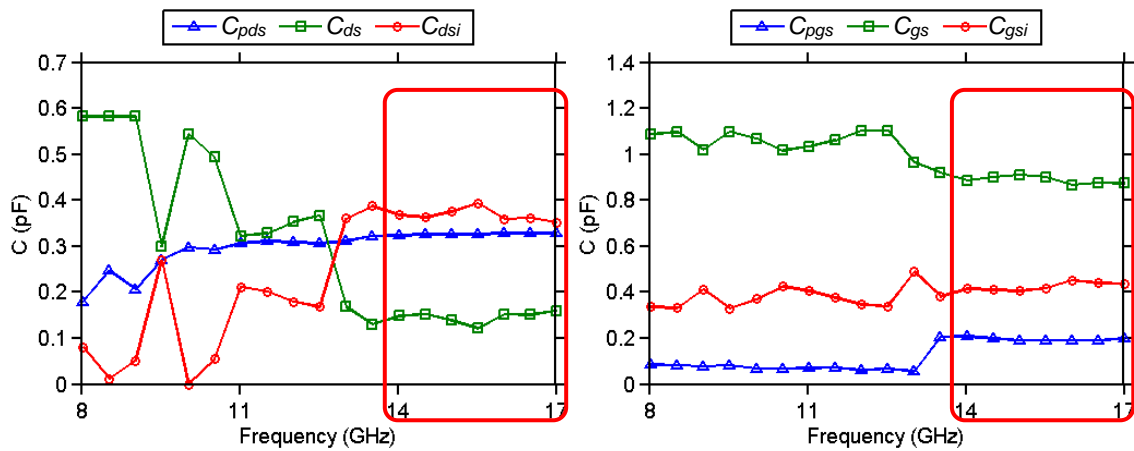


Figure 5.3 Values of drain-source (left) and gate-source (right) capacitance parameters extracted for the model of the 2-mm device with different frequency ranges of the S-parameters data. The optimal frequency range is highlighted.

5.1.2 Starting and Optimized Values of the Extrinsic Parameters

Chapter 4 presented the extrinsic parameter extraction of model and exemplified the procedure with measured data of the 3.2-mm and the 2-mm devices. The frequency ranges used in those examples of extraction were 10 and 16 GHz, respectively, which is in accordance with the optimal ranges specified in the previous section. Table 4.3 and Table 4.4 of Chapter 4 listed model parameter values extracted using the capacitance ratio values generated from top-view images, the proposed 4-parameter sweeps and the *cold pinch-off* S-parameters measurements. Table 4.5 listed the values of extrinsic resistance parameters extracted from measurements of *cold reverse* S-parameters. The parameter values of those tables are summarized in the following Table 5.1.

Table 5.1 High-quality measurement-correlated values extracted for the model in cold *pinch-off* conditions taken as starting point of the refining optimization process.

3.2-mm device		2-mm device	
Extrinsic Parameters	Intrinsic Parameters	Extrinsic Parameters	Intrinsic Parameters
$C_{pgs} = 201.38 \text{ fF}$	$C_{gs} = 579.14 \text{ fF}$	$C_{pgs} = 190.60 \text{ fF}$	$C_{gs} = 875.42 \text{ fF}$
$C_{gsi} = 523.17 \text{ fF}$	$C_{ds} = 77.89 \text{ fF}$	$C_{gsi} = 442.74 \text{ fF}$	$C_{ds} = 353.29 \text{ fF}$
$C_{pds} = 99.74 \text{ fF}$	$C_{gd} = 1614.98 \text{ fF}$	$C_{pds} = 157.02 \text{ fF}$	$C_{gd} = 875.42 \text{ fF}$
$C_{dsi} = 259.33 \text{ fF}$	$R_i = 0.00 \text{ } \Omega$	$C_{dsi} = 329.75 \text{ fF}$	$R_i = 0.53 \text{ } \Omega$
$C_{pgd} = 8.96 \text{ fF}$	$R_{gd} = 0.00 \text{ } \Omega$	$C_{pgd} = 0.00 \text{ fF}$	$R_{gd} = 0.00 \text{ } \Omega$
$C_{gdi} = 123.10 \text{ fF}$	$G_{ds} = 0.00 \text{ mS}$	$C_{gdi} = 0.00 \text{ fF}$	$G_{ds} = 0.00 \text{ mS}$
$L_g = 90.10 \text{ pH}$	$G_m = 0.00 \text{ mS}$	$L_g = 42.38 \text{ pH}$	$G_m = 0.00 \text{ mS}$
$L_d = 187.27 \text{ pH}$	$G_{gsf} = 0.00 \text{ mS}$	$L_d = 77.19 \text{ pH}$	$G_{gsf} = 0.00 \text{ mS}$
$L_s = 0.59 \text{ pH}$	$G_{gdf} = 0.00 \text{ mS}$	$L_s = 17.12 \text{ pH}$	$G_{gdf} = 0.00 \text{ mS}$
$R_g = 1.69 \text{ } \Omega$	$\tau = 0.00 \text{ ps}$	$R_g = 2.58 \text{ } \Omega$	$\tau = 0.00 \text{ ps}$
$R_d = 2.21 \text{ } \Omega$		$R_d = 1.86 \text{ } \Omega$	
$R_s = 0.50 \text{ } \Omega$		$R_s = 0.39 \text{ } \Omega$	

The values tabulated above are measurement-correlated and their good quality is demonstrated by the agreements that they produce between simulated S-parameters and measurements in *cold pinch-off*, which are shown in Figure 5.4 and Figure 5.5 for the studied large-size devices.

Thus, those values are taken as high-quality starting values of an optimization routine of refinement. A similar routine was utilized as in [74], which only varies the extrinsic elements, and which uses a modified *simplex* optimization algorithm, originally presented in [59]. The objective error function was described in section 4.2.4 by equation (4.24).

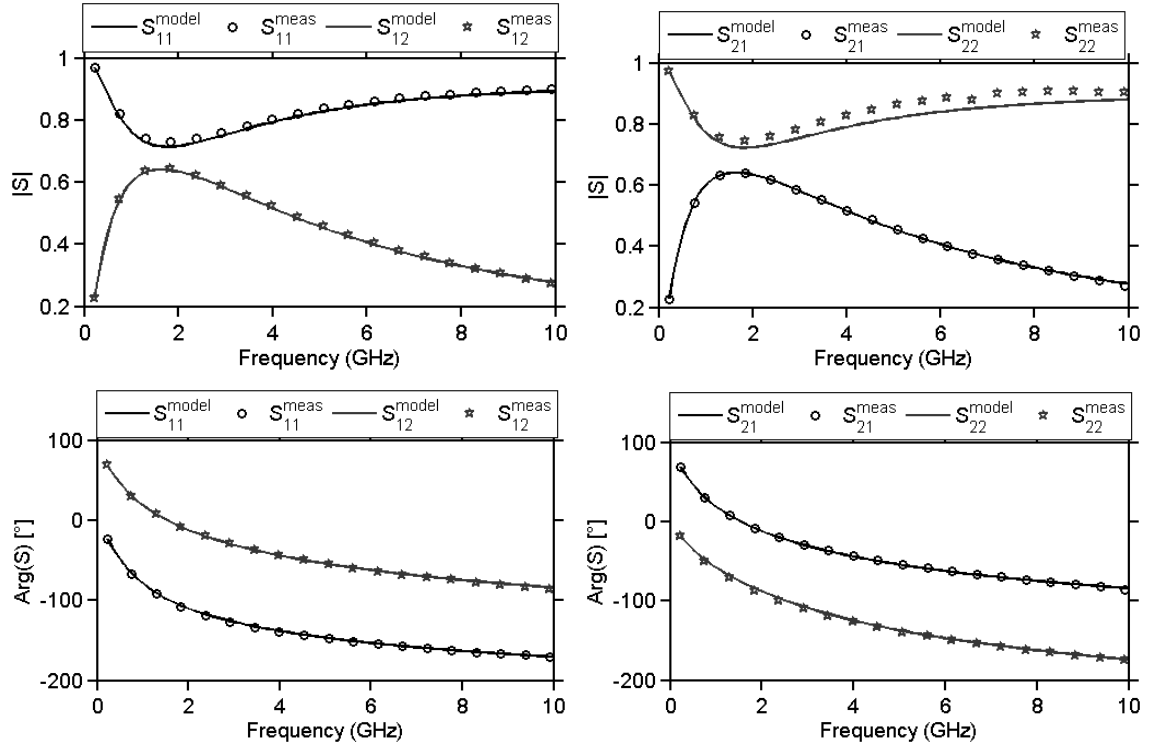


Figure 5.4 S-parameters measured in *cold pinch-off* of the 3.2-mm device (markers) compared with the simulations (lines) produced with the high-quality starting values of model parameters given in Table 5.1.

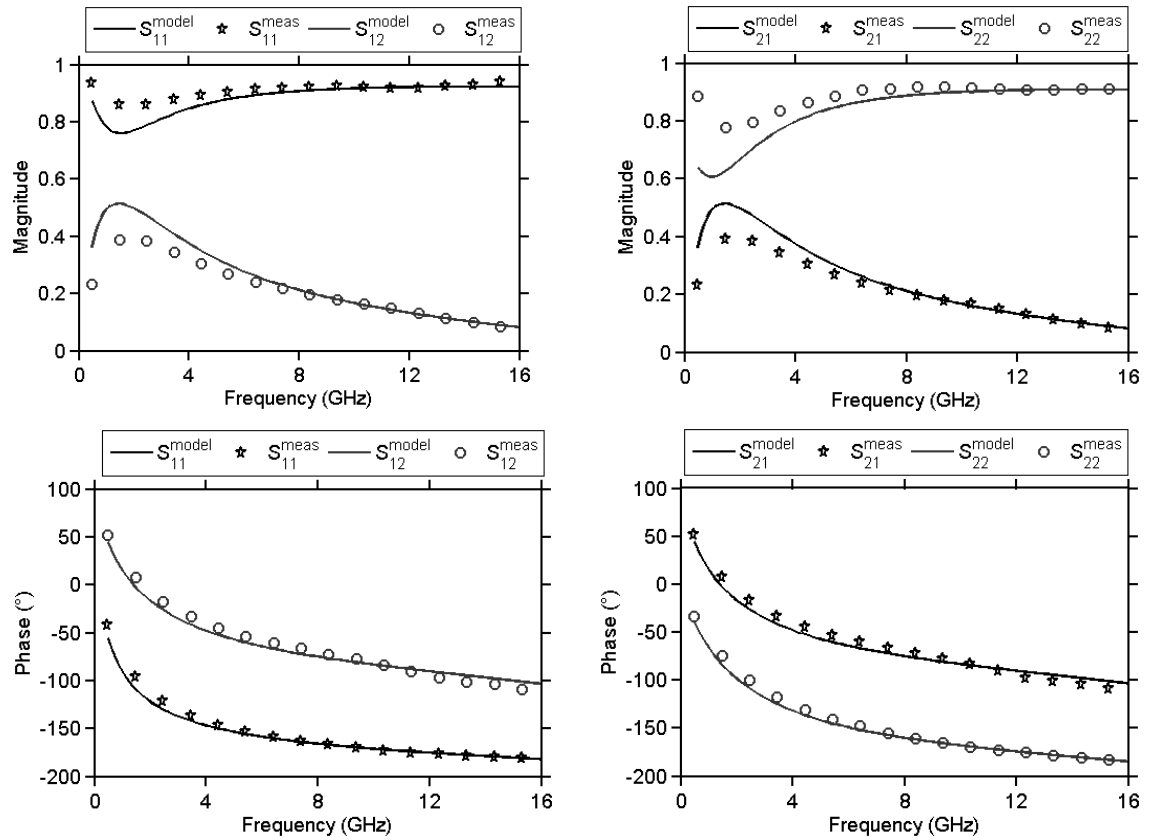


Figure 5.5 S-parameters measured in *cold pinch-off* of the 2-mm device (markers) compared with the simulations (lines) produced with the high-quality starting values of model parameters given in Table 5.1.

The model parameter values obtained after optimization are listed in Table 5.2 for the studied large-size devices. The similarity with the values of the previous table underlines the high-quality of the starting values.

Table 5.2 Optimized parameter values for the model in cold *pinch-off* conditions

3.2-mm device		2-mm device	
Extrinsic Parameters	Intrinsic Parameters	Extrinsic Parameters	Intrinsic Parameters
$C_{pgs} = 203.87 \text{ fF}$	$C_{gs} = 603.86 \text{ fF}$	$C_{pgs} = 232.04 \text{ fF}$	$C_{gs} = 1037.21 \text{ fF}$
$C_{gsi} = 567.27 \text{ fF}$	$C_{ds} = 119.46 \text{ fF}$	$C_{gsi} = 392.99 \text{ fF}$	$C_{ds} = 150.33 \text{ fF}$
$C_{pds} = 115.48 \text{ fF}$	$C_{gd} = 1581.37 \text{ fF}$	$C_{pds} = 238.48 \text{ fF}$	$C_{gd} = 1021.54 \text{ fF}$
$C_{dsi} = 213.15 \text{ fF}$	$R_i = 1.63 \text{ } \Omega$	$C_{dsi} = 319.51 \text{ fF}$	$R_i = 0.00 \text{ } \Omega$
$C_{pgd} = 10.21 \text{ fF}$	$R_{gd} = 0.00 \text{ } \Omega$	$C_{pgd} = 0.00 \text{ fF}$	$R_{gd} = 0.00 \text{ } \Omega$
$C_{gdi} = 130.87 \text{ fF}$	$G_{ds} = 50.08 \text{ mS}$	$C_{gdi} = 0.00 \text{ fF}$	$G_{ds} = 3.69 \text{ mS}$
$L_g = 83.89 \text{ pH}$	$G_m = 0.00 \text{ mS}$	$L_g = 49.81 \text{ pH}$	$G_m = 0.00 \text{ mS}$
$L_d = 168.26 \text{ pH}$	$G_{gsf} = 0.00 \text{ mS}$	$L_d = 99.62 \text{ pH}$	$G_{gsf} = 0.32 \text{ mS}$
$L_s = 8.22 \text{ pH}$	$G_{gdf} = 0.00 \text{ mS}$	$L_s = 17.83 \text{ pH}$	$G_{gdf} = 0.00 \text{ mS}$
$R_g = 1.60 \text{ } \Omega$	$\tau = 0.00 \text{ ps}$	$R_g = 2.68 \text{ } \Omega$	$\tau = 0.00 \text{ ps}$
$R_d = 2.05 \text{ } \Omega$		$R_d = 2.29 \text{ } \Omega$	
$R_s = 0.14 \text{ } \Omega$		$R_s = 0.31 \text{ } \Omega$	

5.2 Results of Intrinsic Parameter Extraction

The measured behavior that corresponds to the intrinsic transistor is readily determined after de-embedding the extrinsic parameters of the model. The de-embedding procedure is based on equation (4.42) and gives the Y-parameter matrix of the intrinsic transistor $[Y^{Int}]$, as outlined in subchapter 4.3. The following results of intrinsic parameter extraction are obtained using the optimized values of the extrinsic parameters reported in the previous Table 5.2 for the studied large-size devices.

5.2.1 Frequency and Bias Dependency of Intrinsic Parameters

The extraction of the bias-dependent intrinsic parameters of the small-signal model, in terms of the admittance matrix of the intrinsic transistor, $[Y^{Int}]$, was explained in subchapter 4.3. Most of the intrinsic parameters are obtained by linear approximation of measured data of the branch admittances Y_{gs} , Y_{gd} , Y_{gm} and Y_{ds} (which are in terms of $[Y^{Int}]$).

Figure 5.6 demonstrates that the measured data on active bias points satisfies the linear frequency-dependencies formulated in subchapter 4.3.

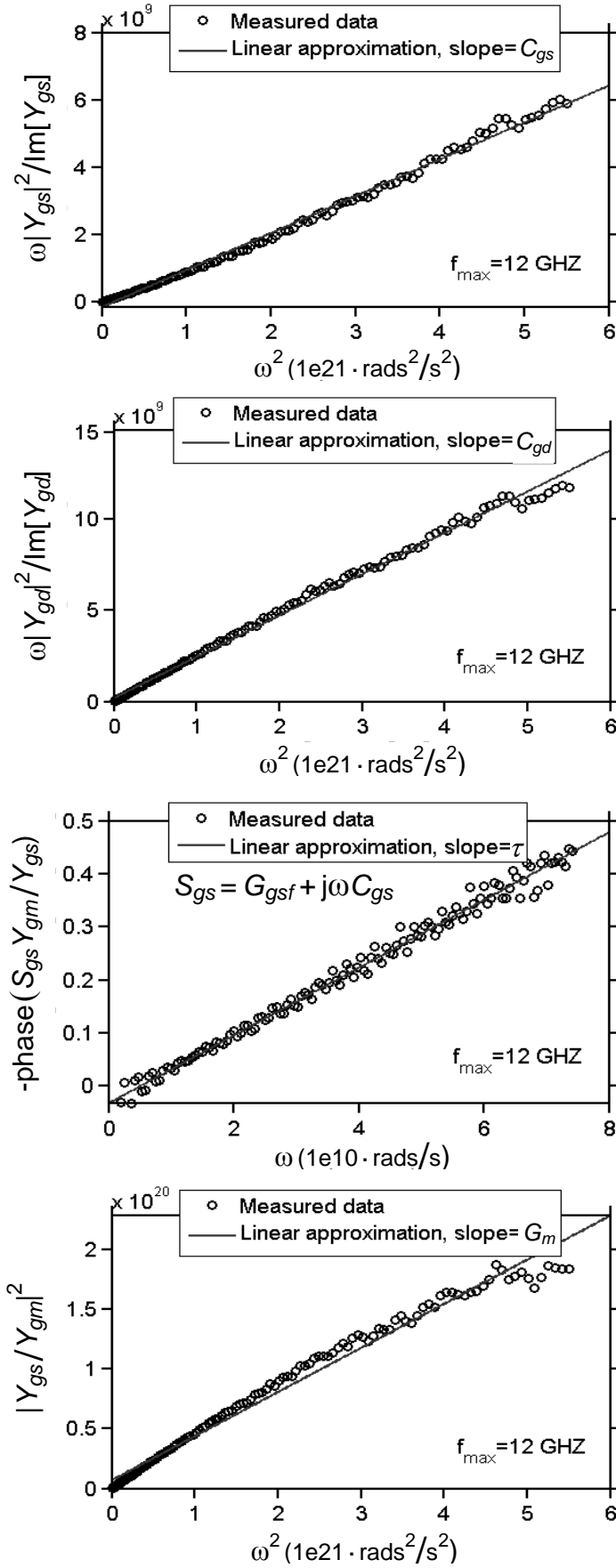


Figure 5.6 Plots of measured data related to the intrinsic transistor used to extract by linear approximation C_{gs} , C_{gd} , τ and G_m , respectively, from S-parameter measurements of the 2-mm device on the active bias point $V_{GS} = -1.5\text{V}$, $V_{DS} = 5\text{V}$.

The adequate frequency-dependency shown in Figure 5.6 by the measured data of the 2-mm device corresponding to the intrinsic parameters is a further validity check of the extracted values of extrinsic parameters. Comparable linear behavior as that shown in Figure 5.6 appears in that type of plots with measured data of the 3.2-mm device, which are not shown here for the sake of brevity.

Figure 5.7 shows the bias-dependency of the intrinsic parameters obtained after carrying out the intrinsic extraction with the S-parameters measured in a multitude of active bias points on the IV plane, for the 2-mm device.

The results for the 3.2-mm device are shown in Figure 5.8. The extracted intrinsic parameters exhibit the expected trends with respect to the bias according to their physical interpretation, as explained in the following paragraphs.

The intrinsic parameters C_{gd} and C_{gs} represent charge storage effects of the gate-drain and gate-source regions between the gate and the 2DEG. With $V_{DS} = 0V$ and V_{GS} decreasing from 0V towards the pinch-off region (approaching the V_{th} value), negative charges at the gate due to the increasingly negative V_{GS} reduce the charge storage in the gate-drain and gate-source regions. The corresponding reductions of C_{gd} and C_{gs} are observed in the extracted values shown in Figure 5.7 and Figure 5.8.

In subsection 3.2.1.3 (S-parameter characterization results), imaginary parts of the Y-matrix of the device measured at low-frequency with $V_{DS} = 0V$ and V_{GS} around the V_{th} value were analyzed to identify $V_{pinch-off}$, and results were shown in Figure 3.9. Those results indicated that with $V_{GS} \approx V_{th}$ and more negative (the pinch-off and deep pinch-off IV regions) the capacitive effects in the device turn almost constant at low values, with respect to the V_{GS} variation. This behavior of C_{gd} and C_{gs} is correctly depicted by the extracted values shown in Figure 5.7 and Figure 5.8.

Previous publications, like those in [75] and [98], have reported that with $V_{DS} = 0V$ and V_{GS} increasing from pinch-off towards 0V, C_{gs} rises up to a maximum value, which occurs around the V_{GS} value that corresponds to the maximum transconductance G_m . Beyond that maximum point, C_{gs} will show again a notable increase only when the increasing V_{GS} turns positive [85, 99]. This dependency of C_{gs} with respect to V_{GS} in the low- V_{DS} region is reflected by the extracted values of this parameter shown in Figure 5.7 and Figure 5.8.

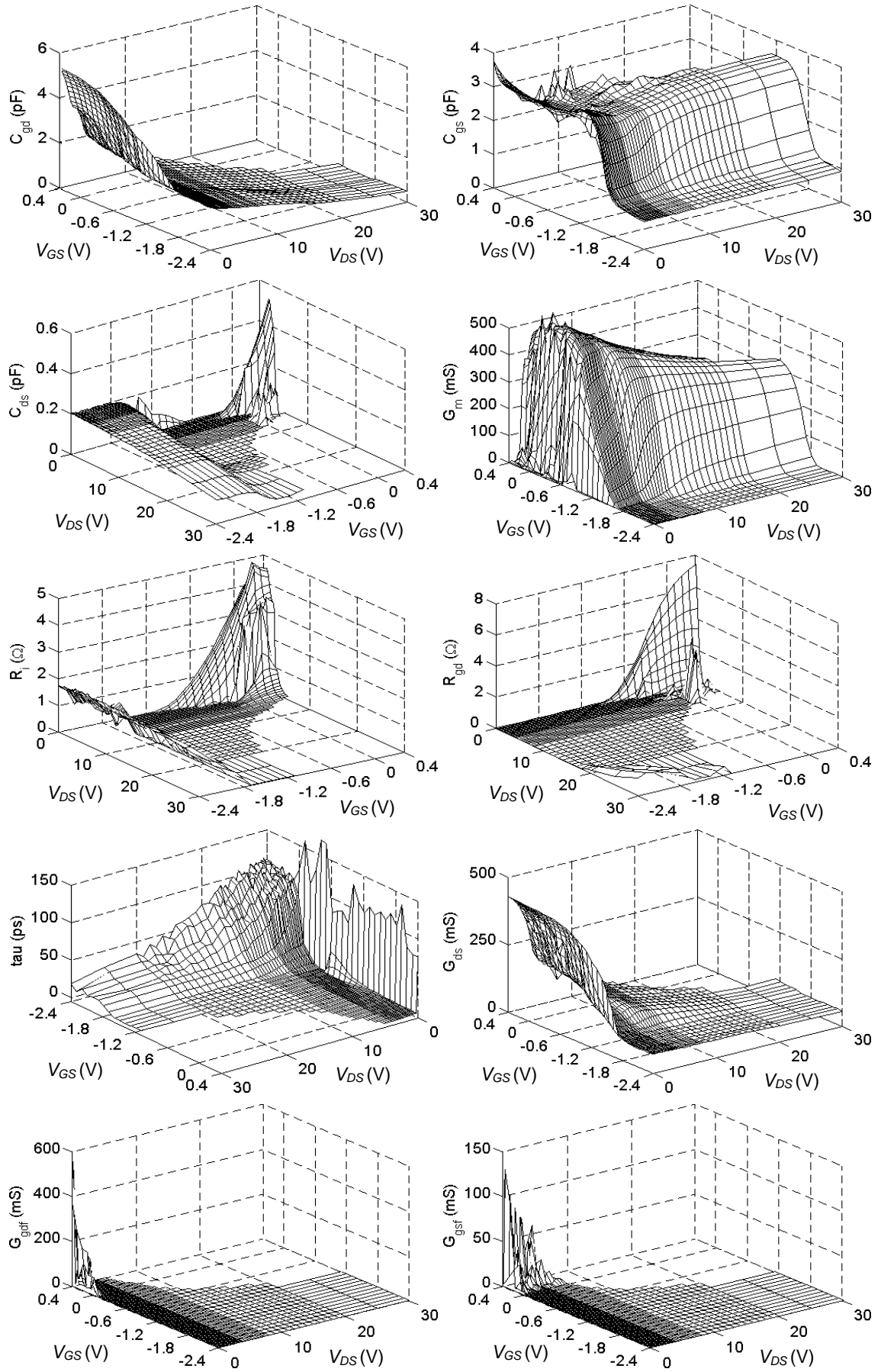


Figure 5.7 Extracted bias-dependency of the 10 intrinsic parameters of the small-signal model for the 2-mm.

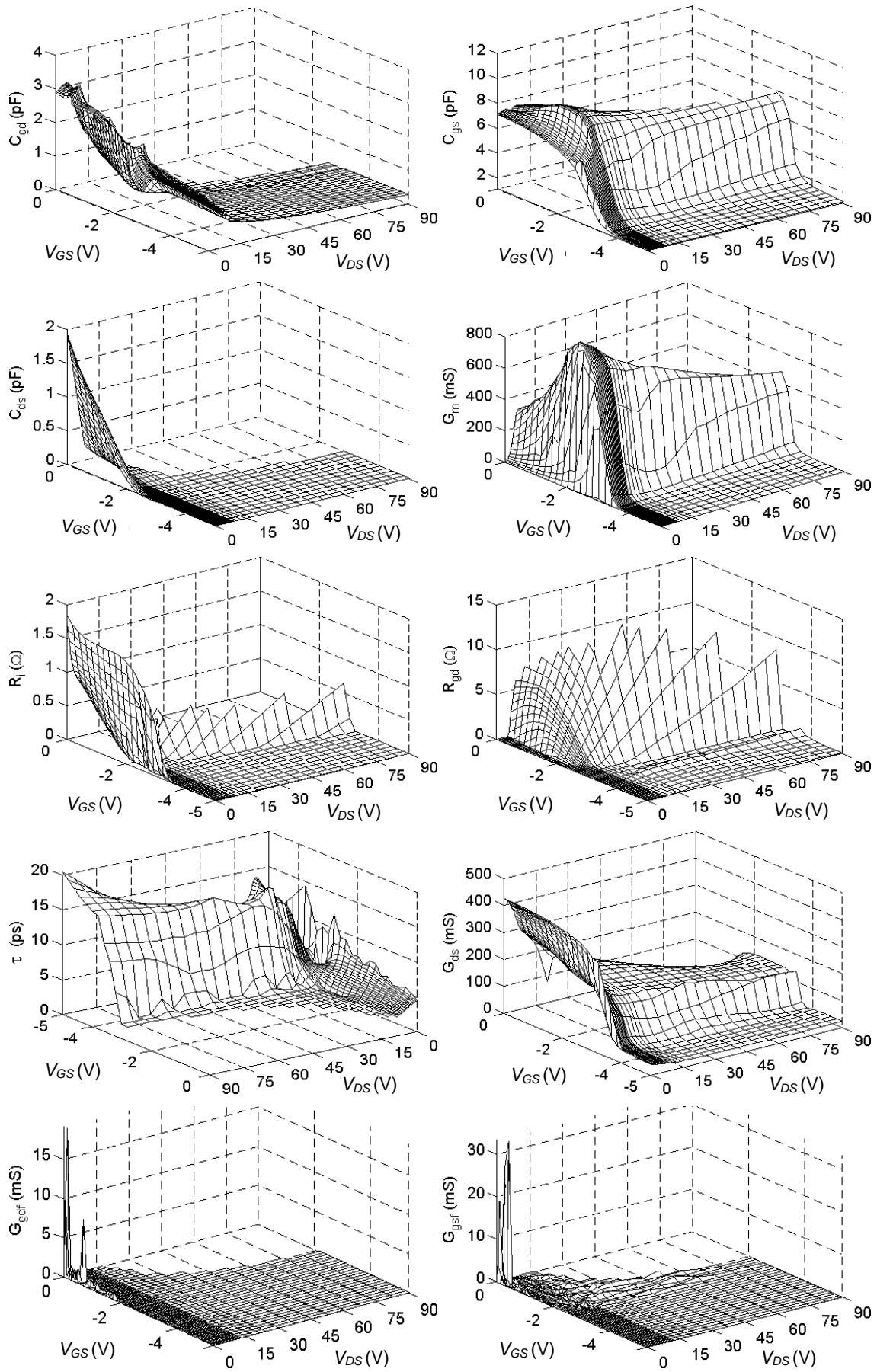


Figure 5.8 Extracted bias-dependency of the 10 intrinsic parameters of the small-signal model for the 3.2-mm device.

With a fixed V_{GS} , increasing V_{DS} from 0V presents positive charges in the drain that hinder the capacitive effects of the gate-drain region, leaving the gate-source region unaffected. Thus, effects denoted by C_{gd} decrease, whereas those denoted by C_{gs} remain roughly constant. These dependencies on V_{DS} are correctly portrayed by the extracted values of this parameter.

The parameter C_{ds} represents the geometrical capacitance between drain and source. With $V_{DS} = 0V$, V_{GS} allows or hinders the formation of the 2DEG. Near the pinch-off region and with more negative V_{GS} , the 2DEG formation is blocked, setting the maximum electrostatic separation between drain and source and therefore large values of C_{ds} . These values decrease as V_{GS} turns less negative and allows the 2DEG formation. The emergence of significant effects related to C_{ds} around $V_{DS} = 0V$ and $V_{GS} \geq 0V$ has been reported in works of GaN HEMT modeling like [67, 69]. All these bias-dependencies are accounted for by the extracted values of C_{ds} .

Large V_{DS} values produce high electric fields along the channel that diminish the geometrical capacitance between drain and source, especially with V_{GS} near the pinch-off region or at more negative values. Thus, C_{ds} is expected to show a decrease with respect to the drain voltage, particularly in the pinch-off region, as shown by the extracted values of this parameter.

G_m represents the rate of change of the drain current with respect to the gate voltage. Then, its bias dependency is deduced of the DC IV transfer characteristic. With $V_{DS} = 0V$ or with V_{GS} near pinch-off or more negative, the values of G_m are expected to be low. The transconductance increases rapidly in the low- V_{DS} range when V_{GS} moves away from pinch-off. For large V_{DS} values G_m is expected to show a saturated almost-constant behavior with a decrease due to thermal effects for V_{GS} values that allow high drain currents. With V_{DS} above 0V, it is a well-known characteristic of GaN HEMTs that the transconductance has a non-symmetrical bell-shape with respect to V_{GS} , with an accentuated increase from pinch-off than gradual decrease after the peak value. These properties of the transconductance are well represented by the extracted G_m .

The parameter τ represents the time delay due to the drift of electrons along the 2DEG, and thus, increases strongly as the gate voltage approaches the pinch-off region and as the drain voltage approaches 0V. This is correctly shown by the extracted values of this parameter.

R_{gd} and R_i represent spatial delays in the setup of the charge storage effects related to C_{gd} and C_{gs} . The resistive parts of these delays are expected to be similar in the high-current ohmic region, characterized by high- V_{GS} and low- V_{DS} values [74]. The extracted values of R_{gd} and R_i are similar and show a comparable bias dependency in that region.

According to several small-signal models for GaN HEMTs previously published [67, 69, 78], G_{ds} is expected to present its lowest values outside the ohmic region, there, it is often considered constant with respect to V_{DS} . In the ohmic region, G_{ds} is expected to increase fast in direct proportion with V_{GS} and indirect proportion V_{DS} . These bias dependencies are shown by the extracted G_{ds} values shown in Figure 5.9 and Figure 5.10.

The conductance parameters related to the gate G_{gdf} and G_{gsf} represent effects of forward bias of the gate diodes that mainly occur with increasing V_{GS} values above 0V. In particular, G_{gdf} is related to the gate-drain voltage, and thus, it has a more marked decrease with increasing V_{DS} . These bias dependencies are reflected by the extracted G_{gdf} and G_{gsf} values.

5.2.2 Verification Tests with S-Parameters on Active Bias Points

The small-signal model can be completely evaluated, and the related S-parameters calculated, on all the bias points where the intrinsic parameter values have been extracted. The model is usually verified testing the agreement of its calculated S-parameters with the actual measurements on any given bias point. In the present section, the following equation is used to evaluate the agreement of modeled and measured S-parameters.

$$E_{S,rel} = \frac{1}{N} \sum_{n=1}^N \frac{1}{4} \sum_{i,j=1}^2 \frac{|S_{ij,n}^{model} - S_{ij,n}^{meas}|}{|S_{ij,n}^{meas}|} \times 100\% \quad (5.1)$$

This expression is a simple relative-error metric applicable for all the bias points, in contrast with the S-parameters component (E_S) of the objective function E^P , which was previously employed in this thesis work, in the sweeps of values and the optimization process. The E_S error metric, as defined in equation (4.24) was not used to evaluate model accuracy on all bias points, because it contains weighting factors specifically oriented to the S-parameters of the *cold pinch-off* condition.

Modeled S-parameters were calculated for all the bias points on which S-parameters were measured, evaluating $E_{S,rel}$ with equation (5.1) for each point. The frequency ranges considered were 0.4 to 18 and 0.4 to 10 GHz, for the 2-mm and 3.2-mm devices, respectively.

In this way, the bias dependency of the accuracy to predict S-parameters was obtained, that is, $E_{S,rel}(V_{DS}, V_{GS})$, for the small-signal models of the studied large-size devices. These $E_{S,rel}(V_{DS}, V_{GS})$ are shown in Figure 5.9 and Figure 5.10, where the Z-axis is presented in logarithmic scale to get a better illustration on the whole percentage span.

The high- V_{GS} low- V_{DS} region markedly exhibits the lowest accuracy. This is likely due to a combination of the following three factors:

- The high channel conductivity in the high- V_{GS} low- V_{DS} region makes S-parameter measurements on such bias points especially sensitive to instantaneous variations of the bias voltages, which appear at the DC sources that set nominal bias point during S-parameter characterization.
- G_{gdf} and G_{gsf} show their major effect in the high- V_{GS} low- V_{DS} region and are typically calculated from S-parameters data around or below the 50-MHz range. However, I_{DS} at high V_{GS} values of the studied large-size devices exceeded the current rating of the bias tees integrated in the available VNAs, and thus, external biasing circuits were needed for S-parameters characterization on active bias points (as stated in subsection 3.2.2.2 related to S-parameters measurement techniques and setup). The commercial bias tees applied had minimum operation frequency of 400 MHz, so the lowest frequency points measured were not low enough for the optimal extraction of G_{gdf} and G_{gsf} , and their values are likely overestimated. Mengistu reported a similar situation in [65] and performed an iterative search to correct the G_{gdf} and G_{gsf} values. That search was not adopted in this thesis work, because it demands the intervention of an experienced modeler (is computationally heuristic), makes ambiguous the physical interpretation of the obtained G_{gdf} and G_{gsf} values and only improves partly the extracted intrinsic parameter values for the high- V_{GS} low- V_{DS} region, as was presented in [65].
- Different works suggest that the extrinsic resistance parameters are bias dependent in high power devices [77, 100, 101], specifically the access resistances R_d and R_s . Using constant values with respect to the bias could be causing a model mismatch in the high- V_{GS} low- V_{DS} region.

Nonetheless, the relative error values averaged on all bias points are 2.48% and 2.05% for the 2-mm and 3.2-mm device models, respectively.

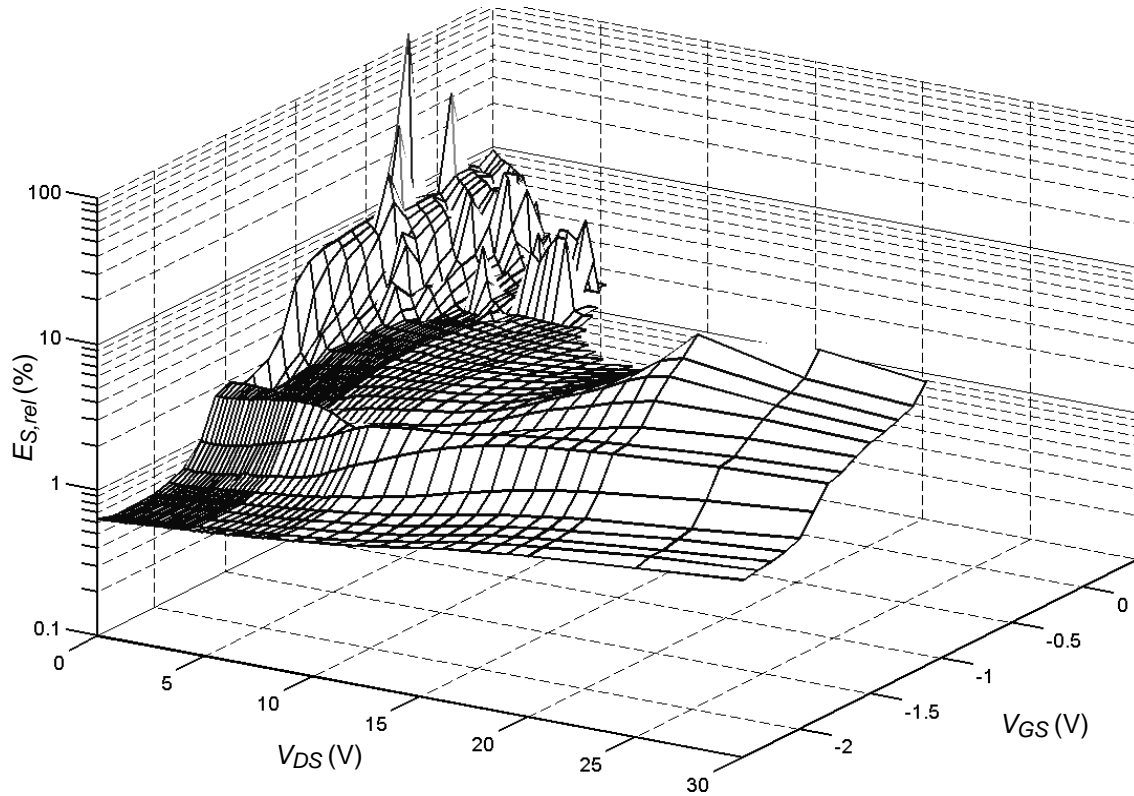


Figure 5.9 Bias dependency of the accuracy to predict S-parameters of the small-signal model developed for the 2-mm device.

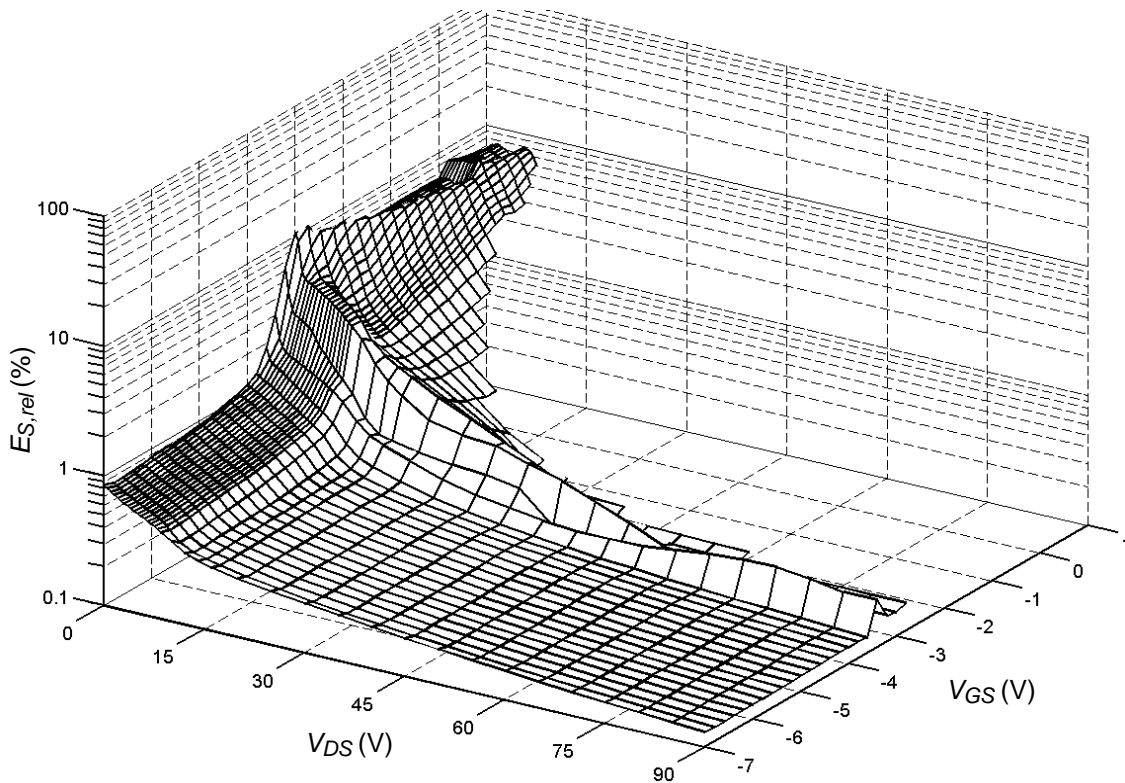


Figure 5.10 Bias dependency of the accuracy to predict S-parameters of the small-signal model developed for the 3.2-mm device.

Figure 5.11 and Figure 5.12 show agreements between modeled and measured S-parameters for bias points distributed in the IV regions, for the 2-mm and 3.2-mm devices, respectively. In such figures, S_{22} and S_{12} were multiplied by given factors to show all S-parameters together clearly in a single chart. Factor values are indicated besides the corresponding trace.

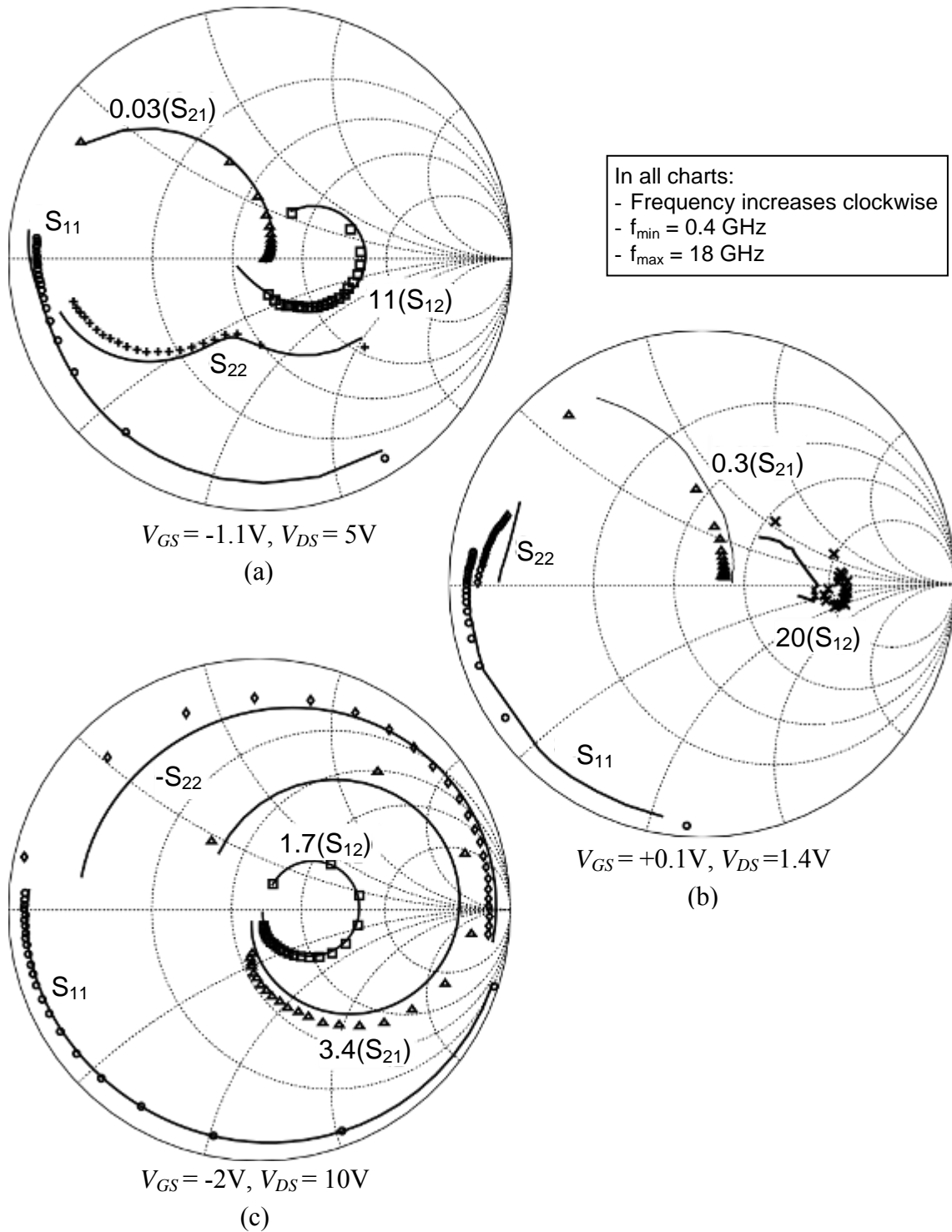


Figure 5.11 Comparison of measured S-parameters with predictions of the small-signal model developed for the 2-mm, on active bias points in the (a) saturation, (b) high- V_{GS} low- V_{DS} and (c) pinch-off regions.

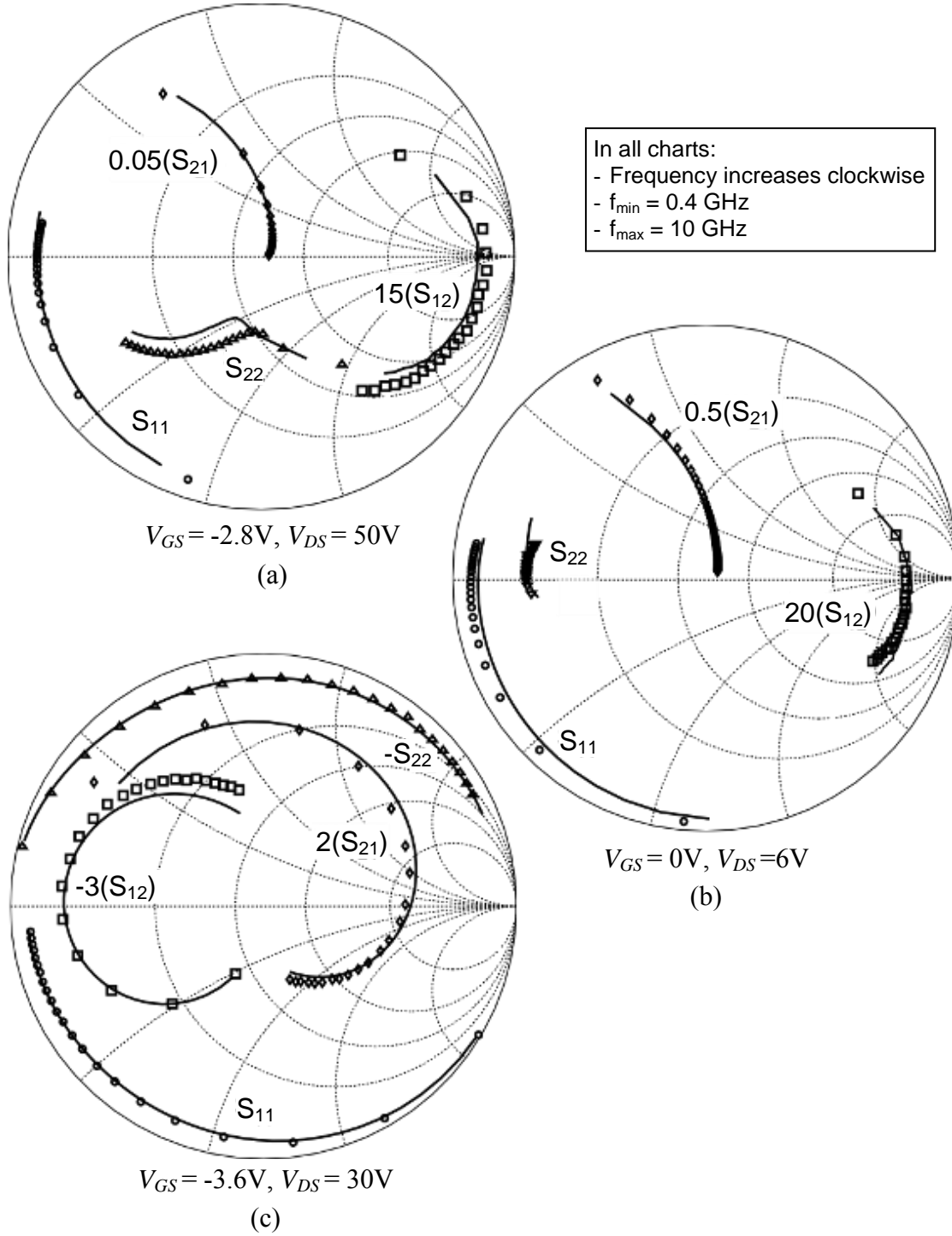


Figure 5.12 Comparison of measured S-parameters with predictions of the small-signal model developed for the 3.2-mm device, on active bias points in the (a) saturation, (b) high- V_{GS} low- V_{DS} and (c) pinch-off regions.

Figure 5.11 and Figure 5.12 show a better agreement for S_{11} than for the other S-parameters, although a general concordance between the model predictions and measurements is observable. The good agreement of S_{11} highlights the correctness of the modeling of the device input impedance, which is related to adequate representation and identification of parasitic and intrinsic effects related the gate-source branch for both studied devices.

The largest deviations of modeled and measured S_{11} appear in bias points located in the high- V_{GS} low- V_{DS} region, shown in (b) of Figure 5.11 and Figure 5.12. This occurs for the other S-parameters too. It is more marked for S_{22} and S_{21} and it is more evident for S-parameters of the 2-mm device than for those of the 3.2-mm device.

Moderate accuracy in the high- V_{GS} low- V_{DS} region, and the fact that the problem is more marked for the 2-mm device model than for the 3.2-mm device model are observations also traceable in the bias-dependency of the relative error of the model, $E_{S,rel}$, shown in Figure 5.9 and Figure 5.10.

A deviation between modeled and measured S_{22} of the 2-mm device is evident in the low-frequency range for the bias point in pinch-off, shown in Figure 5.11(c). It is supposed to be caused by a deficit of the small-signal model to represent parasitic current conduction in the buffer or substrate of GaN devices built on Si, according to [69]. Two extrinsic RC circuits in series with C_{pgs} and C_{pds} were used in [69] to solve that deficit, but the extra 4 elements were added to a circuit that only has 8 extrinsic elements, in contrast with the 12 extrinsic elements of the circuit used in the present work. The parameter extraction for 16 extrinsic elements is feasible with the use of optimization, but was discarded in the present work in pursuit of other modeling goals, such as maximizing generality of application and physical meaningfulness of the extracted parameter values. Taking into account the importance of these goals, the specific deviation of low-frequency S_{22} in pinch-off for GaN devices on Si is considered acceptable.

Decreased model accuracy in the high- V_{GS} low- V_{DS} region is attributed to the following factors: (i) Increased sensitivity to instantaneous bias voltage variations for bias points of that IV region, (ii) imperfect estimation of G_{gdf} and G_{gsf} at 400 MHz and (iii) bias-dependent extrinsic resistances.

5.3 Small-Signal Model Scalability

The present subchapter deals with the small-signal model scalability. As indicated at the beginning of Chapter 3, 0.5-, 0.8- and 2-mm IAF devices were studied with the purpose, besides the 3.2-mm (8x0.4-mm) device that has been on the main focus of this thesis until this point.

Top-view images of this family of devices were given already in Chapter 4 from Figure 4.17 to Figure 4.21 (except Figure 4.18). None of

these devices has source-connected field plates like the Nitronex[®] device, but the 2-mm device of this family has the same source air bridges in the gate side as the 3.2-mm device (shown in Figure 4.19). Taking those facts into account and following Table 4.2, the capacitance ratios that can be evaluated for this family of the devices are listed in Table 5.3. It contains the generated capacitance ratios values and the values of required ratios of physical features. Such ratios of physical features are estimated using the top-view images from Figure 4.17 to Figure 4.21 (except Figure 4.18).

Table 5.3 Capacitance ratio values generated for the studied family of devices.

Gate periphery	$\frac{C_{pds}}{C_{pgs}} \approx \frac{A_{p+bd}}{A_{p+bg}}$	$\frac{C_{pds}}{C_{dsi2}} \approx \frac{A_{p+bd}}{A_{fd}}$	$\frac{C_{dsi1}}{C_{pgd}} \approx$	$\frac{n_{fg}}{n_{fd}} \cdot \frac{d_{pgd}}{d_{dsi2}} \cdot \frac{w_{fg}}{l_{fd}} \cdot \frac{C_{gsi}}{C_{gdi}} \approx \frac{d_{gdi}}{d_{gsi}}$
0.5 mm	2.84	0.43	11.44	$\approx 2 \cdot 0.80 \cdot 7.14 \cdot 4.25$
0.8 mm	4.45	0.27	18.31	$\approx 2 \cdot 0.80 \cdot 11.43 \cdot 4.25$
2 mm	-	1.63	11.31	$\approx 2 \cdot 1.28 \cdot 4.42 \cdot 4.25$
3.2 mm	-	1.02	18.03	$\approx 2 \cdot 1.28 \cdot 7.04 \cdot 4.25$

For the extrinsic parameter extraction of the 2-mm device the same 4-parameter sweep of values was performed as exemplified in section 4.2.4 for the 3.2-mm device (sweeps on C_{gsi} , C_{dsi} , C_{ds} and C_{gs}/C_{gd}). For the 0.5-mm and 0.8-mm devices the extrinsic parameter extraction requires sweeps only on 3 parameters, because one extra capacitance ratio can be reliably evaluated from top-view images (C_{pds}/C_{pgs}). Similarly as demonstrated in section 4.2.4 for the large-size devices, the sweeps of values employed *cold pinch-off* S-parameter measurements to extract the values of the extrinsic capacitance and inductance parameters (obtained from the best solution candidates found by sweeps). Afterwards, values of the extrinsic resistance parameters were extracted from *cold reverse* S-parameter measurements.

As a result, high-quality measurement-correlated starting values of the model parameters in *cold pinch-off* conditions were obtained for the whole family of devices. Then, those starting values were subject of the same optimization process as performed previously for the large-size devices.

5.3.1 Extracted Parameter Values for Different Device Sizes

Results of the extrinsic parameter extraction after optimization are listed in Table 5.4 for the whole family of IAF devices. The large C_{gd} values are noteworthy, they are attributed to physical device properties and are supposed to be caused by strong V_{GS} -activated trapping effects or influence

of the passivation layers [52, 64, 85-87]. These parameter values produce the agreement shown in Figure 5.13 between S-parameters measurements and model predictions in *cold pinch-off* conditions.

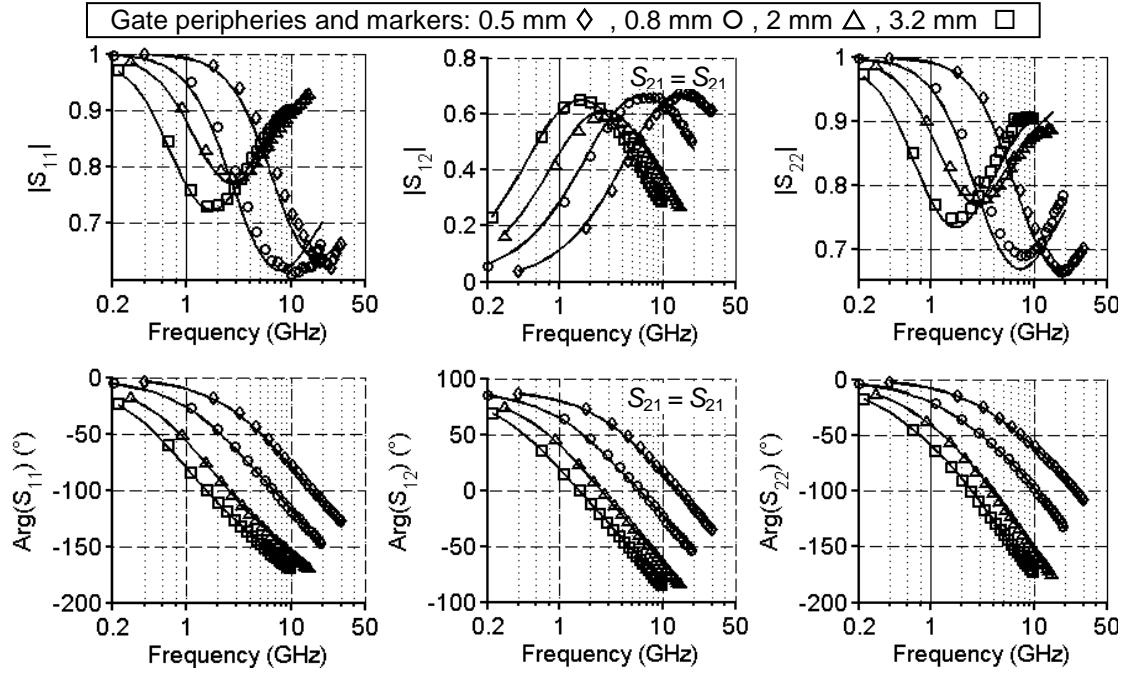


Figure 5.13 Comparison of measured *cold pinch-off* S-parameters (solid lines) with predictions of the small-signal models (markers) developed for the family of devices.

Table 5.4 Extracted values of the model parameters for the studied family of devices with different gate peripheries.

		Gate periphery			
Parameter		0.5 mm (2x250 μm)	0.8 mm (2x400 μm)	2 mm (8x250 μm)	3.2 mm (8x400 μm)
Extrinsic	C_{pgs} (fF)	19.10	20.87	215.00	203.87
	C_{pds} (fF)	11.30	10.50	141.96	115.48
	C_{pgd} (fF)	2.09	1.80	9.08	10.21
	C_{gsi} (fF)	85.85	129.14	365.45	567.27
	C_{dsi} (fF)	39.89	58.35	136.50	213.15
	C_{gdi} (fF)	19.96	31.09	76.07	130.87
	L_g (pH)	18.15	28.47	48.85	83.89
	L_d (pH)	23.84	40.15	98.57	168.8
	L_s (pH)	0.06	1.49	4.88	8.22
	R_g (Ω)	5.15	8.81	0.78	1.6
	R_d (Ω)	5.28	3.69	2.98	2.05
	R_s (Ω)	3.34	1.98	0.45	0.14
Intrinsic	C_{gs} (fF)	88.70	137.63	373.66	603.86
	C_{ds} (fF)	19.50	30.84	75.80	119.46
	C_{gd} (fF)	263.63	401.47	851.44	1581.37
	R_i (Ω)	0.00	0.00	1.34	1.63
	G_{ds} (mS)	4.43	0.52	14.06	50.08
	R_{gd} (Ω)	0.00	0.00	0.00	0.00

5.3.2 Scalability of Model Parameters in Terms of w_{fg}

This section presents the analysis of scalability in terms of the gate width for the extracted parameter values. For each parameter whose scalability is analyzed, the extracted value of a device with an initial w_{fg} is denoted by $f(\text{initial})$, and the extracted value of a device with scaled w_{fg} by $f(\text{scaled})$. The parameter values listed in Table 5.4 are used for the analysis.

For devices with equal number of fingers n_{fg} , extracted values of C_{pgs} and C_{pds} and C_{pgd} listed in Table 5.4 do not show a significant difference with the scaling of w_{fg} . That is so, because the related capacitive effects are due to contacting pads, bus-bars and air bridges, which are physical features of the finger layout that are not modified by the scaling of w_{fg} .

According to the scaling rules presented in section 4.4.1, the parameters C_{gsi} , C_{dsi} , C_{gdi} , C_{gs} , C_{ds} , C_{gd} , L_g , L_d , L_s , R_g , and the reciprocals $1/R_d$ and $1/R_s$, scale in direct proportion to w_{fg} .

Figure 5.14 shows the calculated ratios $f(\text{scaled})/f(\text{initial})$ for parameters of the 0.5-mm and 0.8-mm devices, which have equal n_{fg} of 2, but w_{fg} scaled from 250 to 400 μm , respectively. The figure also shows the ratios between parameter values of the 2-mm and 3.2-mm devices, which have equal n_{fg} of 8, but w_{fg} scaled, also from 250 to 400 μm .

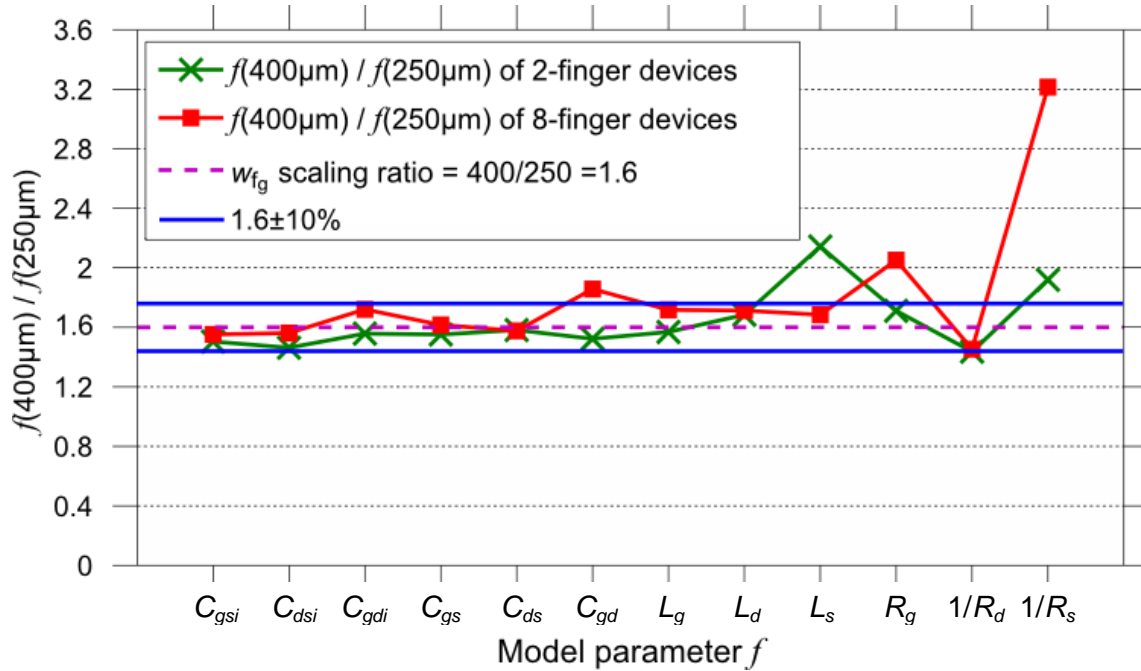


Figure 5.14 Calculated scaling ratios of extracted parameter values for devices with w_{fg} scaled but same number of fingers.

In Figure 5.14, a dashed line highlights the expected ratio value of 1.6 (400/250) and solid lines enclose the range where deviations from the expected value were considered minor. The range was defined in a conventional way as $\pm 10\%$ of the expected value.

The calculated scaling ratios for L_s of the 2-finger devices and R_s of the 8-finger devices show considerable deviations from 1.6. However, these element values appear to be rather low, e.g. L_s of the 0.5-mm device is 0.06 pH and R_s of the 3.2-mm device is 0.14Ω , so that small uncertainties of the related parameter extraction cause large ratio spreading.

The scaling ratio for R_g of the 2-finger devices also exhibits a significant deviation from 1.6. R_g is known to be a parameter difficult to scale in terms of w_{fg} , for example, reference [8] proposed a composite scaling rule given by $R_g(w_{fg}) = R_{g0} + R_{g1}(w_{fg})$, where R_{g1} is the component that scales in direct proportion to the scaling of w_{fg} , and R_{g0} a component constant with respect to w_{fg} .

Such composite scaling rules were not employed in this thesis work, because only two devices with different values of w_{fg} were available (of the same manufacturer and with the same number of gate fingers) and a meaningful evaluation of such expressions requires more w_{fg} values.

Also $C_{gd}(\text{scaled})/C_{gd}(\text{initial})$ of the 8-finger devices shows considerable deviation from 1.6. This is attributed to variations of capacitive effects related to C_{gd} of the 3.2-mm device that are unrelated to the scaling of w_{fg} , but that are due to the device localization on the wafer. Such variations of C_{gd} values are caused by charge-trapping effects in the active-layer gate-drain region that are not uniform along the wafer, as explained in [102]. Besides, according to [85], fluctuations of the passivation layers along the wafer due to imperfections of the layer growth process also lead to fluctuations of the C_{gd} values at different wafer regions.

Figure 5.15 locates the family of analyzed devices on the studied wafer fragment. On one hand, Figure 5.15 shows that the 3.2-mm and 2-mm HEMTs, used to calculate $C_{gd}(\text{scaled})/C_{gd}(\text{initial})$ of the 8-finger devices, are found more apart on the wafer than any other pair of analyzed devices. Furthermore, the analyzed 3.2-mm device is found on a different wafer cell than the other devices, because the corresponding device in the original cell was broken. Thus, the above mentioned fluctuations of layer properties on

the wafer fragment are thought to produce C_{gd} variations on the 3.2-mm device that are unrelated to the w_{fg} scaling, and that leads to the observed deviation from 1.6 of $C_{gd}(\text{scaled})/C_{gd}(\text{initial})$ of the 8-finger devices.

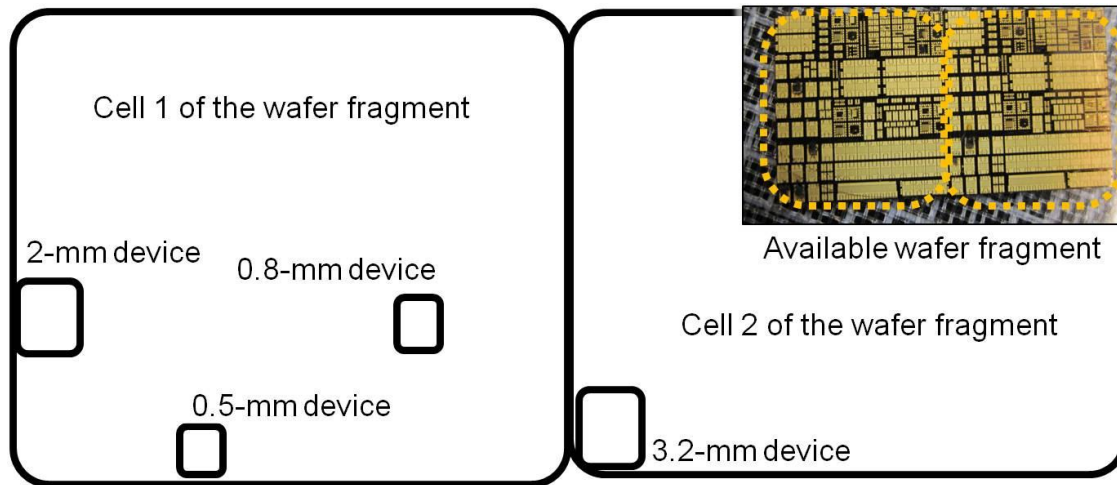
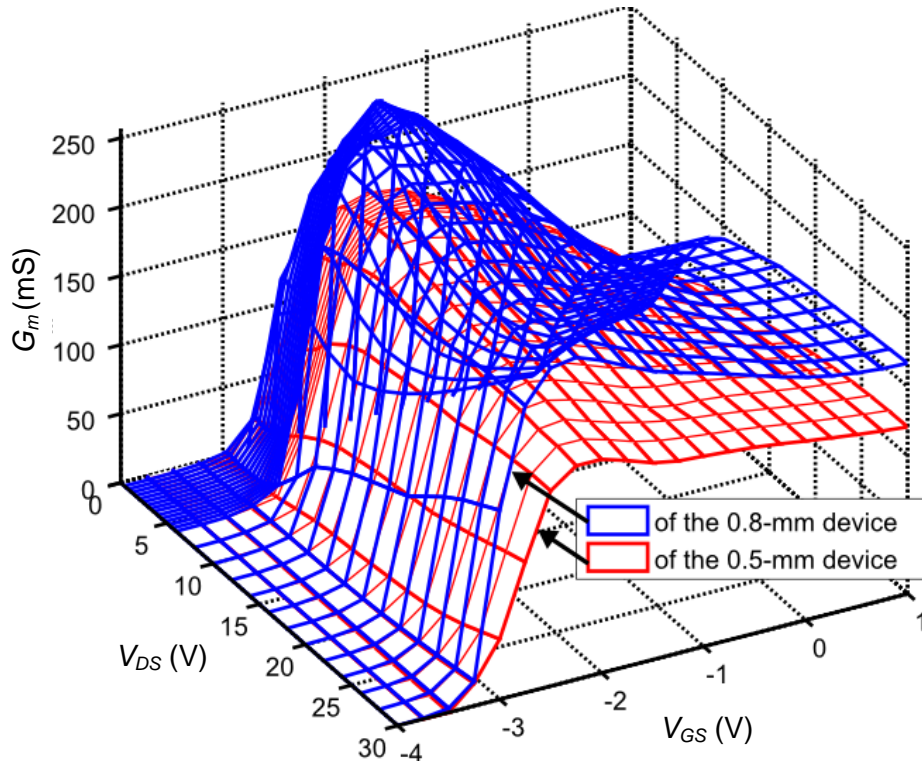


Figure 5.15 Location of the devices, whose model parameter scalability was analyzed, on the available wafer fragment.

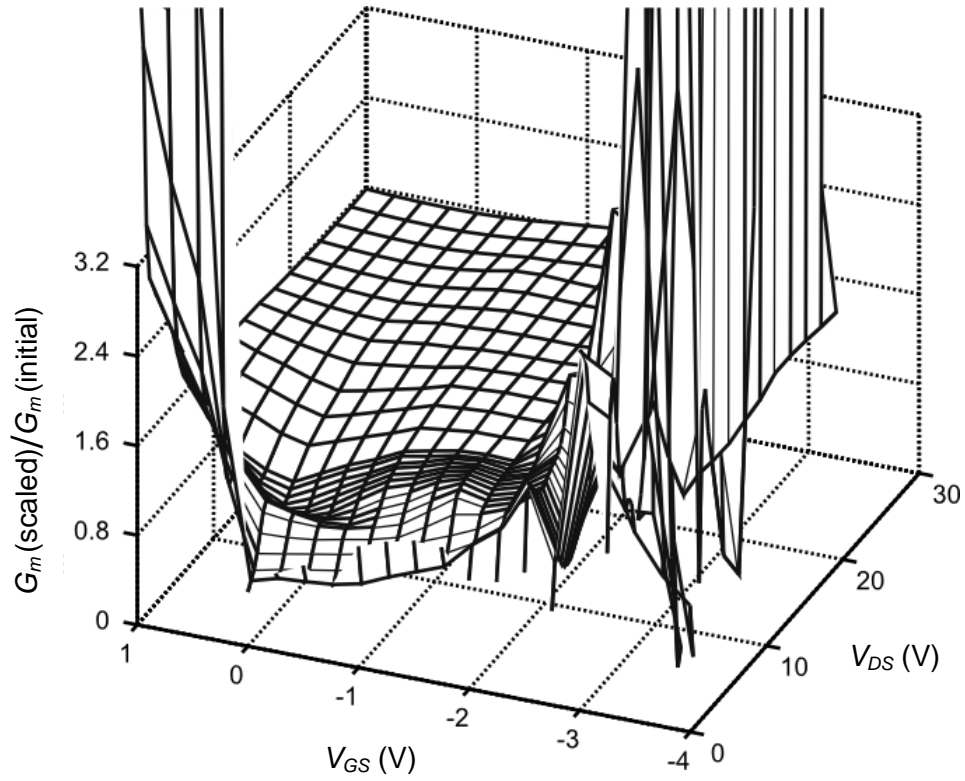
Figure 5.16 to Figure 5.18 exemplify scaling behaviors of small-signal bias-dependent intrinsic parameters with respect to the scaling of w_{fg} . On their parts (a), the figures show bias-dependent extracted values of C_{gs} , G_m and C_{gd} for two devices that have the same n_{fg} but different w_{fg} , using lines with circle markers for device case with scaled w_{fg} . On their parts (b), the figures present the bias-dependent scaling ratios $f(\text{scaled})/f(\text{initial})$ that are received. The intrinsic parameter values were extracted using extrinsic parameter values listed in Table 5.3 and S-parameters measured on active bias points, as explained in section 5.2.1 for the studied large-size devices.

Calculated $f(\text{scaled})/f(\text{initial})$ ratios of the intrinsic parameters agree reasonably with the expected value of 1.6, for bias points outside the high- V_{GS} and low- V_{DS} region. Deviations inside that region are probably originated by decreased model accuracy related to such region (whose causes were discussed in section 5.2.12), and are least likely originated by flaws of model scalability.

The largest deviations of $G_m(\text{scaled})/G_m(\text{initial})$ from 1.6 that appear in Figure 5.16(b) on bias points of the pinch-off region, are due to the related small parameter values. In the pinch-off region, G_m values are negligible, and thus, deviations of $G_m(\text{scaled})/G_m(\text{initial})$ from 1.6 are not meaningful.

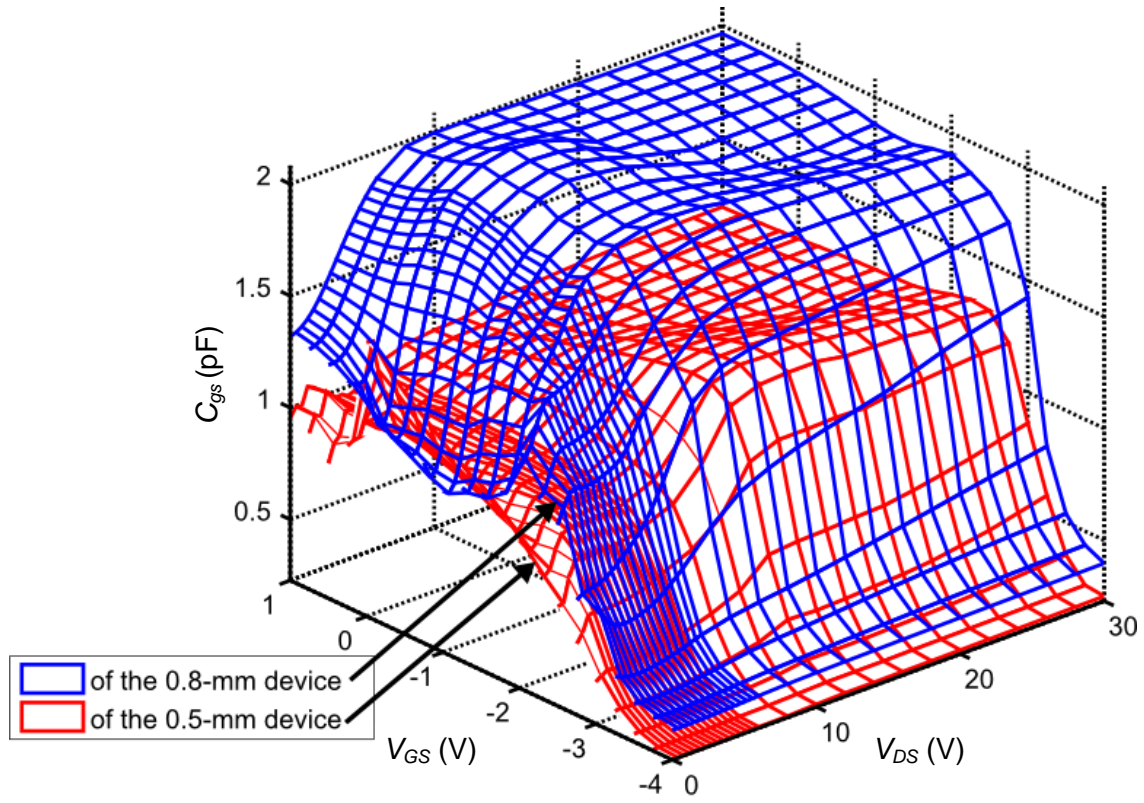


(a)

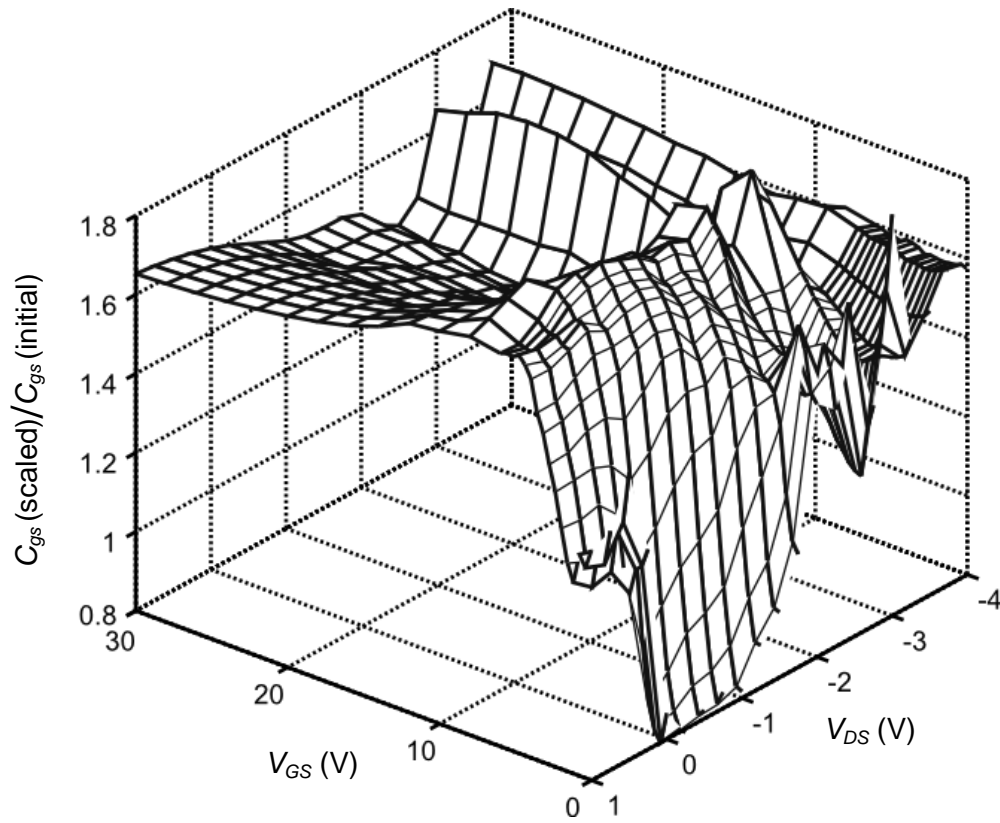


(b)

Figure 5.16 (a) Bias-dependent extracted values of G_m of 2-finger devices with scaling gate width from 250 μm (red line) to 400 μm (blue line), and (b) bias-dependent values calculated for $f(\text{scaled})/f(\text{initial})$.

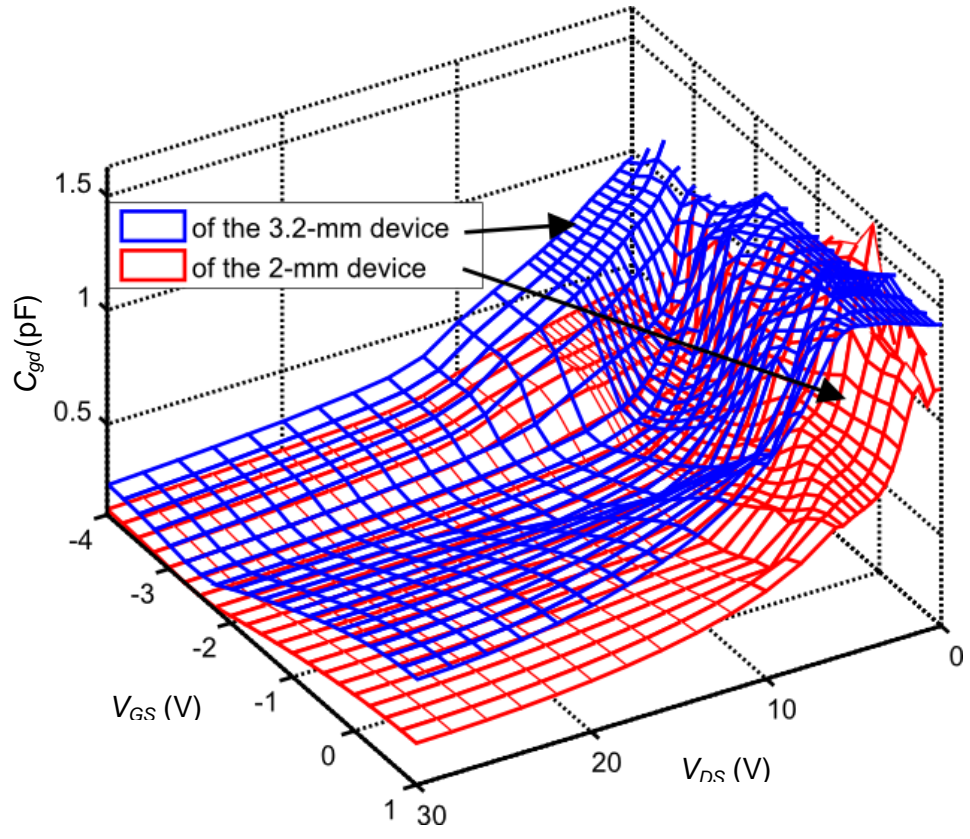


(a)

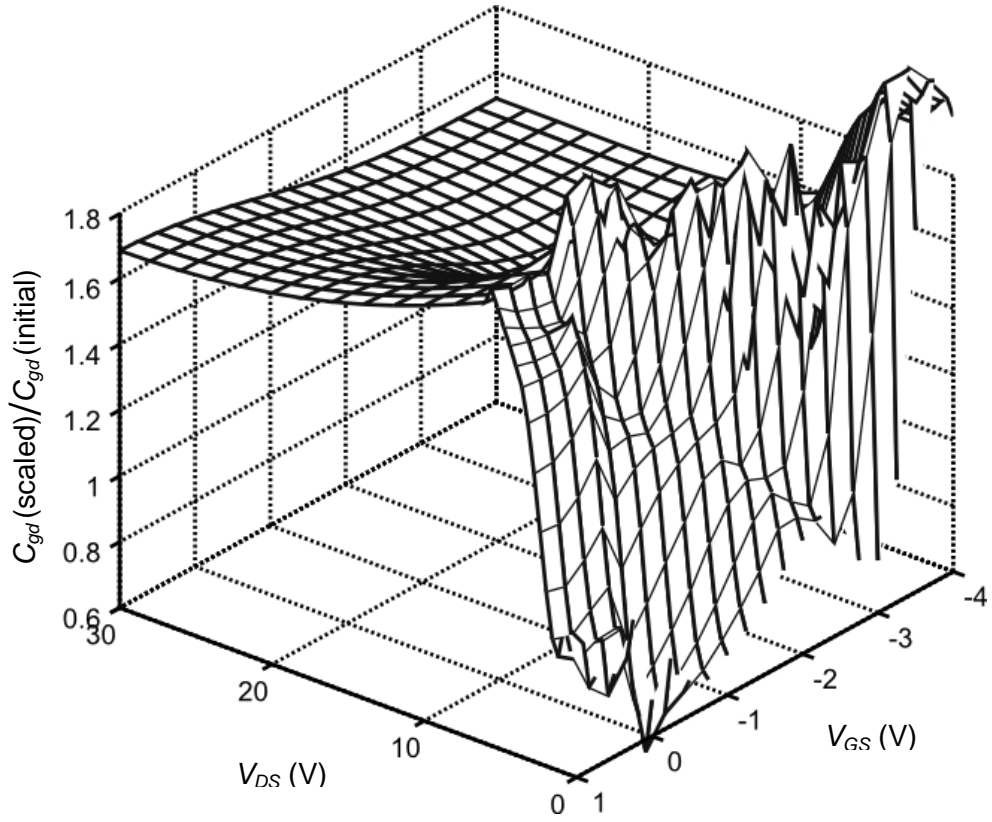


(b)

Figure 5.17 (a) Bias-dependent extracted values of C_{gs} of 2-finger devices with scaling gate width from 250 μm (red line) to 400 μm (blue line), and (b) bias-dependent values calculated for $f(\text{scaled})/f(\text{initial})$.



(a)



(b)

Figure 5.18 (a) Bias-dependent extracted values of C_{gd} of 8-finger devices with scaling gate width from 250 μm (red line) to 400 μm (blue line), and (b) bias-dependent values calculated for $f(\text{scaled})/f(\text{initial})$.

5.3.3 Scalability of Model Parameters in Terms of n_{fg}

This section presents analysis of scalability in terms of the number of gate fingers for the extracted parameter values. For each parameter whose scalability is analyzed, the extracted value of a device with an initial n_{fg} is denoted by $f(\text{initial})$, and the extracted value of a device with scaled n_{fg} by $f(\text{scaled})$. The parameter values listed in Table 5.4 are used for the analysis.

As stated in section 4.4.2, for the parasitic effects denoted by C_{pgs} and C_{pds} no specific scaling rule could be setup, in a general and reliable way, in terms of the scaling of n_{fg} .

On another hand, as was also discussed in section 4.4.2, the parameters C_{gsi} , C_{dsi} , C_{gdi} , C_{gs} , C_{ds} , C_{gd} , L_g , L_d , L_s , and the reciprocals $1/R_g$, $1/R_d$ and $1/R_s$, scale in direct proportion to n_{fg} .

Figure 5.19 shows the calculated ratios $f(\text{scaled})/f(\text{initial})$ for parameters of the 0.5-mm and 2-mm devices, which have equal w_{fg} of 250 μm , but n_{fg} scaled from 2 to 8, respectively. The figure also shows the ratios between parameter values of the 0.8-mm and 3.2-mm devices, which have equal w_{fg} of 400 μm , but n_{fg} scaled, also from 2 to 8 fingers. In Figure 5.19, a dashed line indicates the expected ratio value of 4 (8/2) and solid lines enclose the range where deviations from expected value were considered minor. The range was defined in a conventional way as $\pm 10\%$ of the expected value.

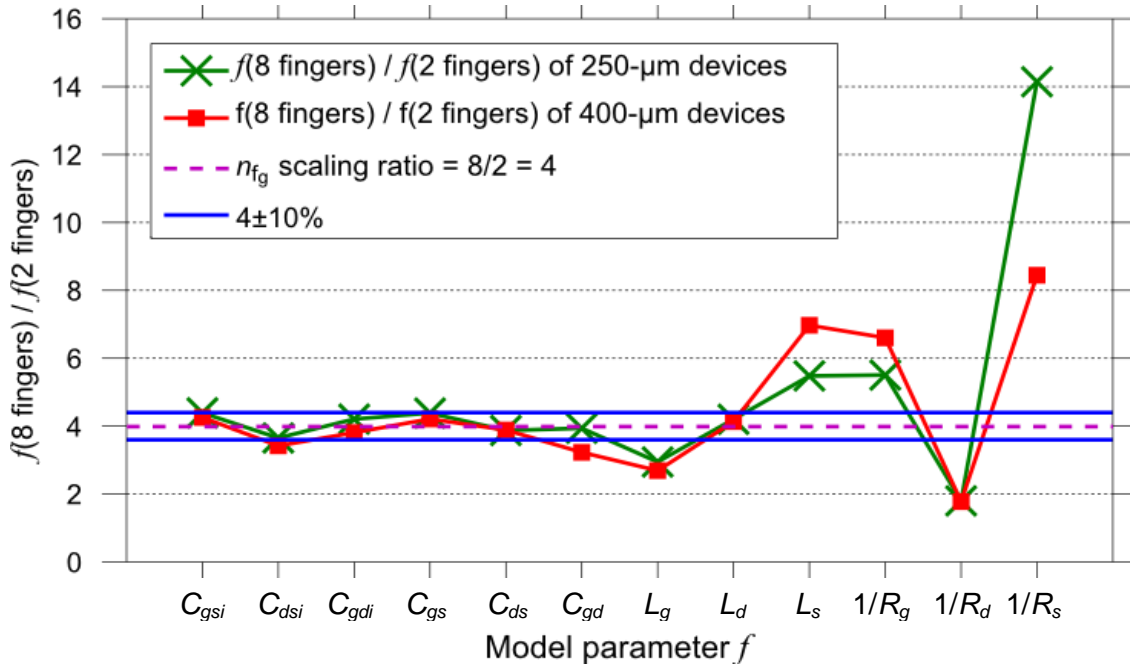


Figure 5.19 Calculated scaling ratios of extracted parameter values for devices with n_{fg} scaled but same unit gate electrode width.

The calculated scaling ratios of L_s and of R_s show considerable deviations from 4. Similarly as explained in the previous section 5.3.2, the extracted values of L_s for the 2-finger devices and of R_s for the 8-finger devices are rather low, e.g. L_s of the 0.5-mm device is 0.06 p Ω and R_s of the 3.2-mm device is 0.14 Ω , so that small uncertainties of the related parameter extraction cause large ratio spreading from the expected value.

Significant deviations from 4 also displayed for $f(\text{scaled})/f(\text{initial})$ of the extrinsic resistance parameters R_g and R_d . The scaling of n_{f_g} from 2 to 8 requires the use of bus bars and larger contacting pads for the drain and the gate. These modifications create additional resistance effects that do not have a precedent in the 2-finger devices, thus, the changes in R_g and R_d are not only due to the scaling of n_{f_g} and the calculated scaling ratios are likely to deviate from the expected value.

The considerable deviation of $L_g(\text{scaled})/L_g(\text{initial})$ from 4 is caused by the gate bus bars used on the 8-finger devices, which do not have a equivalent or precedent on the 2-finger devices. Conversely, the deviation of $L_s(\text{scaled})/L_s(\text{initial})$ from 4 is due to the source air bridges that are used on the 8-finger devices and that do not appear on the 2-finger devices.

Moreover, increasing finger number increases the device output power level and current, and its operation temperature. Uneven heat distribution between fingers of large-size devices has been documented, for example for the 3.2-mm device by Dahmani *et al.* in [103]. Conductivity is known to be linked to temperature and different heat distribution between fingers modifies the scaling behavior of resistance effects in terms of n_{f_g} .

For instance, consider an initial n_{f_g} equal to 2 fingers, then dissipated heat is evenly distributed between fingers. Temperature-related changes of the conductivity affect both fingers equally, and resistance effects are equally divided between the fingers, i.e. they are simply averaged over n_{f_g} .

Now consider a scaled n_{f_g} equal to 8 fingers. For such large-size devices heat is unevenly distributed between fingers, as demonstrated by Dahmani *et al.* in [103, 104], and thus, the fingers exhibit different temperatures. Temperature-related changes of the conductivity affect each finger differently, and resistance effects are not equally divided among the fingers, i.e. they are not simply averaged over n_{f_g} .

In this thesis work, the model parameter scalability in terms of n_{f_g} faces at least the next three obstacles: (i) the leap from even (2-finger devices) to uneven (8-finger devices) heat distribution between fingers, leading to temperature-related effects on the conductivity for the largest devices, and (ii) the difficulty to find a general and straightforward scaling rule for C_{pgs} and C_{pds} for the scaling of n_{f_g} from 2 to 8 fingers.

In consequence, it is concluded that model parameter scaling from 2-finger to 8-finger devices must be discussed only for the 2-mm device (from the 0.5-mm device), to avoid problems of inexact model scalability due to temperature-related effects of the conductivity that are expected for the largest 3.2-mm device.

Thus, scaled models for the 3.2-mm device must use scaling rules only in terms of w_{f_g} based on models for the 2-mm device and on C_{pgs} and C_{pds} values directly extracted from measurements (not scaled).

5.3.4 Tests of the Scaling Rules

Model scalability was tested comparing measurements with S-parameters of scaled models created by three different approaches (already foreseen in subchapter 4.4): (i) using only scaling rules in terms of w_{f_g} , (ii) using only scaling rules in terms of n_{f_g} and (iii) using both types of scaling rules. In the present section, the resulting scaled models are termed in a specific way, to ease the presentation of the scalability analysis, as follows:

- *Initial model*: Model developed initially for each device based on S-parameter measurements, top-view images and the parameter extraction proposed in sections 4.2 and 4.3, without using any scaling rules.
- *w_f -scaled model*: Model developed only with scaling rules in terms of w_{f_g} , based on an *initial model* of smaller device.
- *Quasi-scaled model*: Model of the 2-mm device developed with scaling rules in terms of n_{f_g} , based on the *initial model* of the 0.5-mm device, but also including non-scaled C_{pgs} and C_{pds} values from the *initial model* of the 2-mm device. The lack of proper scaling rules for C_{pgs} and C_{pds} in terms of n_{f_g} was discussed in section 4.4.2 and restated in 5.3.3. Reasons to omit a *quasi-scaled model* of the 3.2-mm device were also discussed in section 5.3.3 and will be restated later in the present section.

- *Two-step scaled model*: Model of the 3.2-mm device developed with the two types of scaling rules, based on the *initial model* of the 0.5-mm device, but also including non-scaled C_{pgs} and C_{pds} values from the *initial model* of the 2-mm device.

Thus, tests of model scalability were started with w_f -scaled models.

5.3.4.1 Tests of Scalability for w_f -Scaled Models

The *initial models* of the 0.5-mm and 2-mm devices served as basis to generate w_f -scaled models of the 0.8-mm and 3.2-mm devices, respectively. Then, S-parameters of the resulting w_f -scaled models were calculated and compared with measurements, as portrayed in Figure 5.20 and Figure 5.21. As reference, the figures also show with red dashed lines S-parameters of the *initial models* of the 0.8-mm and 3.2-mm devices.

Agreements of red dashed and solid lines on (a) and (c) of Figure 5.20 and Figure 5.21 indicate that w_f -scaled and *initial models* are similar, for bias points outside the high- V_{GS} low- V_{DS} region. This implies that outside that region, calculated scaling ratios of parameter values must agree with the scaling of w_{fg} , which actually confirms the findings of section 5.3.2. Moreover, agreements of the marker traces of the measurements with the solid lines of modeled S-parameters, shown on (a) and (c) of Figure 5.20 and Figure 5.21, validate the w_f -scaled models.

The largest discrepancies between measured and modeled S-parameters appear on (b) of Figure 5.20 and Figure 5.21, for bias points in the high- V_{GS} low- V_{DS} region. These specific discrepancies are partly attributed to decreased accuracy of *initial models*, but also partly attributed to flaws of the formulated scaling rules in terms of w_{fg} .

On one hand, decreased agreement of measurements with S-parameters of *initial models* for bias points in the high- V_{GS} low- V_{DS} region was already observed and discussed on the model verification tests of section 5.2.2. But on Figure 5.20(b) and Figure 5.21(b), S-parameters of *initial models* and measurements differ mainly for the high-frequency S_{22} and S_{21} , and the disagreements appear augmented for S-parameters of the w_f -scaled models.

Thus, the discussed discrepancies are not only originated by decreased accuracy of the *initial models*, but also by flaws of scaling rules in terms of w_{fg} to represent real parameter scaling at the high- V_{GS} low- V_{DS} region.

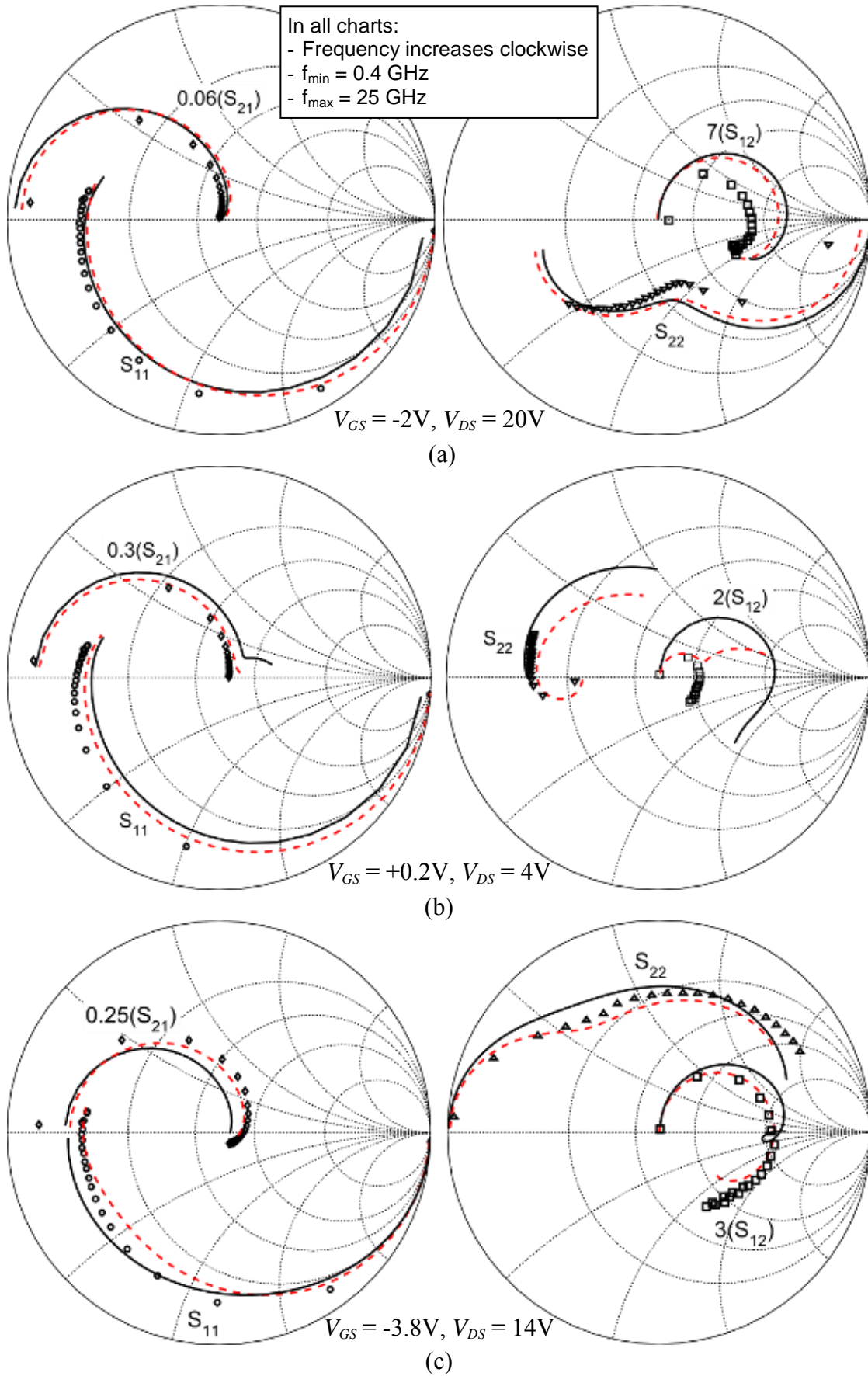


Figure 5.20 Measurements of the 0.8-mm device (markers) compared to S-parameters of the corresponding w_f -scaled (solid lines) and *initial models* (red dashed lines), on bias points in the (a) saturation, (b) high- V_{GS} low- V_{DS} and (c) pinch-off regions.

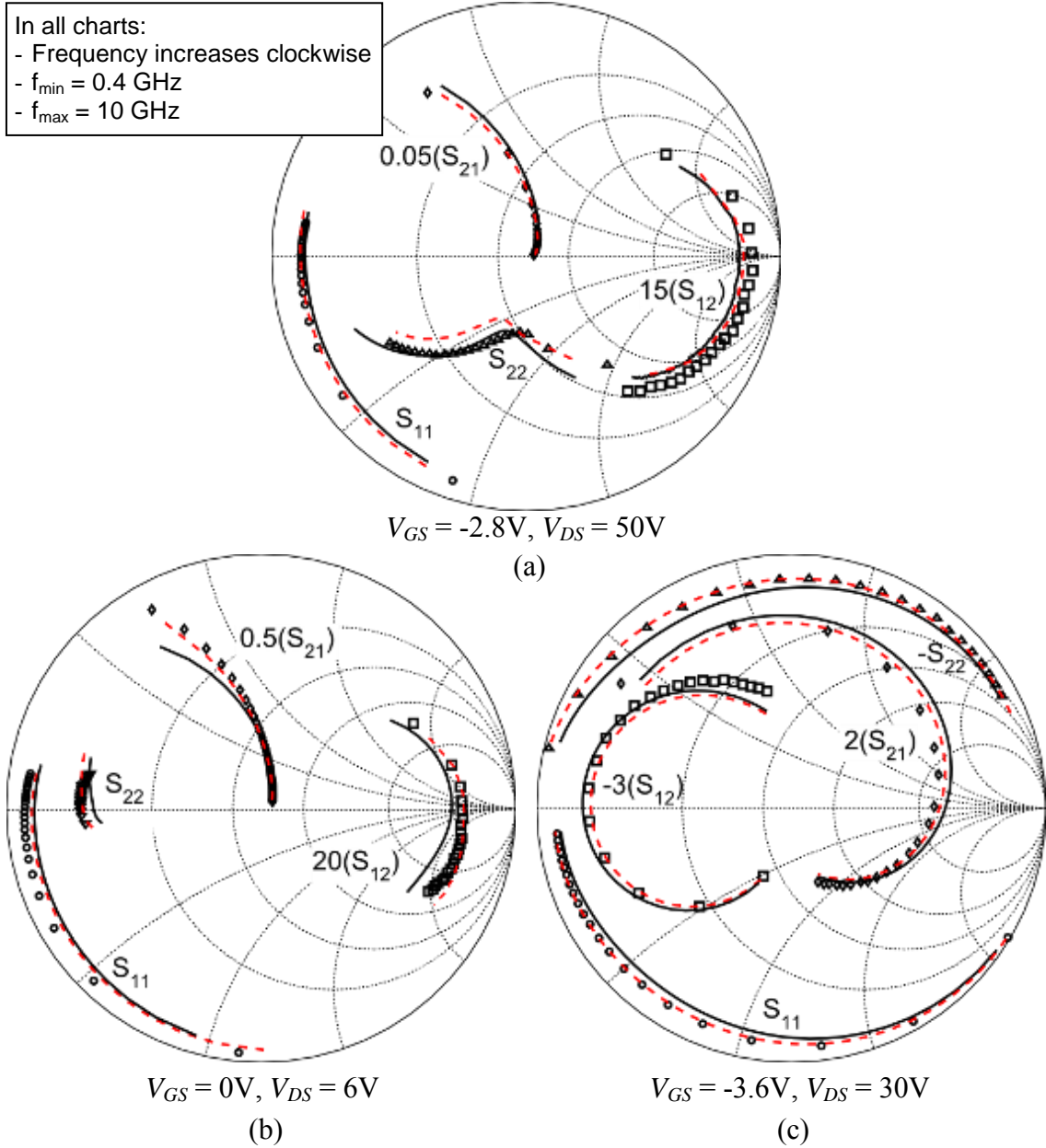


Figure 5.21 Measurements of the 3.2-mm device (markers) compared to S-parameters of the corresponding w_f -scaled (solid lines) and *initial models* (red dashed lines), on bias points in the (a) saturation, (b) high- V_{GS} low- V_{DS} and (c) pinch-off regions.

5.3.4.2 Tests of Scalability for *Quasi-Scaled Models*

Regarding model scalability tests in terms of n_{fg} , the *initial model* of the 0.5-mm device served as basis to generate a *quasi-scaled model* of the 2-mm device.

Following the conclusions of section 5.3.1, the C_{pgs} and C_{pds} values were not result of scaling, but were those of the *initial model* of the 2-mm device (listed in Table 5.4).

S-parameters of the *quasi-scaled model* were calculated and compared with measurements as shown in Figure 5.22, where red dashed lines indicate S-parameters of the *initial model* of the 2-mm device, as reference.

The largest disagreements of measurements with S-parameters of the *quasi-scaled model* appear at bias points in the high- V_{GS} low- V_{DS} region, shown in Figure 5.22(b), similarly as for w_f -scaled models. For other bias points, as those shown in (a) and (c) of Figure 5.22, the good agreements are also comparable with results of testing w_f -scaled models, which validates the *quasi-scaled model*.

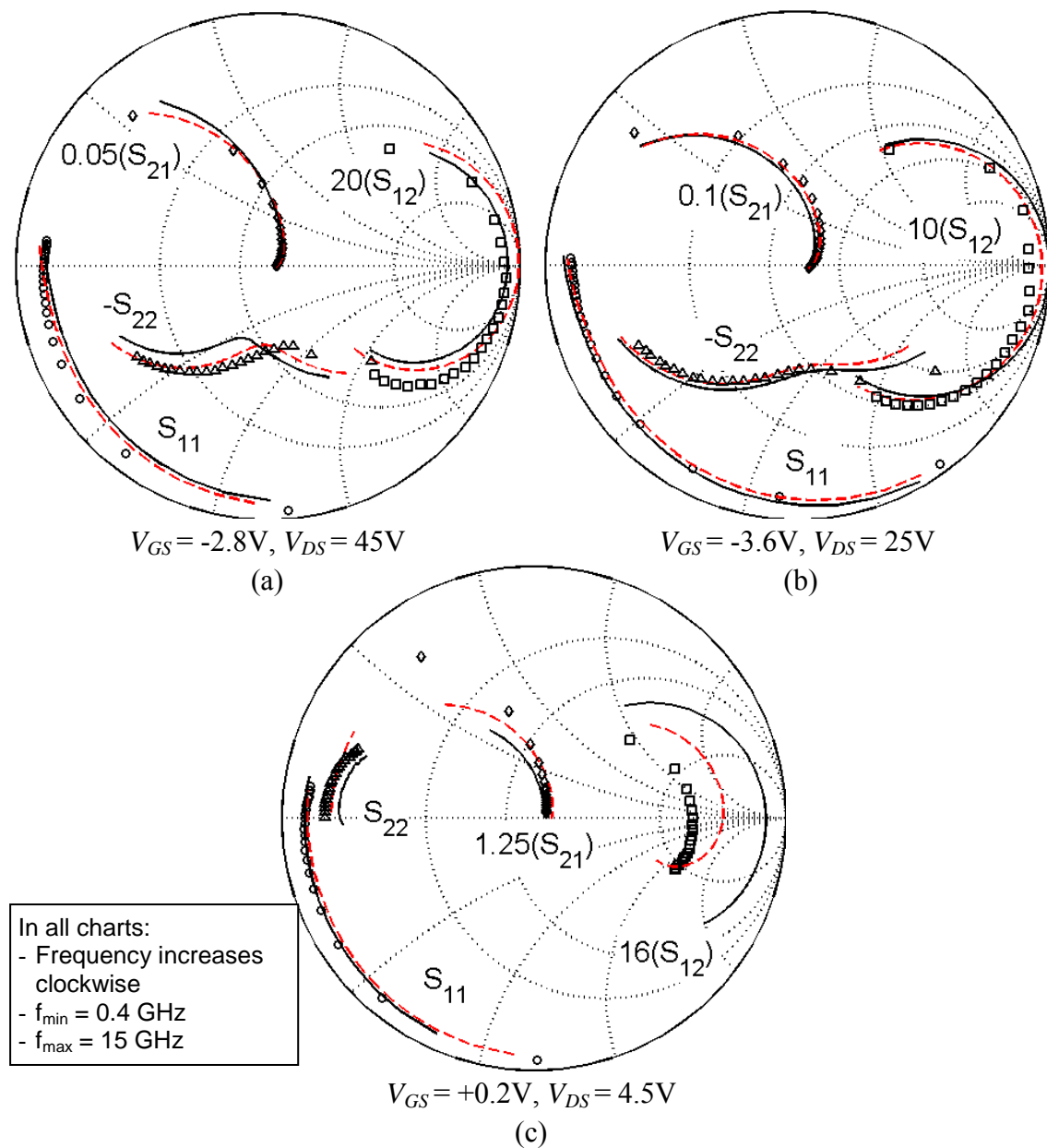


Figure 5.22 Measured S-parameters of the 2-mm device (markers) compared with predictions of the quasi-scaled model from the 0.5-mm device model (solid lines) and with predictions of the *initial* model (red dashed lines), on bias points in the (a) saturation, (b) pinch-off and (c) high- V_{GS} low- V_{DS} regions.

Following conclusions of section 5.3.1, generation of a scaled model of the 3.2-mm device from a model of the 0.8-mm device, was disregarded, to avoid the parameter scaling from 2-finger to 8-finger devices with rules in terms of n_{fg} . The reason to avoid this type of scaling for the largest device studied was that rules in terms of n_{fg} were considered imperfect, due to uneven heat-distribution and conductivity fluctuations between fingers at high operation temperatures. These phenomena were expected to occur for the 3.2-mm device, as documented in [103, 104].

5.3.4.3 Tests of Scalability for *Two-Step Scaled Models*

The *quasi-scaled* model of the 2-mm device obtained before was scaled using rules in terms of w_{fg} to generate a *two-step scaled model* of the 3.2-mm device. S-parameters of the *two-step scaled model* were calculated and compared with measurements as depicted in Figure 5.23 and Figure 5.24. S-parameters of w_f -scaled and *initial models* of that device are also depicted as reference, with thick solid and red dashed lines, respectively.

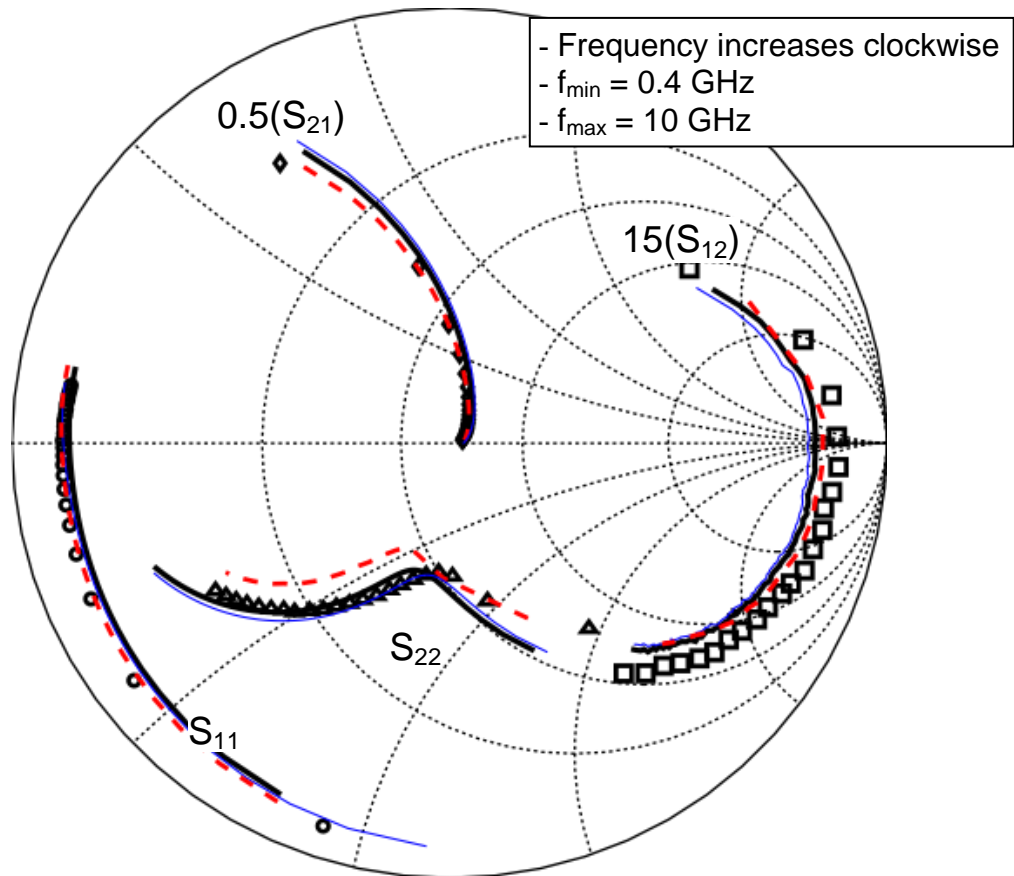


Figure 5.23 Measurements of the 3.2-mm device biased on $V_{GS} = -2.8V$ and $V_{DS} = 50V$ (circles) compared with S-parameters of the *two-step scaled model* (blue thin lines), of the w_f -scaled model (black thick lines) and of the *initial model* (red dashed lines).

The good agreement of modeled S-parameters with measurements shown in Figure 5.23, on a bias point in the saturation region, serves to validate the *two-step scaled model*. In general, for bias points outside the high- V_{GS} low- V_{DS} region, the w_f -scaled and *two-step scaled models* of the 3.2-mm device are considered equivalent, from the point of view of S-parameter prediction accuracy.

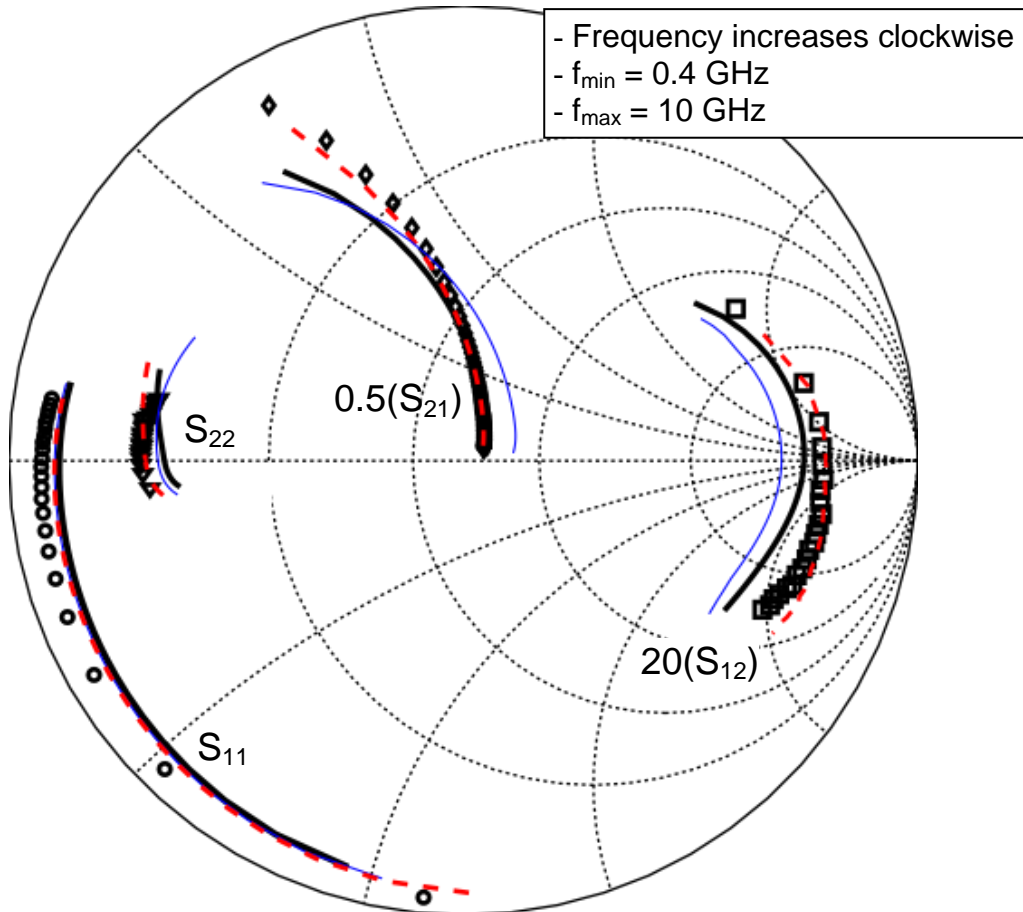


Figure 5.24 Measurements of the 3.2-mm device biased on $V_{GS} = 0V$ and $V_{DS} = 6V$ (markers) compared with S-parameters of the *two-step scaled model* (blue thin lines), of the w_f -scaled model (black thick lines) and of the *initial model* (red dashed lines)

Now let us analyze the agreement of measurements with S-parameters of the *two-step scaled model* for the 3.2-mm device exclusively for bias points in the high- V_{GS} low- V_{DS} region, as illustrated with Figure 5.24.

On such bias points, the largest discrepancies between measurements and S-parameters of scaled models occur for S_{21} and S_{22} . This remark is true when the measurements indicated by markers in Figure 5.24 are compared with the S-parameters of the *two-step scaled model* indicated by black thick lines. Besides, the remark is also true, when the comparison is made with the S-parameters of the w_f -scaled model indicated by thin blue lines.

This indicates that on bias points in the high- V_{GS} low- V_{DS} region, the reasons behind model-to-measurements discrepancies of the *two-step scaled model* are partly traceable in flaws of scaling rules in terms of w_{fg} (2nd scaling step of the *two-step scaled model*), which were already discussed in section 5.3.4.1.

There are differences between blue thin and black thick lines in Figure 5.24, e.g. compare S_{12} and S_{21} , indicating that model-to-measurements discrepancies augment for the *two-step scaled model* with respect to those for the *w_f-scaled model*. Then, flaws of the scaling rules in terms of n_{fg} possibly also contribute to the model-to-measurements discrepancies of the *two-step scaled model* for bias points located in the high- V_{GS} low- V_{DS} region.

In any way, this contribution is considered small, taking into account that differences between blue thin and black thick lines is not dramatic and that the magnitudes of S_{12} and S_{21} in Figure 5.24 are small (observe the magnification factor of 20).

As a result of tests of small-signal model scalability, the scaling rules in terms of w_{fg} proved to be more precise than those in terms of n_{fg} .

The rules in terms of n_{fg} were not as precise as expected, so their usage to generate models for circuit design of final prototypes would probably produce suboptimal results. However, it is certainly useful for device performance prognosis.

Besides, the requirements of nonlinear model accuracy for the circuit design must be distinguished from the requirements for the device optimization, regarding fabrication of larger-size and higher-power transistors. The latter application is more appropriate for the presented small-signal model scalability.

Chapter 6

Proposed Strategy for Large-Signal Modeling

An accurate description of the nonlinear effects in the transistor is essential for the optimal design of power amplifiers of modern technologies. For this purpose, the small-signal model must progress into a large-signal model.

The large-signal model developed in this thesis work was empirical, which means that the parameter extraction is based on measurements. Besides, the model was formulated using an electrical equivalent circuit.

6.1 Large-Signal Modeling with Electrical Equivalent Circuits

Empirical large-signal models with equivalent circuits use nonlinear sources of current and charge to represent the current flow in the transistor. Typically, these nonlinear sources are voltage-controlled and surrounded by a linear circuit, the extrinsic elements. The current sources stand for *conduction* currents [105], which can be understood as current components directly related to the motion of charge carriers [106]. The charge sources characterize *displacement* currents [105], which are considered to represent current components related to time-varying accumulation of charge [106].

The first large-signal models with equivalent circuits were developed for silicon MOS FETs employing a basic formulation, known as the quasi-static charge model, where charge in the device only depends on present values of the instantaneous voltages at its terminals, v_{GS} , v_{GD} and v_{DS} [105]. Figure 6.1(a) illustrates the physical origin of the quasi-static charge model. Parts (b) and (c) of Figure 6.1 depict the corresponding small-signal and large-signal equivalent circuits, respectively. The mathematical expressions relating the elements of the small- and large-signal circuits are shown in Figure 6.1(d). As indicated by those expressions, capacitance parameters of the small-signal circuit represent rates of change of large-signal charge sources with respect to the instantaneous voltages v_{GS} , v_{GD}

and v_{DS} . Similarly, conductance parameters of the small-signal circuit denote rates of change of the large-signal current source with respect to the instantaneous voltages v_{GS} and v_{DS} .

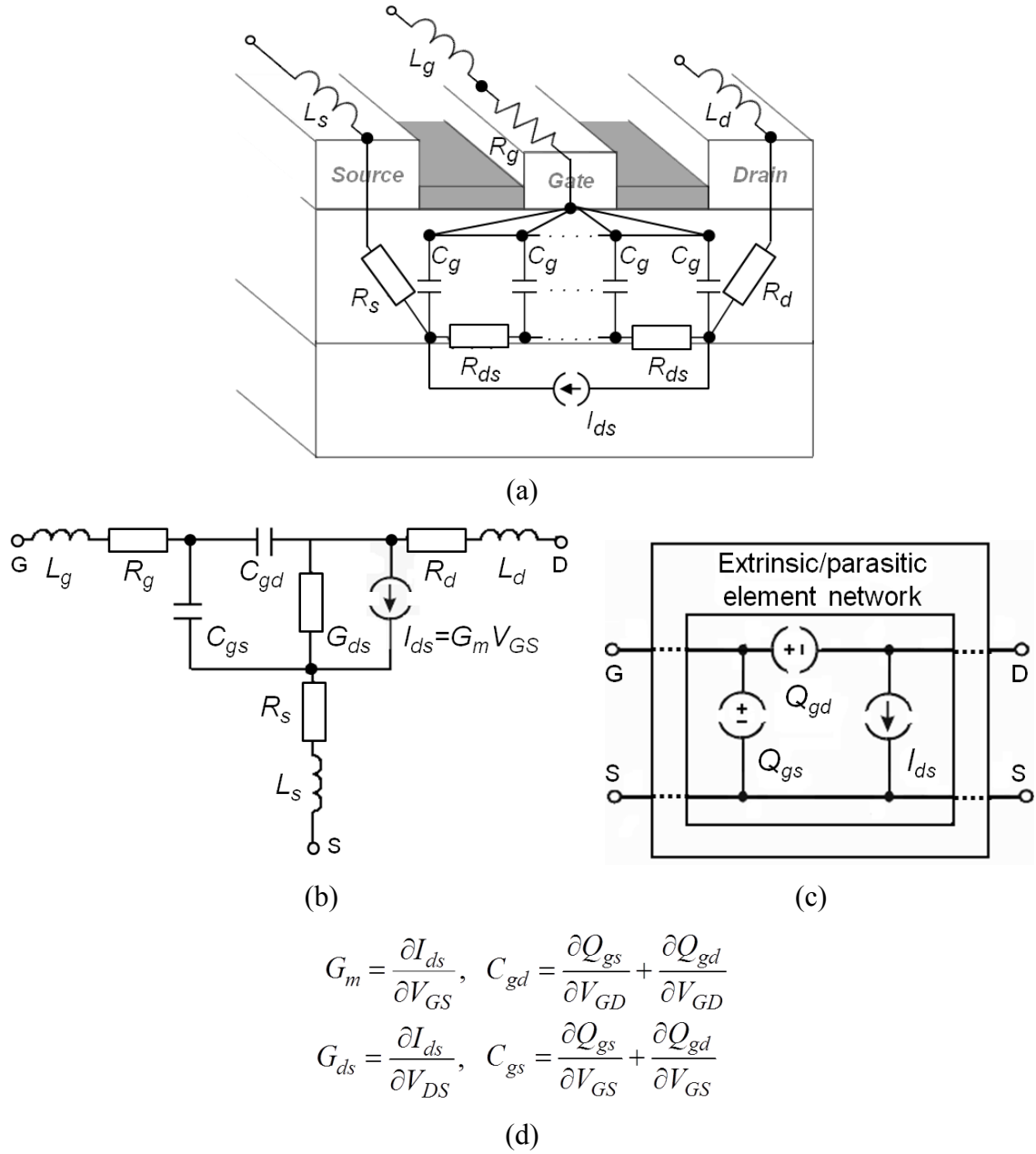


Figure 6.1 Typical formulation of the quasi-static charge model: (a) physical origin, (b) small-signal (b) and large-signal equivalent circuits, (d) voltage-dependent relationships between small-signal capacitance and conductance parameters and large-signal current and charge sources.

6.2 Non-Quasi-Static Charge Modeling

Reference [107] demonstrated that as the frequency increases, the measured behavior of the transistor shows a lag in comparison with the

quasi-static model. The reference proved that the lag was caused by the disregard of transient effects inherent of the quasi-static formulation. As a result, delay mechanisms of the charge accumulation need to be added. Besides, it was observed that the transconductance G_m also shows a delay, due to the propagation time of the electrons in the conduction channel [108].

In models developed for HEMTs, current sources are usually added in the gate-source and gate-drain branches, I_{gs} and I_{gd} , to denote forward conduction of the gate-source diode and reverse breakdown of the gate-drain diode, respectively [8].

New formulations of the charge behavior, called non-quasi-static or dispersive models have been proposed to overcome the limitations of quasi-static models. The non-quasi-static equivalent circuits of Figure 6.2 were adopted in this thesis work, after [74]. The circuits represent the intrinsic transistor and must be embedded in the same network of linear extrinsic elements, which was discussed in the small-signal modeling.

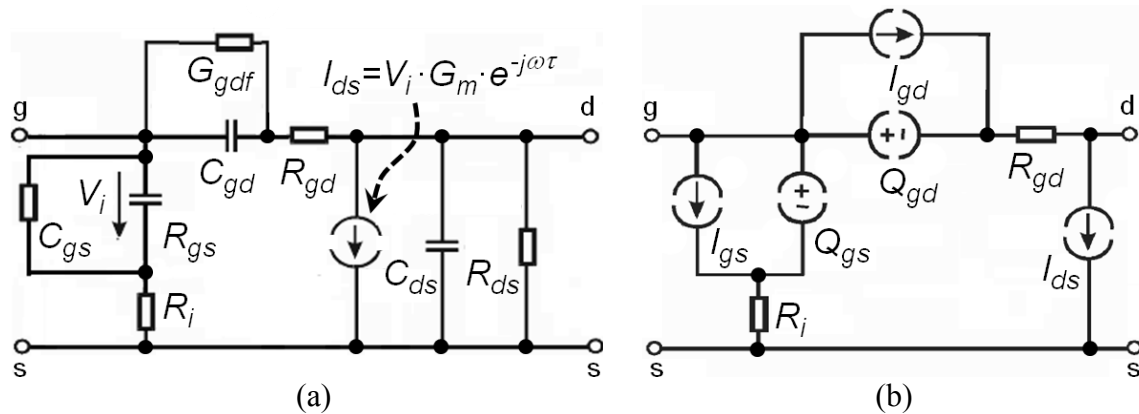


Figure 6.2 Non-quasi-static equivalent circuits adopted in this thesis work in the (a) small-signal and (b) large-signal models

A non-quasi-static formulation of the charge accumulation is provided in the equivalent circuits of Figure 6.2 with the gate-source and gate-drain resistances, R_i and R_{gd} . This formulation uses time constants of series-RC circuits ($R_i C_{gs}$ and $R_{gd} C_{gd}$) to account for the delays of the set-up of charge-storage effects under the gate, as first proposed in [109].

The non-quasi-static equivalent circuit adopted in this thesis work as small-signal model (shown in section 4.3, Figure 4.34, p. 114) corresponds to physical effects in small signal and also has a topology that agrees well with the non-quasi-static equivalent circuit of the large-signal model.

6.2.1 Large-Signal Charge Sources

The relationships between large-signal charge sources and small-signal intrinsic capacitance parameters are expressed as follows, after [110]:

$$Q_{gs}(V_{gs}, V_{ds}) = \int_{(V_{gs0}, V_{ds0})}^{(V_{gs}, V_{ds})} C_{gs} dV_{gs} + \int_{(V_{gs0}, V_{ds0})}^{(V_{gs}, V_{ds})} C_{ds} dV_{ds} \quad (6.1)$$

$$Q_{gd}(V_{gs}, V_{ds}) = \int_{(V_{gs0}, V_{ds0})}^{(V_{gs}, V_{ds})} C_{gd} dV_{gs} + \int_{(V_{gs0}, V_{ds0})}^{(V_{gs}, V_{ds})} (-C_{gd} - C_{ds}) dV_{ds} \quad (6.2)$$

The values of V_{gs0} and V_{ds0} represent the integration starting point. In reference [110] it was established that these integrals are path-independent, so that V_{gs0} and V_{ds0} can be chosen arbitrarily in the V_{gs} - V_{ds} grid.

Small-signal intrinsic parameter extraction was carried out in section 5.2.1, and the obtained dependencies on V_{DS} and V_{GS} were shown in Figure 5.7 and Figure 5.8. V_{DS} and V_{GS} denote the bias voltages applied to the contacting pads of the devices, which in the equivalent circuits correspond to the device ports outside the extrinsic parameters. Therefore, in this thesis, V_{DS} and V_{GS} are called extrinsic voltages. The voltages that appear at the ports of the intrinsic transistor are called intrinsic voltages and are denoted by V_{ds} and V_{gs} .

The intrinsic voltages are obtained from V_{DS} and V_{GS} as follows [111]:

$$V_{ds} = V_{DS} - (R_d + R_s)I_{ds} - R_s I_{gs} \quad (6.3)$$

$$V_{gs} = V_{GS} - (R_g + R_s)I_{gs} - R_s I_{ds} \quad (6.4)$$

The voltage remapping expressed by (6.3) and (6.4) was evaluated with extracted values of R_g , R_d and R_s of the 3.2-mm device, and with the measured voltages and currents from the static- DC IV characteristics of the same device.

Results of this voltage remapping are illustrated in Figure 6.3, where the original V_{GS} - V_{DS} grid, shown with black dots, is overlapped with the received V_{gs} - V_{ds} grid, shown with red circles.

Note that in Figure 6.3, V_{gs} - V_{ds} points appear shifted to lower voltage values with respect to the related V_{GS} - V_{DS} points, for $V_{ds} > 0V$ and for V_{gs} values outside the pinch-off region (i.e. $V_{gs} > V_{th}$, where $V_{th} = -3.3V$). That observation agrees with the inspection of equations (6.3) and (6.4) that represent voltage drops on R_g , R_d and R_s .

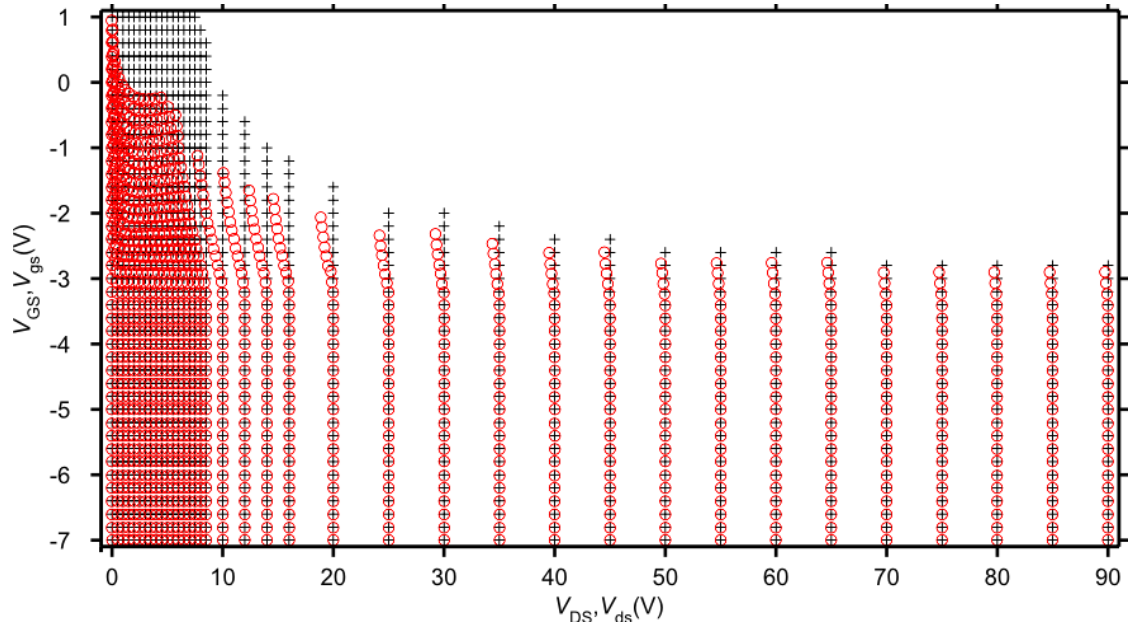


Figure 6.3 Results of voltage remapping for the 3.2-mm device showing the original orthogonal V_{GS} - V_{DS} grid (black crosses) overlapped with received non-orthogonal V_{gs} - V_{ds} grid (red circles).

Figure 6.4 depicts the previously extracted C_{gs} values of the 3.2-mm device expressed on the non-orthogonal V_{gs} - V_{ds} grid received after voltage remapping (instead of expressed on the original bias voltage grid V_{GS} - V_{DS}).

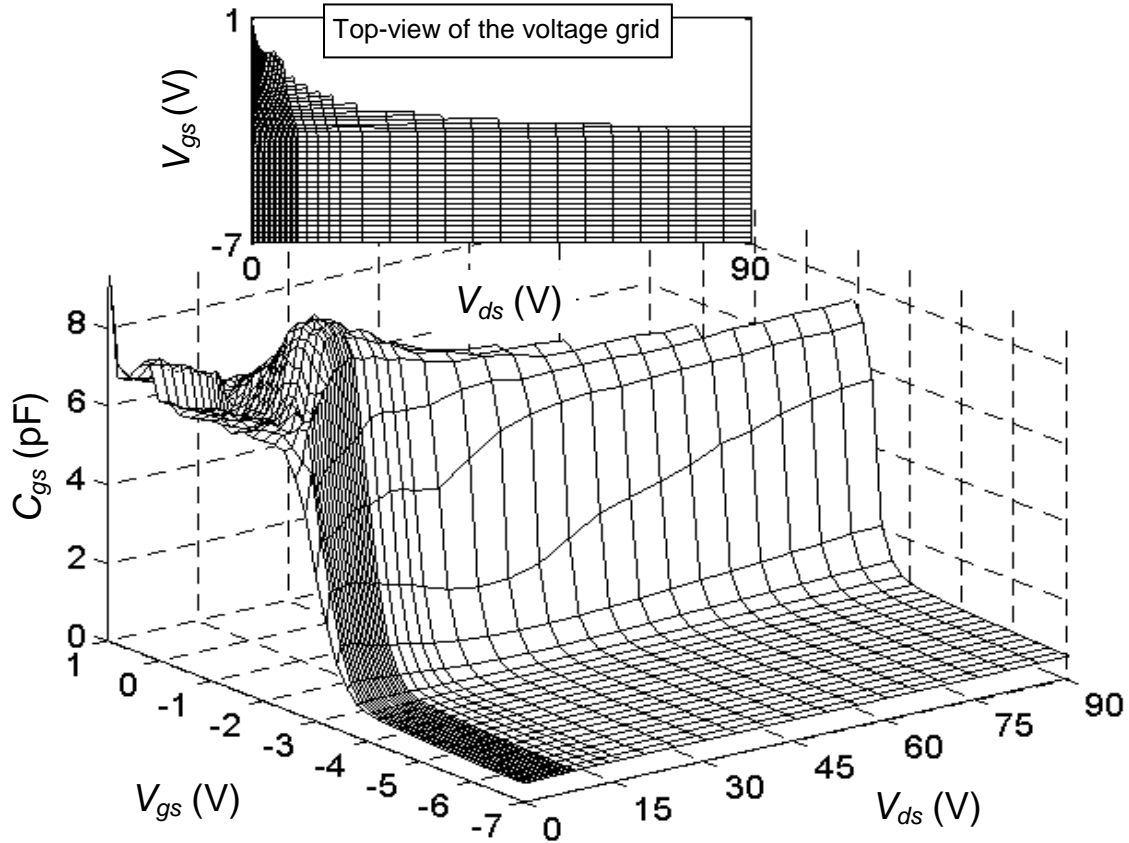


Figure 6.4 Extracted C_{gs} values of the 3.2-mm device, with their dependency on the applied DC voltages expressed on the received non-orthogonal V_{gs} - V_{ds} grid.

It is evident in Figure 6.3 and Figure 6.4 that there are no data points with simultaneous high- V_{GS} and high- V_{DS} values, due to the observation of the DC power limit (P_{DSmax}^{SOA}) by the bias points employed during S-parameters measurements.

In this thesis, grid regions without data points are called *off-range* regions. In this thesis work, when bias dependent parameters were handled as Matlab[®] array variables or stored as text-file tables, cells of the array or table that correspond to data points in the *off-range* region were given the string “NaN” (this is the native way in Matlab[®] to indicate a *not-a-number* or not-available value when executing calculation/visualization routines).

Figure 6.3 and Figure 6.4 demonstrate that the V_{gs} - V_{ds} grid received of the voltage remapping is non-orthogonal. Bias-dependencies of C_{gs} , C_{gd} and C_{ds} must be expressed on an orthogonal V_{gs} - V_{ds} grid to calculate Q_{gs} and Q_{gd} with the integrals of equations (6.1) and (6.2). Thus, a numerical re-gridding must be carried out on the voltage-dependent C_{gs} , C_{gd} and C_{ds} that are expressed on non-orthogonal V_{gs} - V_{ds} grids (after the remapping).

Figure 6.5 is an illustration of the data before and after the re-gridding process: the circles represent the available data points that belong to a non-orthogonal grid, whereas the squares denote the desired data points whose grid is already orthogonal. The filled squares are desired points that require interpolation, but for the hollow ones extrapolation must be employed.

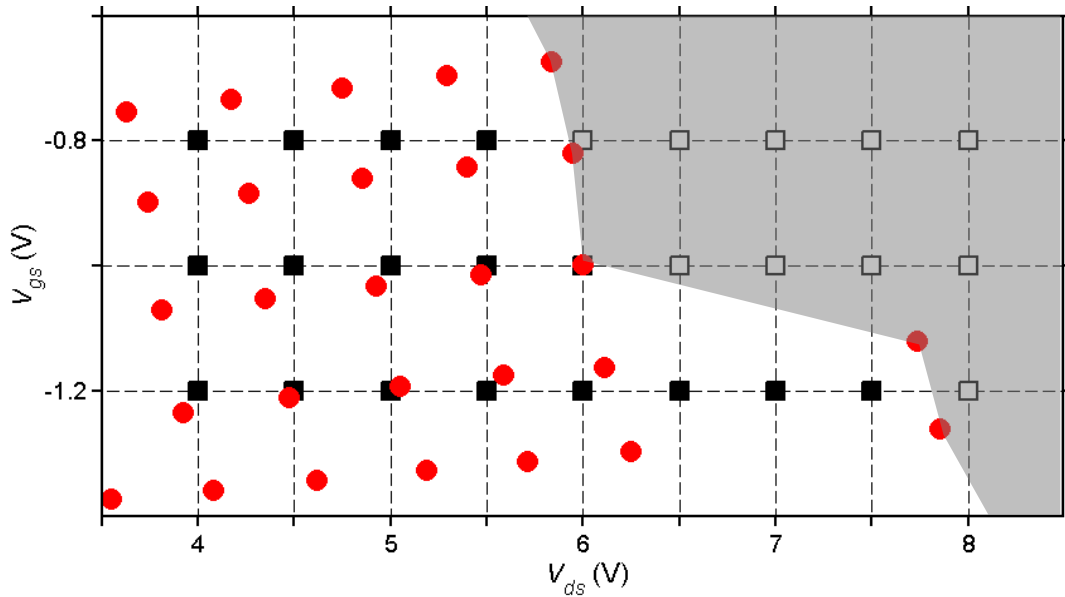


Figure 6.5 Illustration of the data before and after re-gridding: the circles are the non-orthogonal available data points and the squares the desired orthogonal data points. The filled squares require interpolation and the hollow extrapolation. The *off-range* region of the available data is shown shaded.

In this thesis work, the re-gridding was implemented with a Matlab[®] routine developed in [64] that interpolates using a *b-spline* approximation technique. *B-spline* approximation techniques are preferred over other techniques, like polynomial or Bezier, for their high approximation accuracy to supplied data and the continuity of high-order derivatives of the received data [64]. On another hand, using *b-spline* approximation techniques to extrapolate has been proven to produce unreliable values, in many numerical implementations in thesis work. Figure 6.6 illustrates with encircled zones unreliably extrapolated values that were produced by this approximation technique, probably due to the high nonlinearity of the data and the related piece-wise approximation done by *splines* [64].

The required re-gridding only implies interpolation, so that the path-integral formulation can be applied. Observe that in the illustration of Figure 6.5, the desired data points that need extrapolation belong to the *off-range* region. This region is considered out of scope of the present modeling strategy and the related data points are not relevant.

A problem arises in the praxis, since the employed Matlab[®] routine automatically applies the *b-spline* approximation technique to extrapolate values in the *off-range* region. Nevertheless, undesired extrapolation by the routine does not occur if the routine is forced (configured) to assign a “NaN” value to the data points of the *off-range* region.

A Matlab[®] variable must be provided in the call of the re-gridding routine that indicates to it the extension of the *off-range* region in the desired orthogonal grid [64]. Inputting this variable to the routine suitably configures it to assign “NaN” values to data points of the indicated *off-range* region.

In [64, 111] the re-gridding routine was configured to prevent undesired extrapolation, inputting a Matlab[®] array containing the original V_{GS} - V_{DS} grid in the call of the routine as indication of the *off-range* region. That array has “NaN” values assigned to those bias points where S-parameter measurements were not performed.

However, the results of such implementation of the re-gridding routine that are presented in Figure 6.6 still show unreliable values due to extrapolation (encircled zones in the figure). The non-orthogonal available data given to the routine for re-gridding were the voltage-dependent values of C_{gs} expressed on the original V_{gs} - V_{ds} grid, as shown in Figure 6.4.

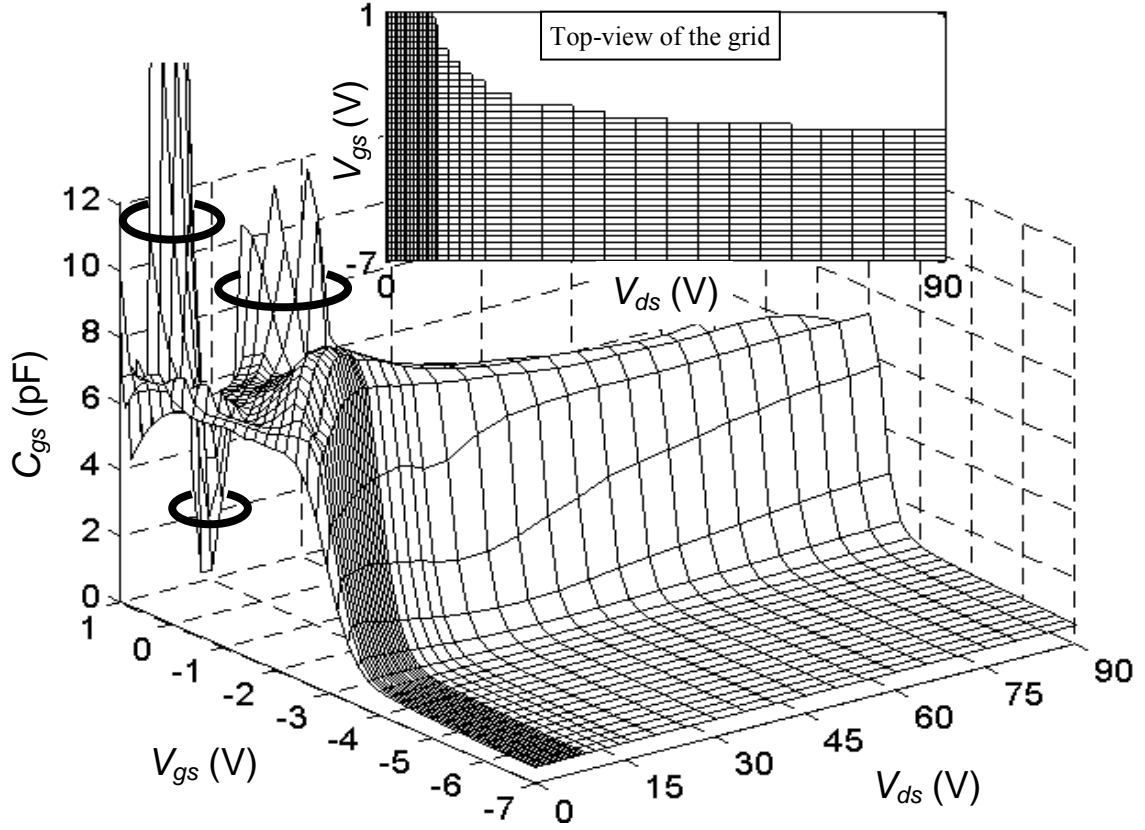


Figure 6.6 Re-gridded voltage-dependency of the C_{gs} values expressed on the V_{gs} - V_{ds} grid encircling unreliable values due to extrapolation. Inset: top-view of the orthogonal grid and with off-range region defined by the DC power limit (an array that contained the V_{GS} - V_{DS} grid was used to indicate the *off-range* region to the re-gridding routine).

Clearly, in the V_{GS} - V_{DS} grid the *off-range* region is directly defined by the DC power limit, but this limit is shifted by the voltage remapping indicated by equations (6.3) and (6.4), as can be observed in Figure 6.7.

In Figure 6.7 the DC power limit is shown with a square-marked line, the resulting shifted limit after voltage remapping is shown with an X-marked line, and an approximated function for the shifted limit is shown with a solid line.

In this thesis work, the DC power limit shifted after voltage remapping was approximated with the Matlab[®] function *interp1* [112], creating the Matlab[®] variable to be provided in the call of the re-gridding routine. The shifted DC power limit describes correctly the *off-range* region in the desired orthogonal V_{gs} - V_{ds} grid.

Results of such implementation of the re-gridding routine are presented in Figure 6.8. Note that the data was correctly re-gridded without appearance of unreliable values, confirming that the routine was properly configured to prevent extrapolation.

The non-orthogonal available data given to the routine for re-gridding were the voltage-dependent values of C_{gs} expressed on the original V_{gs} - V_{ds} grid, as shown in Figure 6.4.

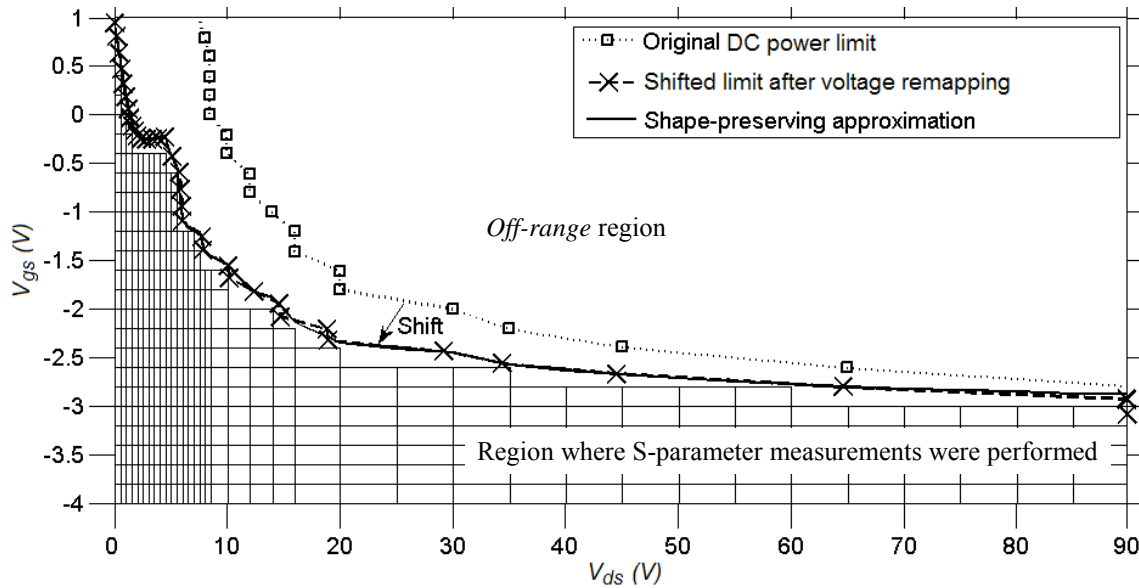


Figure 6.7 Shift of the DC power limit and the related approximated function obtained.

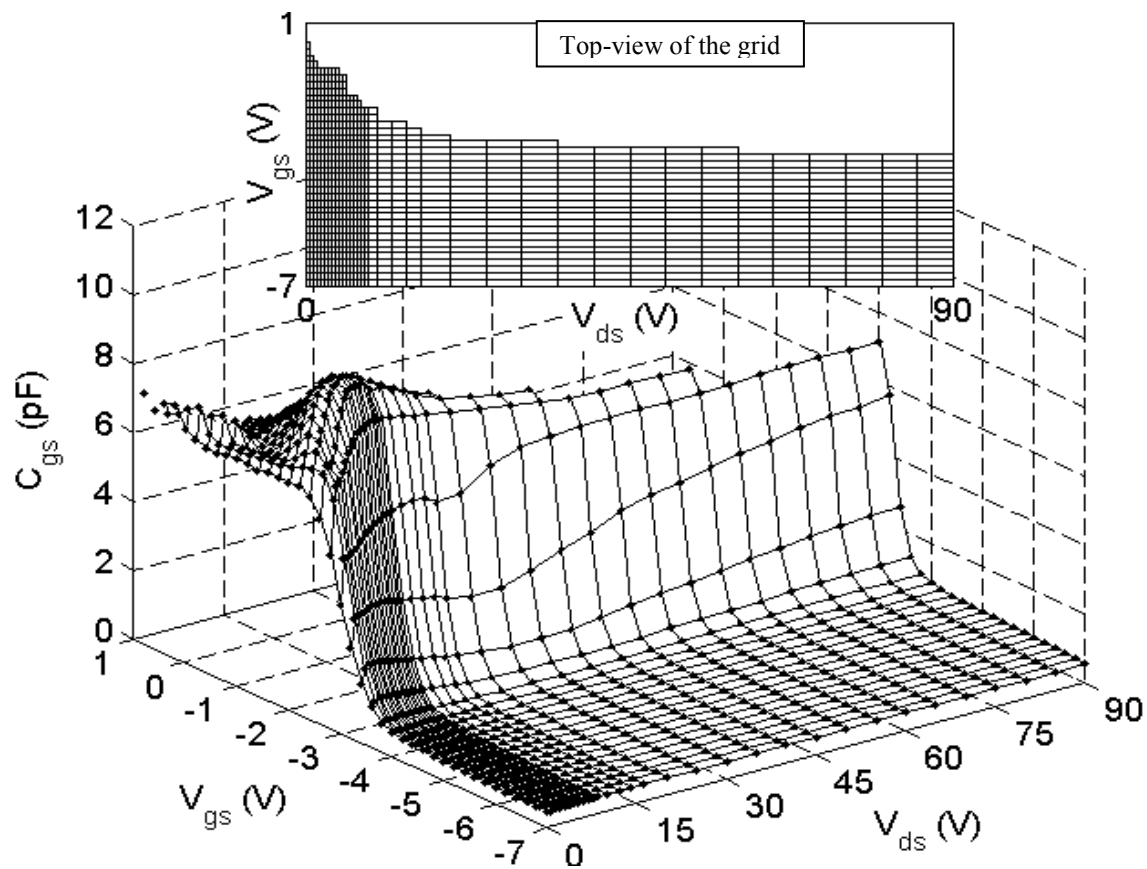


Figure 6.8 Improved re-gridded voltage-dependency of the C_{gs} values expressed on the V_{gs} - V_{ds} grid. Inset: top-view of the grid showing orthogonality and the *off-range* region defined by the shifted limit (a Matlab[®] variable with a functional approximation of the shifted DC power limit to indicate the *off-range* region to the re-gridding routine).

Comparing the results shown in Figure 6.8 and Figure 6.6 demonstrates the improved numerical quality obtained for the C_{gs} , C_{gd} and C_{ds} voltage-dependencies when the re-gridding routine uses the shifted DC power limit to indicate the *off-range* region. The improvement in numerical quality of the C_{gs} , C_{gd} and C_{ds} voltage-dependencies has dramatic effect in the reliability of the integration results for Q_{gs} and Q_{gd} . This is demonstrated by comparing the results shown in Figure 6.9 and Figure 6.10.

In Figure 6.9, the basis for the calculation of Q_{gs} and Q_{gd} were C_{gs} , C_{gd} and C_{ds} re-gridded indicating the *off-range* region to the re-gridding routine by a Matlab[®] array that contained the original V_{GS} - V_{DS} grid, as done in [111] (e.g. C_{gs} as shown in Figure 6.6).

In contrast, in Figure 6.10, the basis for the calculation of Q_{gs} and Q_{gd} were C_{gs} , C_{gd} and C_{ds} re-gridded with improved numerical quality, indicating the *off-range* region to the re-gridding routine by a functional approximation for shifted DC power limit (e.g. C_{gs} as shown in Figure 6.8).

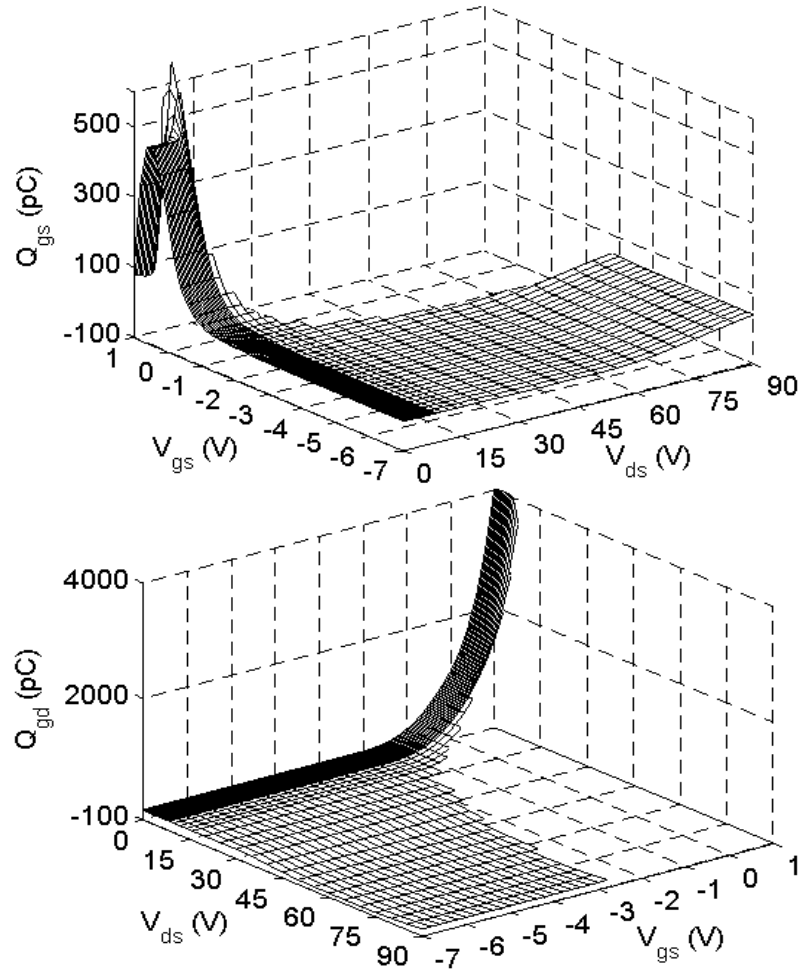


Figure 6.9 Voltage-dependencies of Q_{gs} and Q_{gd} calculated for the 3.2-mm device based on C_{gs} , C_{gd} and C_{ds} re-gridded using the Matlab[®] variable containing the V_{GS} - V_{DS} grid in the call of the re-gridding routine to prevent extrapolation as done in [64, 111].

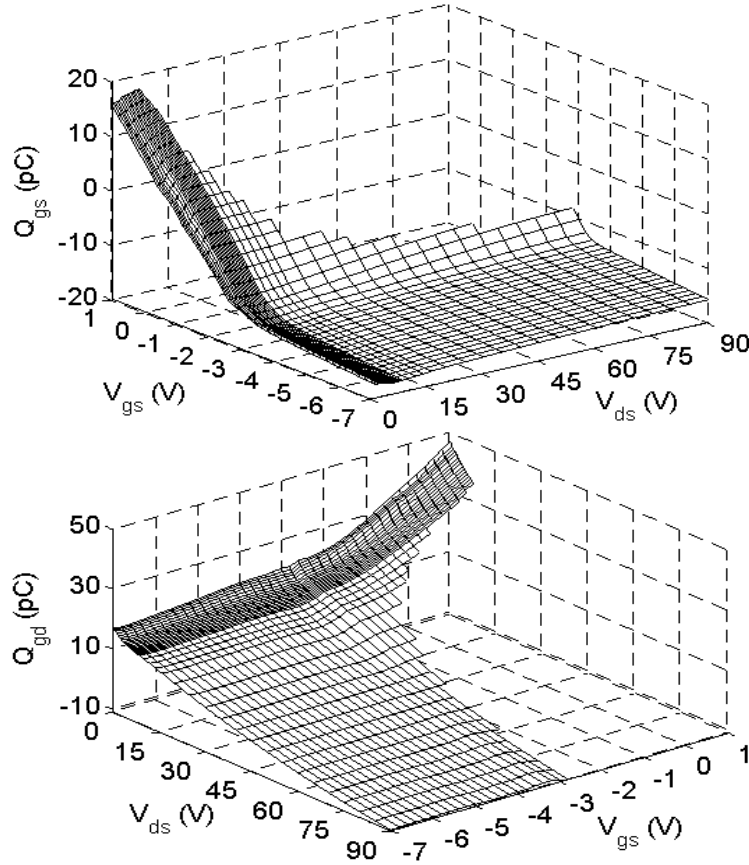


Figure 6.10 Voltage-dependencies of Q_{gs} and Q_{gd} calculated for the 3.2-mm device based on C_{gs} , C_{gd} and C_{ds} re-gridded using the newly created Matlab[®] variable for the shifted limit in the call of the re-gridding routine to prevent extrapolation.

The results for Q_{gs} and Q_{gd} that are shown in Figure 6.9 exhibit unreliable values for the grid region with the largest V_{gs} values, e.g. $V_{gs} > 0V$. In contrast, the results shown in Figure 6.10 present reliable Q_{gs} and Q_{gd} values in the whole V_{gs} - V_{ds} orthogonal grid.

The improved reliability of Q_{gs} and Q_{gd} shown in Figure 6.10 allows the interpolation of those voltage-dependencies to any desired grid density or to uniform grid spacing, and also a correct extrapolation to cover the *off-range* region, i.e. the full V_{gs} - V_{ds} grid. Results of interpolation to a denser equally-spaced grid and of adequate extrapolation to cover the full V_{gs} - V_{ds} grid that were applied to the calculated Q_{gs} and Q_{gd} values of the 2-mm device are shown in Figure 6.11. Linear extrapolation was performed for the *off-range* region. It is uncommon that large-signal models are applied on bias points in the *off-range* region (high-power IV region), so the extrapolation is not strictly required regarding model accuracy. However, it is useful for model implementation in CAD-software when the voltage dependent parameters are represented with look-up tables, as in the models of this thesis work.

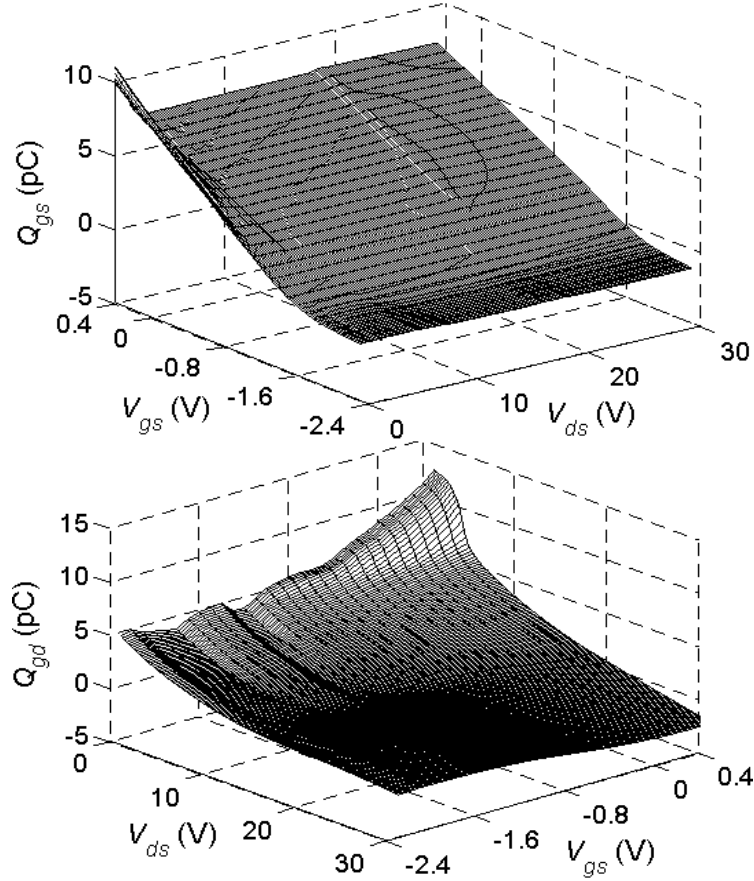


Figure 6.11 Voltage-dependencies of Q_{gs} and Q_{gd} calculated for the 2-mm device interpolated to a denser equally-spaced grid and extrapolated to the *off-range* region, based on C_{gs} , C_{gd} and C_{ds} re-gridded using the newly created Matlab[®] variable for the shifted limit in the call of the re-gridding routine.

6.2.2 Large-Signal Current Sources of the Gate Diodes

A similar integral formulation as for Q_{gs} and Q_{gd} was employed in this thesis work for the current sources I_{gs} and I_{gd} .

The corresponding path-integrals are related to the small-signal gate conductances G_{gsf} and G_{gdf} , as expressed by the following equations [110]:

$$I_{gs}(V_{gs}, V_{ds}) = \int_{(V_{gs0}, V_{ds0})}^{(V_{gs}, V_{ds})} G_{gsf} dV_{gs} \quad (6.5)$$

$$I_{gd}(V_{gs}, V_{ds}) = \int_{(V_{gs0}, V_{ds0})}^{(V_{gs}, V_{ds})} G_{gdf} dV_{gs} - \int_{(V_{gs0}, V_{ds0})}^{(V_{gs}, V_{ds})} G_{gdf} dV_{ds} \quad (6.6)$$

The G_{gsf} and G_{gdf} values originally extracted on the orthogonal V_{GS} - V_{DS} grid were re-gridded to express them on an orthogonal V_{gs} - V_{ds} grid, in the same way as presented in the previous section for C_{gs} , C_{gd} and C_{ds} .

Figure 6.12 and Figure 6.13 show the resulting voltage-dependent values of I_{gs} and I_{gd} calculated for the 2-mm device and for the 3.2-mm device, respectively.

The resulting I_{gs} and I_{gd} values exhibit the expected dependency on the applied DC voltages. They show significant effects mainly on the high- V_{gs} low- V_{ds} region, since their calculation is based on G_{gsf} and G_{gdf} , which presented their major effects in such a region.

For V_{gs} above 0V and increasing, I_{gs} agrees well with the expected exponential increase of the current of the gate-source diode when forward-biased. Similarly, for V_{gd} (i.e. $V_{gs} - V_{ds}$) above 0V and increasing, I_{gs} agrees well with the expected exponential increase of the current of the gate-drain diode when forward-biased.

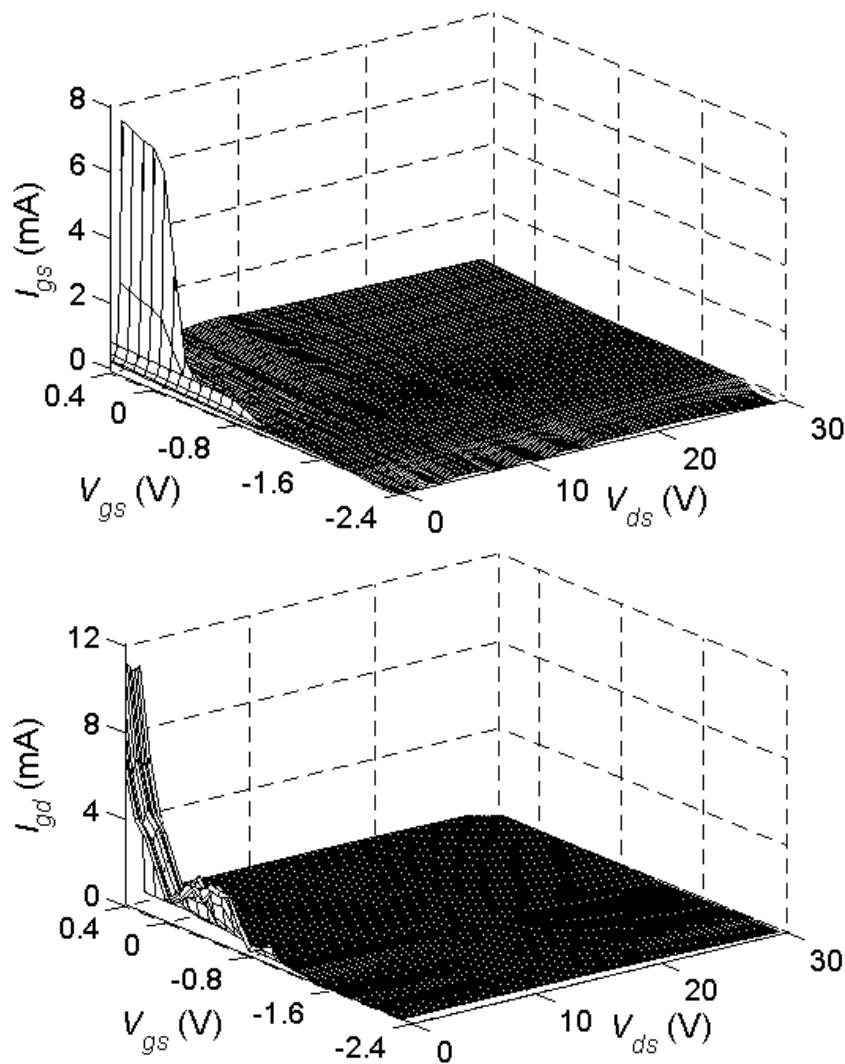


Figure 6.12 Voltage-dependencies of I_{gs} and I_{gd} calculated for the 2-mm device interpolated to a denser equally-spaced grid and extrapolated to the *off-range* region, based on G_{gsf} and G_{gdf} re-gridded using the newly created Matlab[®] variable for the shifted limit in the call of the re-gridding routine.

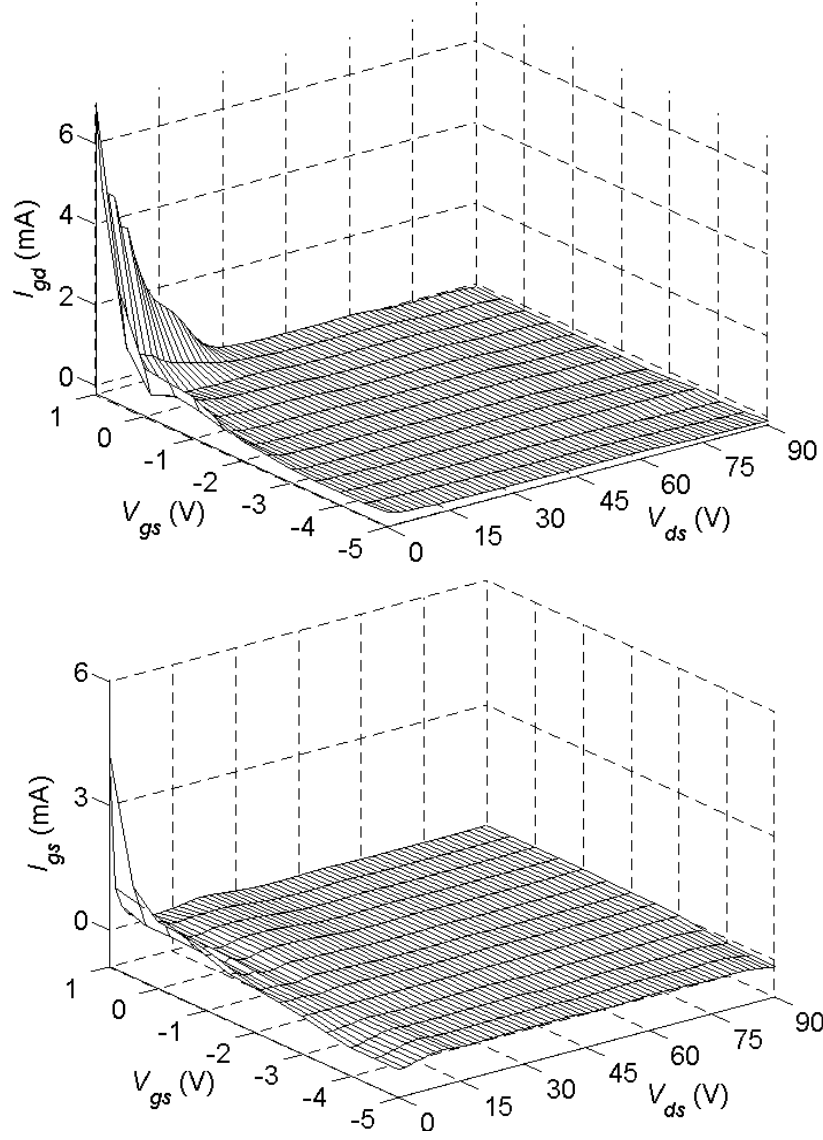


Figure 6.13 Voltage-dependencies of I_{gs} and I_{gd} calculated for the 3.2-mm device interpolated to a denser equally-spaced grid and extrapolated to the *off-range* region, based on G_{gsf} and G_{gdf} re-gridded using the newly created Matlab[®] variable for the shifted limit in the call of the re-gridding routine.

6.3 Modeling of I_{ds}

Certainly, the key nonlinear effect in the large-signal model is the drain-current source. For HEMTs it is well-known that dynamic effects of this current are more complex than those of the gate current, represented with displacement and conduction components.

As discussed in sections 2.3.1 and 2.3.3, I_{ds} shows complex dynamic effects because charge trapping and thermal phenomena of HEMTs cause variations of I_{ds} with the frequency of the RF signals handled, which is known as dispersion or dispersive behavior.

In short, quoting [113], I_{ds} is affected by: (i) low-frequency dispersive phenomena, due to device self-heating and charge trapping, and (ii) high-frequency non-quasi-static effects, related to spatial delays of the charge to rearrange the 2DEG. Transient or dynamic effects when attributed to charge trapping and self heating are known as long-term memory effects, and when attributed to non-quasi-static phenomena are known as short-term memory effects.

The parameter τ stands for the propagation time of electrons in the 2DEG and represents non-quasi-static effects of I_{ds} . However, an additional model formulation for the drain current is required to account for low-frequency dispersion induced by charge-trapping and self-heating effects, that is, for long-term memory effects whose time constants are longer than the period of the RF signal. Pulsed-DC IV measured from a *quiescent* bias point is related to the device RF response on that bias point.

In consequence, as suggested in [114], measured data of pulsed-DC IV represents a suitable database for the large-signal modeling of I_{ds} in measurement-based models, with the objective of describing accurately dispersion induced by charge-trapping and self-heating effects.

6.3.1 Definitions and Assumptions of the Adopted I_{ds} Model

In [115], Filicori *et al.* proposed an empirical I_{ds} model for GaAs MESFETs based on pulsed-DC IV measurements. The following equation is the expression presented in that reference for the I_{ds} model:

$$\begin{aligned} I_{ds}(v_{gs}, v_{ds}) = & I_{ds}^{Iso}(v_{ds}, v_{ds}) + f_G(v_{ds}, v_{ds}) \cdot (v_{gs} - V_{gs}) + \\ & + f_D(v_{gs}, v_{ds}) \cdot (v_{ds} - V_{ds}) + \\ & + f_{th}(v_{gs}, v_{ds}) \cdot \Delta T_{ch} \end{aligned} \quad (6.7)$$

where

$$\Delta T_{ch} = T_{ch} - T_{ch}^* = R_{th} \cdot P_{ds} + (T_C - T_C^*). \quad (6.8)$$

The next are the key model definitions and assumptions given in [115]:

Definition 1: v_{gs} and v_{ds} are voltage signals at the intrinsic ports of the device. The average values of these signals are denoted by V_{gs} and V_{ds} and their alternate (i.e. time-varying) components are equal to $(v_{gs} - V_{gs})$ and $(v_{ds} - V_{ds})$.

Definition 2: P_{ds} is the average value of the instantaneous dissipated power, that is, the mean value of the signal of power p_{ds} , present in the intrinsic drain-source port.

Assumption 1: Contributions of the gate current to the dissipated power of the device are neglected. This assumption is valid for typical operation, on bias points where p_{ds} is notably larger than power at the gate-source port.

Definition 3: T_{ch} denotes the average temperature of the channel and T_C the average temperature of the metallic surface subjacent to the device (i.e. *thermo-chuck* of the probing station). T_C is usually known as *case temperature*. The variables with the superscript “*” denote initial values. R_{th} stands for the thermal resistance of the device, defined as the variation with respect to P_{ds} of the difference between the channel temperature T_{ch} and the *case temperature* T_C .

Assumption 2: The signal frequencies of v_{gs} and v_{ds} are higher than the upper cut-off frequency of the low-frequency dispersive phenomena (self-heating and charge-trapping effects), but are low enough to neglect microwave reactive effects of the gate charge or propagation times of the electrons in the channel, according to Filicori *et al.* [115]. Therefore, charge-trapping and thermal states do not change as swiftly as the voltage signals and are assumed fixed to their average condition.

Assumption 3: The average values of charge-trapping and thermal states are assumed to depend only on V_{gs} , V_{ds} and P_{ds} (average values of v_{gs} , v_{ds} and p_{ds}). This assumption implies that there is no significant AC-to-DC conversion in the relation between the signals v_{gs} and v_{ds} and the charge-trapping states. In consequence, as stated in [115], the average value of the charge-trapping states “*is not significantly affected by the amplitude or shape of the alternate components ($v_{gs}-V_{gs}$) and ($v_{ds}-V_{ds}$)*”. This model assumption appears in other I_{ds} models [116-119], and has been confirmed experimentally, as in the results reported in [120, 121].

Assumption 4: The expression of the I_{ds} model is a first-order Taylor series expansion, i.e. a functional *linearization*, with respect to V_{gs} , V_{ds} and T_{ch} . This assumption implies a linear or mildly nonlinear dependence of the average values of the thermal and charge-trapping states on V_{gs} and V_{ds} . The series expansion is made around the operation condition characterized by the static-DC voltages V_{gs}^* , V_{ds}^* and the steady-state channel temperature T_{ch}^* . Equation (6.7) is ultimately obtained from the first-order

series expansion (i.e. *linearization*) by incorporating the following model definitions 4 to 6.

Definition 4: $I_{ds}^{Iso}(v_{gs}, v_{ds})$ represents a theoretical isothermal DC IV characteristic of an operation with constant channel temperature.

Definition 5: The functions $f_D(v_{gs}, v_{ds})$ and $f_G(v_{gs}, v_{ds})$ represent the differences between dynamic and static I_{ds} due to charge trapping, for each pair of instantaneous voltages v_{gs}, v_{ds} applied to the device.

Definition 6: The function $f_{th}(v_{gs}, v_{ds})$ represents the differences of the dynamic I_{ds} with respect to an isothermal DC characteristic due to changes of heat in the device.

The I_{ds} model for constant *case temperature* ($T_C = T_C^*$) is given by:

$$\begin{aligned} I_{ds}(v_{gs}, v_{ds}) = & I_{ds}^{Iso}(v_{ds}, v_{ds}) + f_G(v_{ds}, v_{ds}) \cdot (v_{gs} - V_{gs}) + \\ & + f_D(v_{gs}, v_{ds}) \cdot (v_{ds} - V_{ds}) + \\ & + f_{th}(v_{gs}, v_{ds}) \cdot R_{th} \cdot P_{ds} \end{aligned} \quad (6.9)$$

For constant *case temperature*, $f_{th} \cdot R_{th}$ is condensed as f_P and the model does not strictly identify the thermal resistance separately. Then, equation (6.9) becomes:

$$\begin{aligned} I_{ds}(v_{gs}, v_{ds}) = & I_{ds}^{Iso}(v_{ds}, v_{ds}) + f_G(v_{ds}, v_{ds}) \cdot (v_{gs} - V_{gs}) + \\ & + f_D(v_{gs}, v_{ds}) \cdot (v_{ds} - V_{ds}) + \\ & + f_P(v_{gs}, v_{ds}) \cdot P_{ds} \end{aligned} \quad (6.9a)$$

The bias-dependent parameters of this model are related to the surface traps (mostly dependent on the gate voltage), buffer traps (mostly dependent on the drain voltage) and the self-heating effect (dependent on the power dissipation of the DC bias point)

In typical static-DC operation that is non-isothermal, $I_{ds} = I_{DC}$, $v_{gs} = V_{gs}$, $v_{ds} = V_{ds}$ and $P_{ds} = I_{DC}V_{ds}$. Applying such equivalences to equation (6.9a) for the model with constant *case temperature*, the following expression is received for the static-DC IV characteristics:

$$I_{DC} = \frac{I_{ds}^{Iso}(v_{gs}, v_{ds})}{1 - f_P(v_{gs}, v_{ds}) \cdot V_{ds}} \quad (6.10)$$

6.3.2 Electro-Thermal Modeling

Equation (6.8) describes the relationship between the change in the channel temperature with respect to the average dissipated power and the change of the *case temperature*. In the sense of classical heat transfer analysis, the thermal resistance is the temperature difference across a device when a unit of heat energy flows through its structure in a unit of time.

In the adopted I_{ds} model, the *thermal resistance* is considered constant with respect to P_{ds} , because the dependency of the thermal state (self-heating phenomena) on the static-DC bias point is already represented in the parameter f_{th} . So, R_{th} agrees well with the classical definition.

However, if the electrical power in the device is function of the frequency so that the dissipated power is denoted by $P_{ds}(\omega)$, then, this frequency-dependency is passed to the change in the channel temperature, and hence, it is correct to discuss a *thermal impedance* Z_{th} , instead of a *thermal resistance* R_{th} . In the original source of the adopted I_{ds} model, reference [115], there is no consideration of a thermal impedance or of the frequency-dependency of the dissipated power. The model formulation found in [115] suggest a first-order low pass filter (a single RC circuit) with the only purpose of calculating P_{ds} (the average value of the dissipated power) from the time-varying power signal p_{ds} .

In the general case of the adopted I_{ds} model, the frequency-dependence of the instantaneous dissipated power, $p_{ds}(\omega)$, must be considered for signals v_{gs} and v_{ds} with any given frequency, by taking into account the device *thermal impedance* Z_{th} .

When the *thermal impedance* Z_{th} is considered, the product $R_{th} \cdot P_{ds}$ (expressed explicitly in (6.8) and (6.9), and implicitly in (6.9a) and (6.10)) must be reformulated. The electro-thermal sub-circuit depicted in Figure 6.14, adopted from [79], shows the relationship proposed in this thesis work between the frequency-dependent dissipated power $p_{ds}(\omega)$, the *thermal impedance* and the produced temperature change ΔT .

In the electro-thermal sub-circuit of Figure 6.14, R_{th} and C_{th} form the *thermal impedance* Z_{th} and the implied time constant of the dispersive thermal phenomena, τ_{th} , is equal to $R_{th} \cdot C_{th}$.

Reference [111] used the electro-thermal sub-circuit of Figure 6.14 with an I_{ds} model also based on the ideas of Filicori *et al.* of [115], as the one

adopted model of this thesis work. However, the proposed values of R_{th} and C_{th} were not related to device characterization.

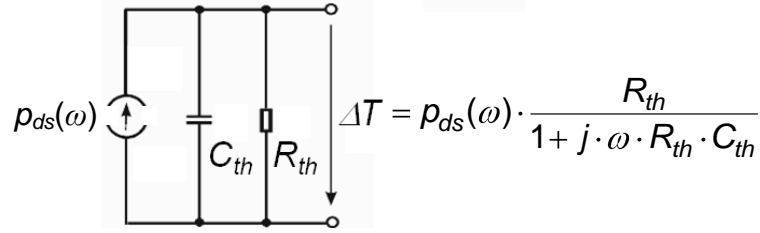


Figure 6.14 Electro-thermal sub-circuit used to represent frequency-dependent self-heating effects [79].

In a later I_{ds} model reported in [122], which also used the electro-thermal sub-circuit of Figure 6.14, R_{th} was calculated with a closed expression related to the device physics (gate finger width, finger spacing and thicknesses of active layers).

On another hand, Dahmani *et al.* presented in [103, 104] a method to calculate the electro-thermal parameters using heat-transfer simulations and numerical techniques. In [103, 104], the thermal profile of the transistor was obtained using a layer structure physically equivalent to that of the studied devices and implementing the heat equation numerically. The procedure takes into account the different types of heat-transfer mechanisms, the boundary conditions and the temperature-dependent thermal conductivities of the materials involved.

In [103, 104], R_{th} is obtained from steady-state DC simulations and the time constant τ_{th} from a transient simulation of DC power dissipation. Moreover, in their published work, Dahmani *et al.* have demonstrated that the parameter values of the electro-thermal sub-circuit calculated using their heat-transfer simulations agree well with values extracted based on measurements. Table 6.1, redrawn from [104], lists values for R_{th} and τ_{th} calculated by Dahmani *et al.* using their heat-transfer simulations and also based on measured data.

Table 6.1 Values of thermal resistance and thermal time constant calculated by Dahmani *et al.* based on measurements and with heat-transfer simulations. Table redrawn from [104].

Gate periphery of the studied device	0.5 mm	0.8 mm	3.2 mm
R_{th} ($^{\circ}\text{C}/\text{W}$) extracted based on measurements	-	-	6.40
R_{th} ($^{\circ}\text{C}/\text{W}$) calculated from heat-transfer simulations	-	19.6	8.35
τ_{th} (μs) extracted based on measurements	20	30.0	65.00
τ_{th} (μs) calculated from heat-transfer simulations	29	36.0	85.00

In this thesis work, the τ_{th} and R_{th} values obtained by Dahmani *et al.* for the studied 3.2-mm device (i.e. $\tau_{th} = 85 \mu s$ and $R_{th} = 8.35 \text{ }^\circ\text{C/W}$) have been used to complete the electro-thermal sub-circuit and to implement the I_{ds} model.

For the 2-mm device the layer structure data was unavailable and the heat-transfer simulations could not be reliably implemented to calculate R_{th} and τ_{th} . In consequence, the I_{ds} model for constant *case temperature* expressed by (6.9) was utilized, where $f_{th} \cdot R_{th}$ is condensed as f_P and the R_{th} value is not strictly needed. Then, the effect of R_{th} is properly taken away from the electro-thermal sub-circuit making R_{th} equal to $1 \text{ }^\circ\text{C/W}$, which implies that the C_{th} values expressed in $s \cdot W/^\circ\text{C}$ must be equal to the τ_{th} value in seconds, obtained from transient measurements.

6.4 Measurement-Based Extraction of I_{ds} -Model Parameters

According to [115], the adopted I_{ds} -model assumes that the v_{ds} and v_{gs} signal frequencies are higher than the upper cut-off frequency of the low-frequency dispersive phenomena due to self-heating and charge-trapping effects, but lower than microwave-related effects of junction charge-storage and propagation times (assumption 2 presented in section 6.3.1).

Pulsed-DC IV measurements are performed using voltage pulses for v_{gs} and v_{ds} with related signal frequencies that satisfy this model assumption.

In this thesis work, voltage pulse width of $0.1 \mu s$ was employed, equivalent to a signal frequency of 10 MHz. The period before repetition of the pulse was selected in 1 ms, equivalent to a pulse repetition frequency of 1 kHz. Then, the corresponding duty cycle was 0.01%.

The narrow pulse width and low duty cycle ensure that the voltage pulses change faster than the low-frequency dispersive phenomena and minimize heat accumulation from one pulse to the next. As a result, charge-trapping and self-heating effects are effectively dictated by the *quiescent* bias point of the pulsed-DC IV measurement.

6.4.1 Extraction of the Parameters I_{ds}^{Iso} , f_G and f_D

In this thesis work, as in [111, 115, 122, 123], voltage-dependent values of $I_{ds}^{Iso}(v_{gs}, v_{ds})$, $f_G(v_{gs}, v_{ds})$ and $f_D(v_{gs}, v_{ds})$ were extracted from pulsed-DC

IV measurements on passive *quiescent* bias points, i.e. with negligible P_{DS} . In such conditions the thermal-related parameter (f_{th} or f_P) vanishes.

The three passive *quiescent* bias points employed were: (i) $V_{GS} = 0V$ with $V_{DS} = 0V$, (ii) $V_{GS} < V_{th}$ with $V_{DS} = 0V$ and (iii) $V_{GS} < V_{th}$ with $V_{DS} \gg 0V$. The specific values of V_{GS} for (ii) and of V_{GS} and V_{DS} for (iii), for the studied large-size devices, were listed in Table 3.3 of subsection 3.2.3.3. The related pulsed-DC IV characterization results were also reported there.

The voltage-dependent values of $I_{ds}^{Iso}(v_{gs}, v_{ds})$, $f_G(v_{gs}, v_{ds})$ and $f_D(v_{gs}, v_{ds})$ that were calculated are shown in Figure 6.15 and Figure 6.16. Voltage-dependencies of I_{ds}^{Iso} that are shown in those figures present the expected shape of IV characteristics, but with nearly-constant values on the saturation region. This corresponds well with an ideal isothermal IV characteristic, which is the effect represented by I_{ds}^{Iso} .

The parameters $f_G(v_{gs}, v_{ds})$ and $f_D(v_{gs}, v_{ds})$ shown in Figure 6.15 for the 3.2-mm device have larger values than those shown in Figure 6.16 for the 2-mm device. This agrees with observations made during pulsed-DC IV characterization, in subsection 3.2.3.3, where charge-trapping effects appeared more pronounced for the 3.2-mm device than for the 2-mm device. As discussed in that subsection, device fabrication technology engineered by seems like the main reason for the lower charge-trapping effects observed of the 2-mm device.

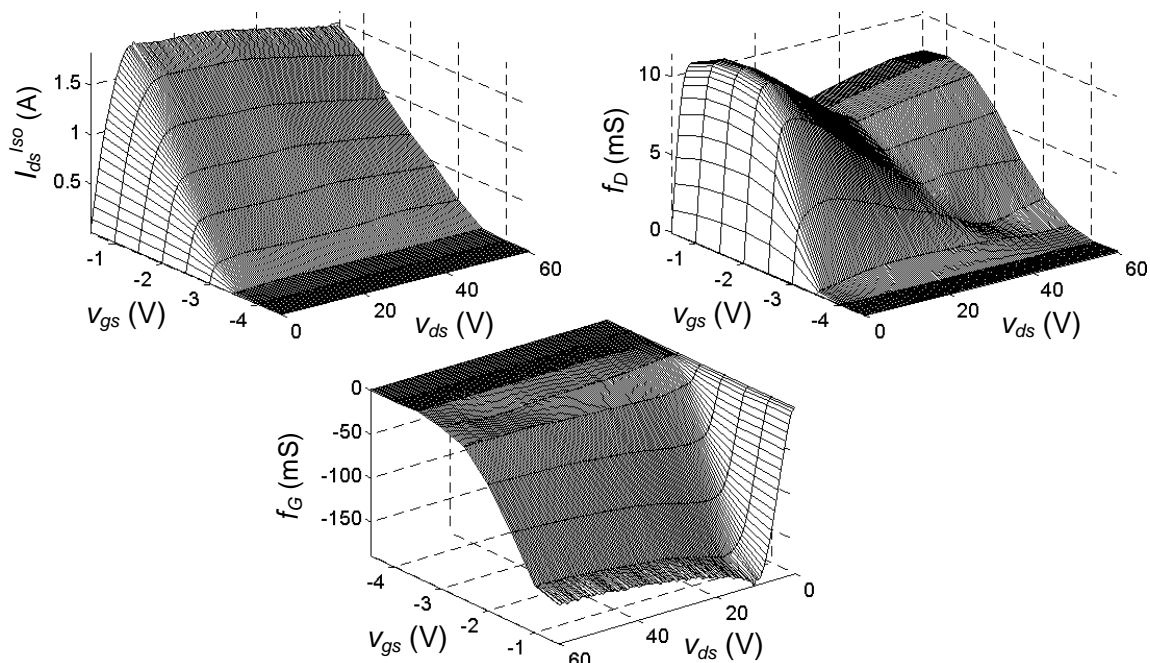


Figure 6.15 Calculated values of $I_{ds}^{Iso}(v_{gs}, v_{ds})$, $f_G(v_{gs}, v_{ds})$ and $f_D(v_{gs}, v_{ds})$ for the 3.2-mm device.

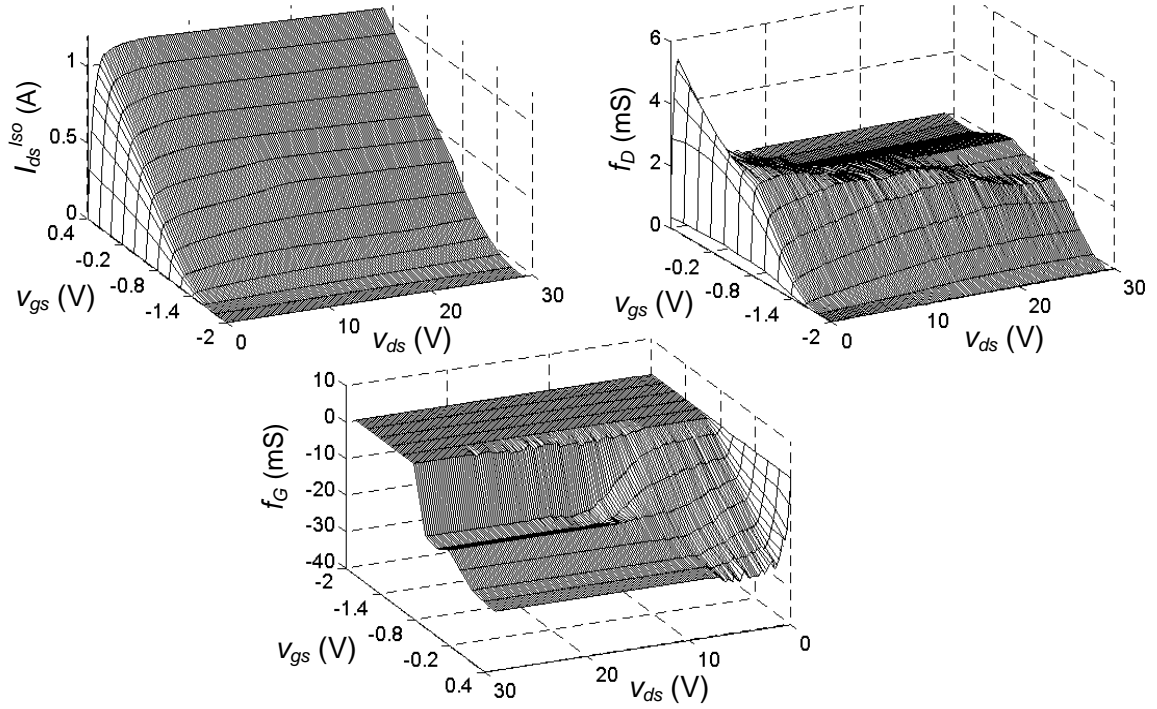


Figure 6.16 Calculated values of $I_{ds}^{Iso}(v_{gs}, v_{ds})$, $f_G(v_{gs}, v_{ds})$ and $f_D(v_{gs}, v_{ds})$ for the 2-mm device.

6.4.2 Extraction of the Parameters f_{th} and f_P

According to Filicori et al. [115], the thermal-related parameters of the I_{ds} -model $f_{th}(v_{gs}, v_{gs})$ or $f_P(v_{gs}, v_{gs})$ are calculated using a pulsed-DC IV measurement without self-heating effects as reference, typically $V_{GS} = 0V$ with $V_{DS} = 0V$, together with pulsed-DC IV measurements on active *quiescent* bias points (*quiescent* bias points with non-negligible P_{DS}).

Actually, in previous I_{ds} models based on the ideas of Filicori *et al.*, such as [111, 115, 123], f_P is calculated using pulsed-DC IV measurements on only one active *quiescent* bias point.

In the modeling developed in this thesis work for the studied large-size devices, calculating f_P with pulsed-DC IV measurements on a single active *quiescent* bias point resulted in models with strictly localized accuracy. This means that during model verification tests, the accuracy of those models rapidly degraded as the tested bias points moved away of the active *quiescent* bias used to calculate f_P .

According to [115], the expression of the adopted I_{ds} -model is a *linearization* with respect to V_{gs} , V_{ds} and T_{ch} , around a given operation condition (assumption 4 discussed in section 6.3.1). This model assumption

implies a linear or mildly nonlinear dependence of the average values of the thermal states on V_{gs} and V_{ds} .

In reality, if the actual dependency of the average values of the thermal states on the bias condition were as linear as assumed, the use of additional pulsed-DC IV measurements on different active *quiescent* bias points would not add linearly independent data to the calculation of f_P . Then, similar results could be expected independently of the number of different active *quiescent* bias points considered to calculate f_P .

However, in this thesis work, it was noted that considering additional pulsed-DC IV measurements on different active *quiescent* bias points improves the representation of self-heating effects by f_P and the extension of the model validity region. The region containing the bias points where the model is considered to produce accurate simulations is called model validity region.

Figure 6.17 depicts validity regions obtained for two modeling trials carried out for the 3.2-mm device that were tested comparing pulsed-DC IV measurements with model simulations. The only difference between the two models developed was the calculation of f_P .

As shown in Figure 6.17, the second modeling trial (part (b)) employed more pulsed-DC IV measurements and with a broader distribution on the IV plane than the first modeling trial (part (a)). As a result, an expansion of the model validity region was obtained for the second modeling trial with respect to the first one. Meanwhile, the accuracy of the related pulsed-DC IV verification tests was improved or preserved. The expansion of model validity region was directly related to the increasing number of active *quiescent* bias points that were considered to calculate f_P .

The high temperatures of operation (high levels of dissipated power) of the studied devices together with device properties related to the fabrication technologies are the reasons considered to explain why the thermal states of the device do not depend on V_{gs} and V_{ds} as linearly as assumed in the I_{ds} -model formulation.

In consequence, in this thesis work, the voltage-dependent values of $f_{th}(v_{gs}, v_{ds})$ and $f_P(v_{gs}, v_{ds})$ were calculated using pulsed-DC IV measurements on multiple active *quiescent* bias points, as listed in Table 6.2. The related pulsed-DC IV characterization results were reported subsection 3.2.3.3.

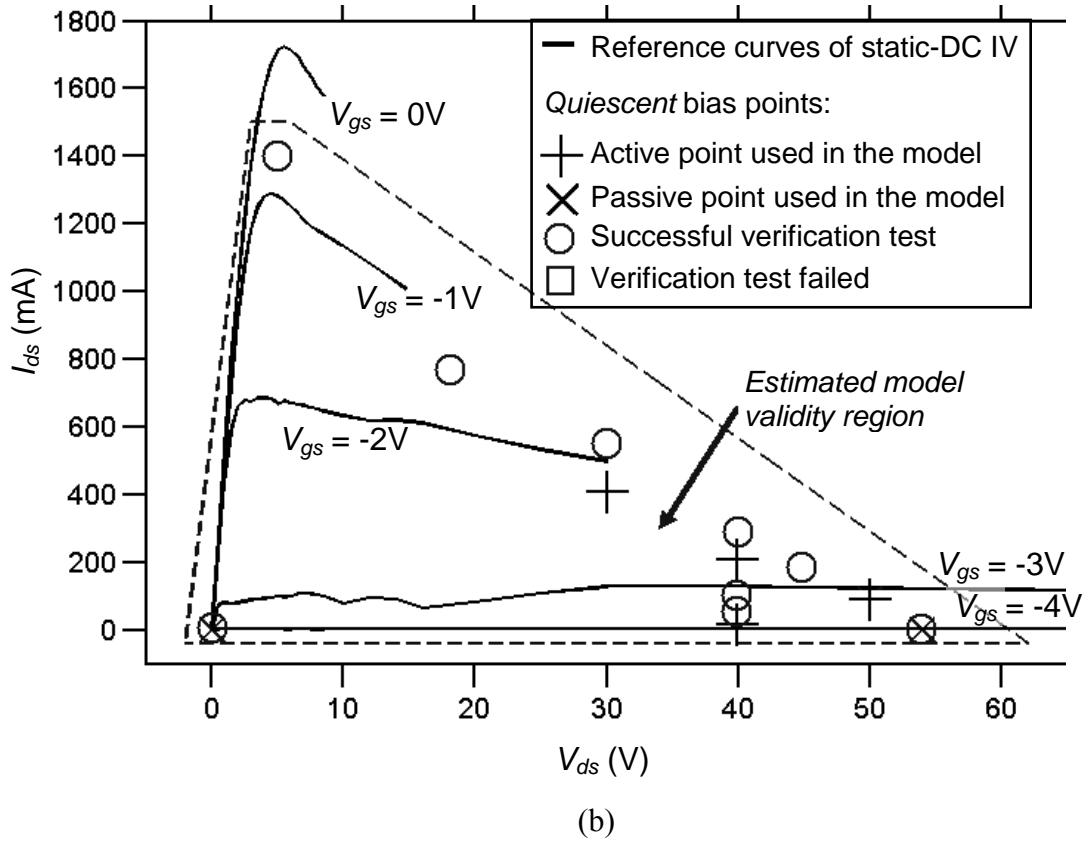
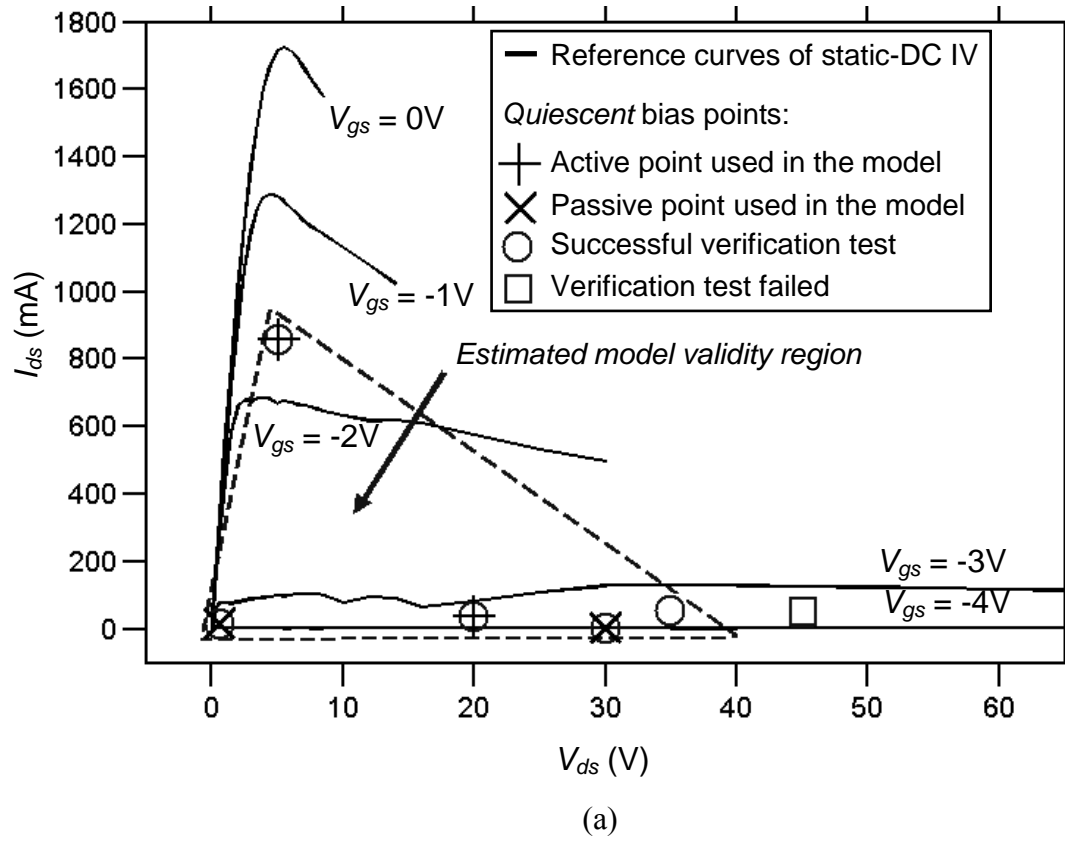


Figure 6.17 Validity regions for pulsed-DC IV verifications tests of models developed for the 3.2-mm device: (a) Model validity region considering only two active *quiescent* bias points for the calculation of f_p and (b) expanded model validity region considering additional active *quiescent* bias points for the calculation of f_p .

Table 6.2 *Quiescent* bias points with non-negligible P_{DS} employed in the calculation of $f_{th}(v_{gs}, v_{ds})$ for the 3.2-mm device and $f_P(v_{gs}, v_{ds})$ for the 2-mm device.

3.2-mm device			2-mm device		
V_{GS}	V_{DS}	P_{DS}	V_{GS}	V_{DS}	P_{DS}
-3.25V	50V	7.4W	-1.25V	15V	1.98W
-3V	40V	11.9W	-1V	22V	4.4W
-2.5V	30V	4.4W	-0.8V	10V	3W
			-1.6V	12V	0.25W
			-1.5V	5V	0.13W

The I_{ds} -model parameters related to self-heating effects that must be calculated are: (i) f_{th} for the model of the 3.2-mm device with R_{th} known and (ii) f_P for the model of the 2-mm device with R_{th} unknown. The calculated values of those parameters are presented in Figure 6.18 and Figure 6.19.

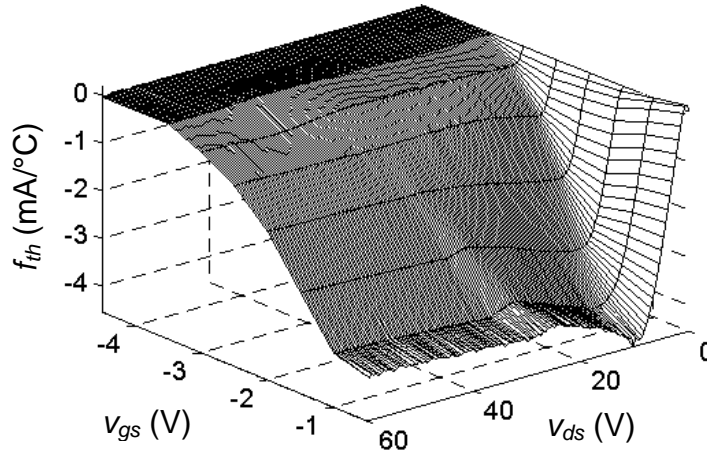


Figure 6.18 Calculated values of $f_{th}(v_{gs}, v_{ds})$ for the 3.2-mm device

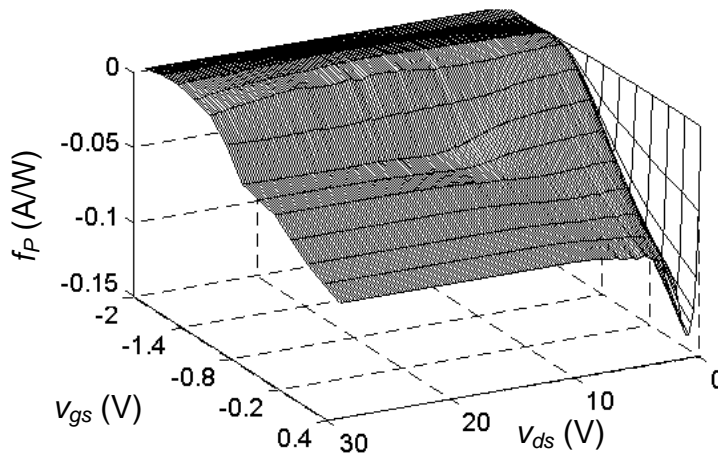


Figure 6.19 Calculated values of $f_P(v_{gs}, v_{ds})$ for the 2-mm device.

Note that the values of f_{th} in Figure 6.18 and f_P in Figure 6.19 were expressed in terms of v_{gs} and v_{ds} , corresponding to intrinsic voltages. But, pulsed-DC IV characteristics were measured in the extrinsic device ports and are in terms of v_{GS} and v_{DS} . Therefore, the pulsed-DC IV measurements

were remapped first to the intrinsic device ports using equations (6.3) and (6.4), before applying the parameter extraction, including the V_{GS} , V_{DS} and P_{DS} values that characterize the *quiescent* bias points. Then, each remapped pulsed-DC IV measurement was re-gridded to an orthogonal v_{gs} - v_{ds} grid. Afterwards, interpolation and linear extrapolation were performed to receive an equally-spaced full-covered v_{gs} - v_{ds} grid.

The critical numerical processes of voltage remapping and re-gridding were carefully performed as delineated in section 6.2.1 for C_{gs} , C_{gd} and C_{ds} .

6.4.3 Extraction of Trapping and Thermal Time Constants

Previous I_{ds} models based on the ideas of Filicori *et al.* used the drain-source and gate-source RC circuits illustrated in Figure 6.20, for the model implementation in CAD [111, 115, 123]. In [115], those RC circuits mainly act as high-pass filters to filter out DC components of v_{gs} and v_{ds} , and to compute in the simulations the I_{ds} -model factors $(v_{gs}-V_{GS})$ and $(v_{ds}-V_{DS})$.

The RC circuits shown in Figure 6.20 are suitable to represent time constants of trapping effects, $R_{GT} \cdot C_{GT}$ and $R_{DT} \cdot C_{DT}$. However, values of those parameters were not related to device characterization by Filicori *et al.* in [115] or in similar I_{ds} models developed later [111, 123]. In [65], a measurement-based extraction of the time constants $R_{GT} \cdot C_{GT}$ and $R_{DT} \cdot C_{DT}$ was presented, using measured drain current transients.

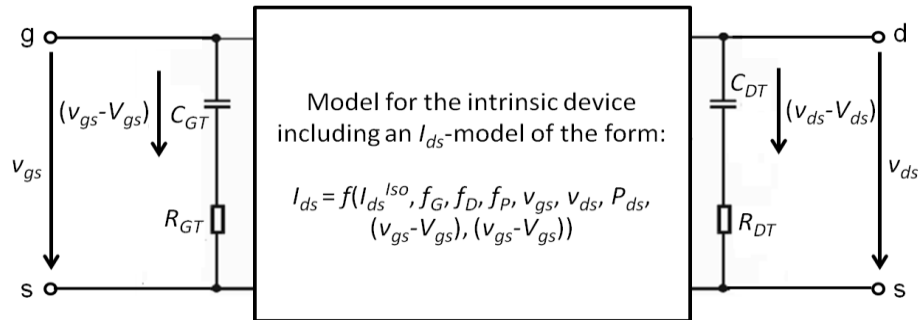


Figure 6.20 Illustration of the RC circuits used in [115] as high-pass filters, for the computation of $(v_{gs}-V_{GS})$ and $(v_{ds}-V_{DS})$ during simulations, and employed in [65] to denote trapping time constants extracted from measured drain current transients.

In this thesis work, a similar extraction of $R_{GT} \cdot C_{GT}$ and $R_{DT} \cdot C_{DT}$ was used as in [65], based on i_{DS} transients measured as response to pulsing the *quiescent* bias, from an initial to *pulsed-to* point. The initial and *pulsed-to* *quiescent* bias points used for the extraction of $R_{GT} \cdot C_{GT}$ and $R_{DT} \cdot C_{DT}$ of the 3.2-mm device are illustrated in Figure 6.21.

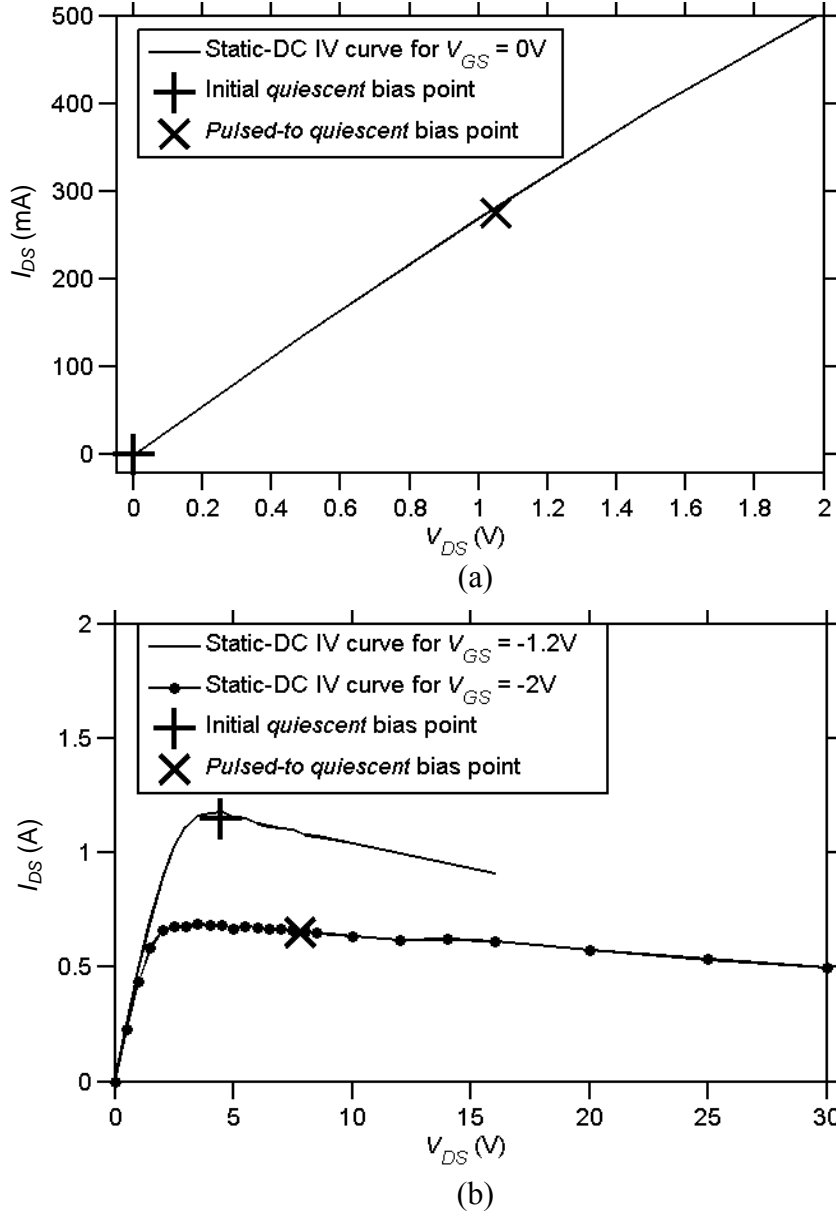


Figure 6.21 Illustration of initial (cross) and *pulsed-to* (X) quiescent bias points chosen for the transient measurements of the 3.2-mm device used to extract (a) $R_{DT} \cdot C_{DT}$ ($V_{GS} = 0V$, $V_{DS} = 0V$, $P_{DS} = 0W$ and $V_{GS} = 0V$, $V_{DS} = 1.05V$, $P_{DS} \approx 0.31W$) and (b) $R_{GT} \cdot C_{GT}$ ($V_{GS} = -1.2V$, $V_{DS} = 4.5V$, $P_{DS} \approx 5W$ and $V_{GS} = -2V$, $V_{DS} = 7.5V$, $P_{DS} \approx 5W$).

Figure 6.22 portrays the measured i_{DS} transient employed to extract the time constant $R_{DT} \cdot C_{DT}$ of the 3.2-mm device. The selected initial and *pulsed-to quiescent* bias points were ($V_{GS} = 0V$, $V_{DS} = 0V$) and ($V_{GS} = 0V$, $V_{DS} = 1.05V$), respectively. The duration of the V_{DS} pulse was 1 ms and the pulse was not repeated. Those *quiescent* bias points were selected to isolate the time constant of V_{DS} -related trapping effects, in accordance with the following considerations, as illustrated in Figure 6.21(a):

- V_{GS} -related trapping effects were not activated because V_{GS} remained constant in $0V$ for the initial and *pulsed-to quiescent* bias points.

- Self-heating was considered negligible because the initial and *pulsed-to quiescent* P_{DS} were 0W and 0.31W (i.e. 0.1 mW/mm), respectively.
- The time constant was related to charge-trapping effects, i.e. electron capture, because decreasing i_{DS} transient was measured for an increased V_{DS} magnitude from the initial to *pulsed-to quiescent* bias point.

The time constant $R_{DT} \cdot C_{DT}$ was extracted from the measured transient shown in Figure 6.22 with an exponential fit, assuming that the i_{DS} component attributed to V_{DS} -related trapping effects is described by:

$$i_{trap}(t) = I(0) \cdot e^{-t/\tau_{trap}}. \quad (6.11)$$

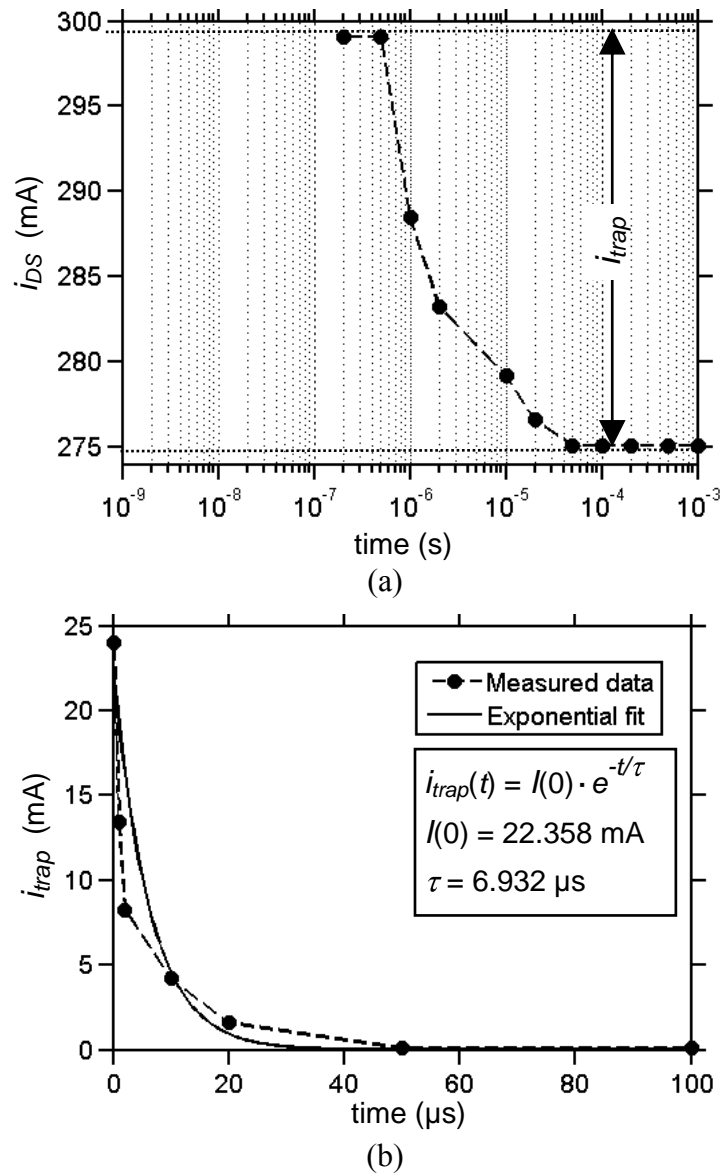


Figure 6.22 (a) Measured i_{DS} transient used to extract $R_{DT} \cdot C_{DT}$ of the 3.2-mm device, highlighting the i_{trap} component related to the dominant trapping effect. (b) Separated i_{trap} (dashed dot-marked lines) and the employed exponential fit (solid line). The initial and *pulsed-to quiescent* bias points were illustrated in Figure 6.21(a).

Figure 6.23 depicts the measured i_{DS} transient used to extract $R_{GT} \cdot C_{GT}$ of the 3.2-mm device. The selected initial and *pulsed-to quiescent* bias points were $V_{GS} = -1.2\text{V}$ with $V_{DS} = 4.5\text{V}$ and $V_{GS} = -2\text{V}$ with $V_{DS} = 7.5\text{V}$, respectively. The duration of the V_{GS} and V_{DS} pulses was 1 ms and the pulses were not repeated. Those *quiescent* bias points were selected to isolate the time constant of V_{GS} -related trapping effects, in accordance with the following considerations, as illustrated in Figure 6.21(b):

- V_{DS} -related trapping effects were not considered dominant, because the initial and *pulsed-to* V_{DS} were in the saturation region ($V_{DS} > V_k$), where current depends mostly on V_{GS} . Moreover, those trapping effects were considered weakly activated, since the 3V-change from initial to *pulsed-to* V_{DS} was small compared to the 54V-change used to extract the related trapping-effects parameter f_D . Thus, a 3V-change is small compared to the V_{DS} change of the maximum V_{DS} -related trapping effects observed.
- Self-heating effects were not activated because P_{DS} values remained constant around 5W for the initial and *pulsed-to quiescent* bias points.
- The time constant was related to charge-trapping effects, i.e. electron capture, because decreasing i_{DS} transient was measured for an increased V_{GS} magnitude from the initial to *pulsed-to quiescent* bias point.

The time constant $R_{GT} \cdot C_{GT}$ was extracted from the measured transient shown in Figure 6.23 with an exponential fit, assuming that the i_{DS} component attributed to V_{GS} -related trapping effects is described by (6.11).

Trapping time constants of the 2-mm device were extracted similarly as for the 3.2-mm device. Table 6.3 summarizes all $R_{GT} \cdot C_{GT}$ and $R_{DT} \cdot C_{DT}$ values extracted and the corresponding initial and *pulsed-to quiescent* bias points that were used.

Table 6.3 Extracted values of the trapping time constants of the studied large-size devices and the selected *quiescent* bias conditions for the transient measurements used.

3.2-mm device							
Time constant	Initial <i>quiescent</i> bias point			<i>Pulsed-to quiescent</i> bias point			Extracted value (μs)
	V_{GS} (V)	V_{DS} (V)	P_{DS} (W/mm)	V_{GS} (V)	V_{DS} (V)	P_{DS} (W/mm)	
$R_{DT} \cdot C_{DT}$	0	0	0	0	1.05	0.1	7
$R_{GT} \cdot C_{GT}$	-1.2	4.5	1.6	-2	7.5	1.6	1.5
2-mm device							
Time constant	Initial <i>quiescent</i> bias point			<i>Pulsed-to quiescent</i> bias point			Extracted value (μs)
	V_{GS} (V)	V_{DS} (V)	P_{DS} (W/mm)	V_{GS} (V)	V_{DS} (V)	P_{DS} (W/mm)	
$R_{DT} \cdot C_{DT}$	0	0	0	0	0.48	0.07	9.4
$R_{GT} \cdot C_{GT}$	-1.1	2	0.13	-1.5	5	0.13	13

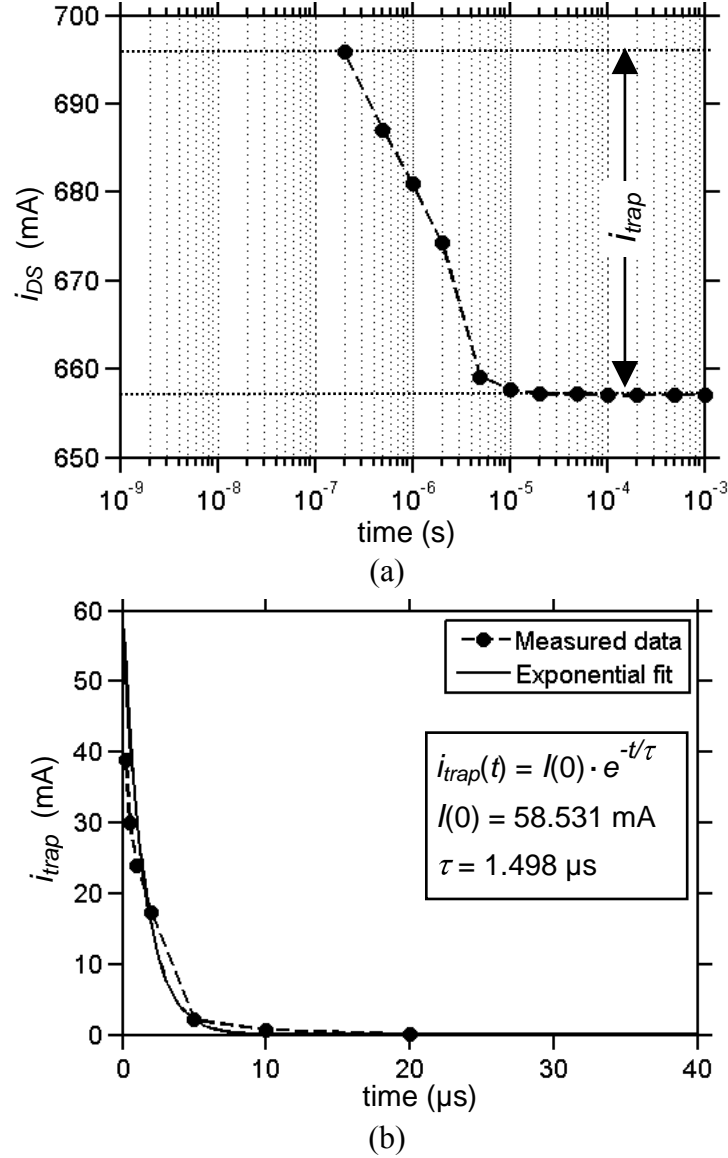
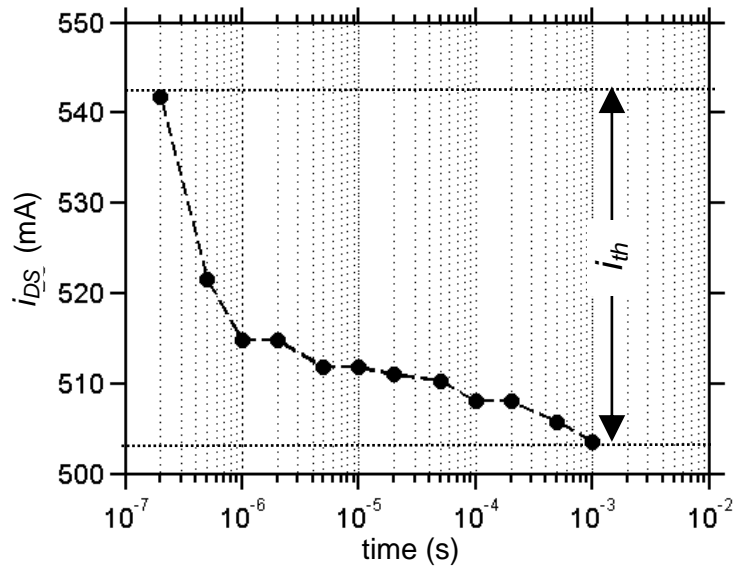


Figure 6.23 (a) Measured i_{DS} transient used to extract $R_{GT} \cdot C_{GT}$ of the 3.2-mm device, highlighting the i_{trap} component related to the dominant trapping effect. (b) Separated i_{trap} (dashed dot-marked lines) and the employed exponential fit (solid line). The initial and *pulsed-to quiescent* bias points were illustrated in Figure 6.21(b).

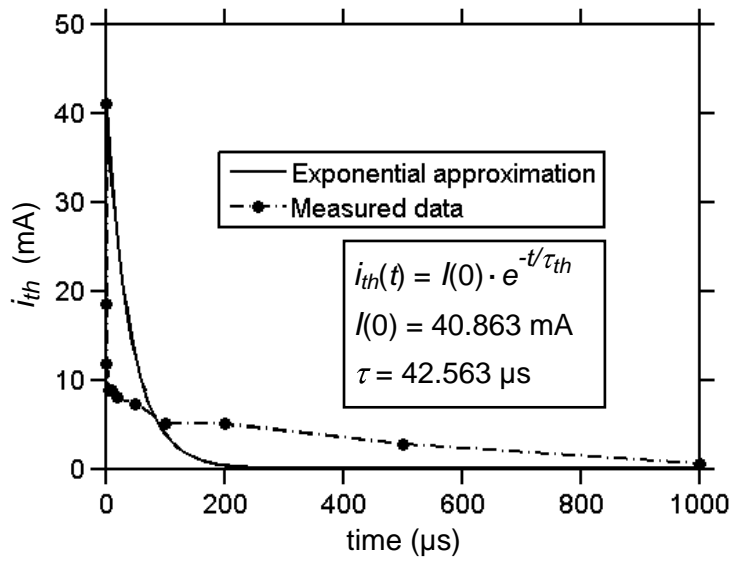
τ_{th} and R_{th} values for the model of the 2-mm device were not calculated with the technique of [103, 104] (as done for the 3.2-mm device model), due to lacking of data needed for heat-transfer simulations. Thus, R_{th} was omitted in model and τ_{th} extracted from i_{DS} transient measurements.

Figure 6.24 portrays the measured i_{DS} transient employed to extract τ_{th} . The selected initial and *pulsed-to quiescent* bias points were $V_{GS} = 0V$ with $V_{DS} = 0V$ and $V_{GS} = 0V$ with $V_{DS} = 1.6V$, respectively. The duration of the V_{DS} pulse was 1 ms and the pulse was not repeated. Those *quiescent* bias points were selected to isolate self-heating effects, in accordance with the following considerations:

- V_{GS} -related trapping effects were not activated because V_{GS} remained constant in 0V for the initial and *pulsed-to quiescent* bias points.
- V_{DS} -related trapping effects were not considered dominant, due to the low V_{DS} change selected, 1.5V, and because the 2-mm device exhibits comparatively low V_{DS} -related trapping effects, as concluded during pulsed-DC IV characterization (subsection 3.2.3.3) and verified during the parameter extraction of f_D (section 6.4.1).
- Self-heating was considered the dominant effect because the *quiescent* P_{DS} was ramped from 0W to around 1W, and 1W represents 20% of the DC power limit of this device.



(a)



(b)

Figure 6.24 (a) Measured i_{DS} transient used to extract τ_{th} of the 2-mm Nitonex[®] device, highlighting the i_{th} component related to the self-heating effect. (b) Separated i_{th} (dashed dot-marked lines) and the exponential fit applied (solid line).

In Figure 6.24, the measured transient exhibited a fast decreasing rate before 1 μs . Then, the rate of decrease was less pronounced for the points measured afterwards. The existence of fast and slow thermal processes in the current component attributed to self-heating effects, i_{th} , was identified before in the work in [103, 104].

Moreover, different material layers of the device structure, suggest that the thermal time constant and resistance are more accurately represented as distributed effects. It has been suggested, that the implementing multiple τ_{th} and R_{th} values to represent thermal processes is more according to the multi-layer device structure [124].

By the time this thesis work was carried out, electro-thermal modeling with multiple thermal time constants integrated with the adopted I_{DS} -model and with a related extraction from transient measurements was still under development. Results of implementing the electro-thermal modeling with multiple thermal time constants suggested in [124] had not been published by his author by the time this thesis was written.

Because of these reasons, electro-thermal modeling with multiple τ_{th} and R_{th} values was not implemented or extracted in this thesis work and it is proposed in the outlook for future research.

In this thesis work, τ_{th} was extracted from the measured transient shown in Figure 6.24 with an exponential fit using a single thermal time constant, assuming that the i_{DS} component attributed to self-heating effects is described by the following equation:

$$i_{th}(t) = I(0) \cdot e^{-t/\tau_{th}}. \quad (6.12)$$

The calculated exponential fit gave the best overall agreement with measurements for the whole time span, and a τ_{th} value of 42.5 μs was extracted.

As discussed at the end of section 6.3.2, parameter values of the electro-thermal sub-circuit for the 3.2-mm device were extracted by Dahmani *et al.* from the heat-transfer simulations reported in [103, 104]. R_{th} was extracted equal to 8.35 $^{\circ}\text{C}/\text{W}$ and τ_{th} equal to 85 μs , as listed in Table 6.1.

Chapter 7

Large-Signal Modeling Verification

7.1 Large-Signal Model Implementation

The complete large signal model was implemented in the ADS[®] software of Agilent[®] to carry out simulations and obtain model predictions to compare them with the device measured behavior. The complete circuitual representation of the large-signal model is shown in Figure 7.1.

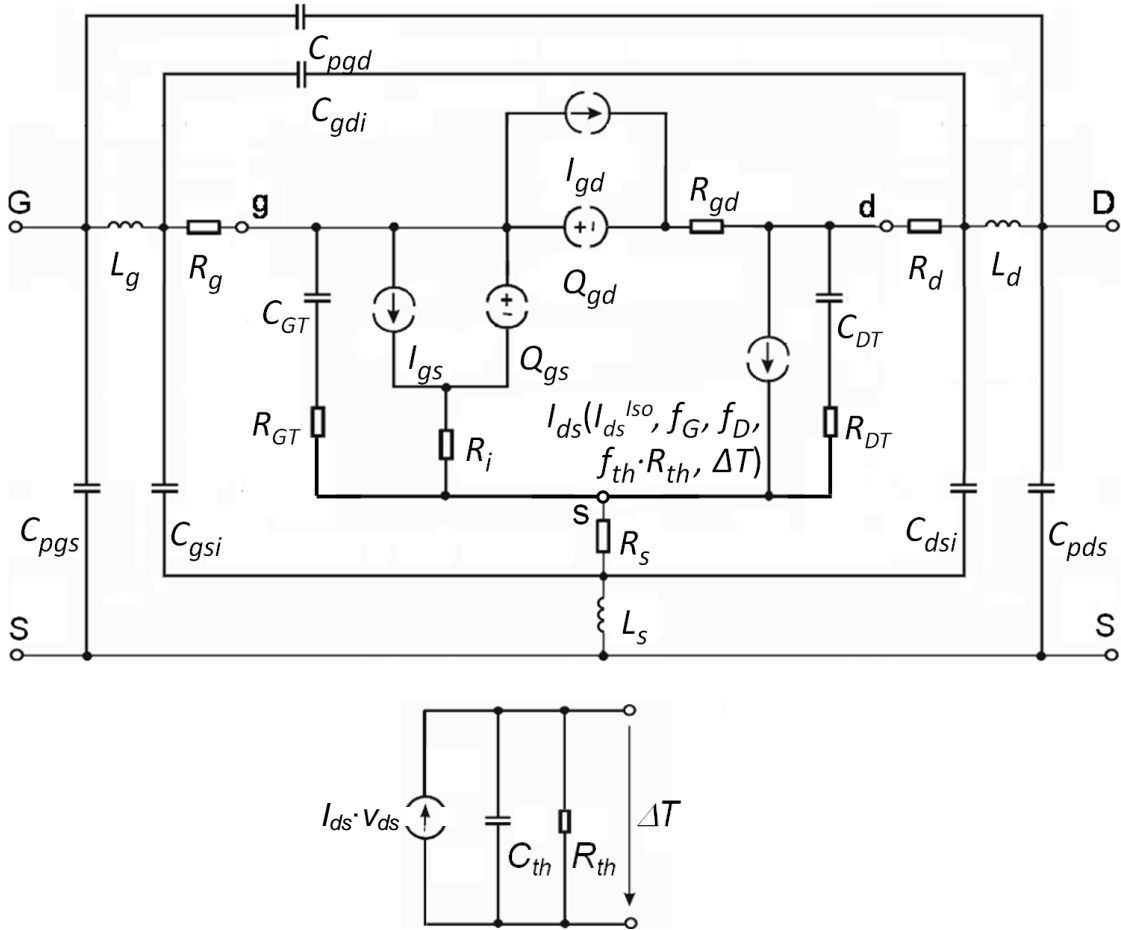


Figure 7.1 Complete circuit representation of the large-signal model proposed in this thesis work.

The extrinsic elements of the circuit C_{pgs} , C_{pds} , C_{pgd} , C_{gdi} , C_{gsi} , C_{dsi} , R_g , R_s , R_d , L_g , L_s and L_d were implemented in the ADS[®] schematic as lumped elements. The remaining elements form the intrinsic part of the circuit,

which was implemented with a SDD (symbolically-defined device) block, as shown in Figure 7.2.

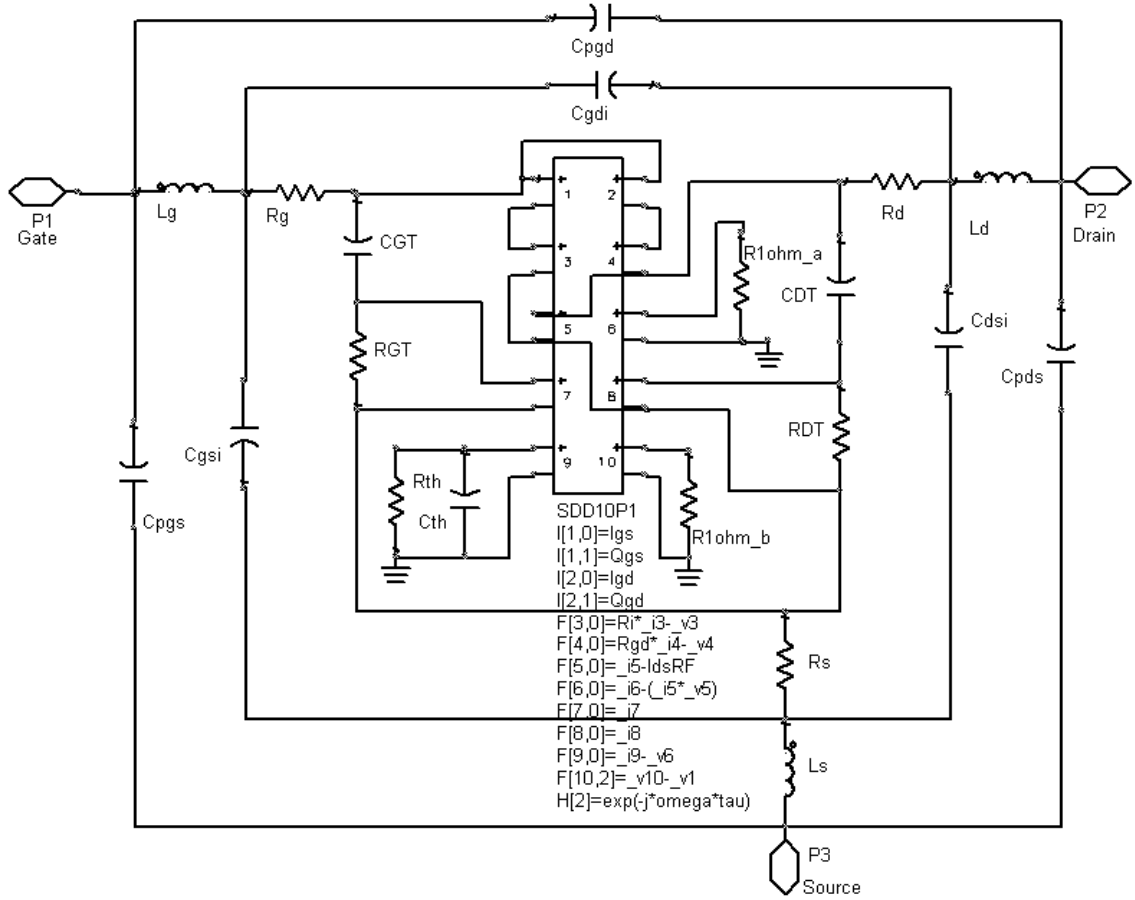


Figure 7.2 Implementation of the intrinsic part of the large-signal model with a 12-port SDD in the ADS® schematic.

The ports 1 and 2 corresponded to the shunt circuits of I_{gs} with Q_{gs} and of I_{gd} with Q_{gd} , the current sources were directly entered as the current of the ports. The current component due to the charge sources was indicated entering the charge source in the corresponding port and applying the 1st weighting factor: The “1” in the second space inside the brackets in the definition $F[n,1]$ by default is equivalent to the time derivative in the simulator. Simultaneously, v_{gs} was given by the voltage sensed by the simulator in port 1, $_v1$. The ports 3 and 4 were used for the parameters R_i , R_{gd} . The I_{ds} current was implemented in a separate expression according the I_{ds} -model equation adopted in this thesis work. Then, the instantaneous I_{ds} value calculated by the simulator was entered as the current of this port 5 and v_{ds} was given by the voltage sensed in port 5, $_v5$. The remaining 5 ports performed auxiliary functions:

- The product $(_v5_i5)$ was calculated in port 6 and entered as current, wherein an 1- Ω resistor gave the dissipated power p_{ds} as $_v6$.

- The function of port 7 and 8 was sensing the time-varying components ($v_{gs}-V_{GS}$) and ($v_{ds}-V_{DS}$) that are factors in the I_{ds} model, and which were available as $_v7$ and $_v8$.
- The power p_{ds} was entered as current in port 9, wherein the electro-thermal sub-circuit was implemented, and then, ΔT was obtained as $_v9$.
- The 2nd weighting function was defined as $H[2]=e^{-j\omega\tau}$, i.e. as the time delay of the transconductance. Then, the gate voltage denoted by $_v1$ was entered as voltage of port 10, applying the user-defined 2nd weighting function with the nomenclature $F[10,2]$. As a result, the delayed gate voltage was obtained as $_v10$.

The extracted values of the bias-dependent intrinsic parameters R_{gd} , R_i , Q_{gs} , I_{gs} , Q_{gd} , I_{gd} , τ , and the bias-dependent I_{ds} -model parameters I_{ds}^{Iso} , f_D , f_G , f_{th} were stored in text files. Then, these parameters were implemented in the ADS[®] schematic as look-up tables that point to the text files. This was done with DAC (data-access component) blocks. For every instantaneous value of the controlling voltages, the simulator reads the value of the required parameter from the look-up-table files.

The v_{ds} and v_{gs} values, given by $_v5$ and $_v1$, were used as controllers for the reading of the file that contained the parameters R_{gd} , R_i , Q_{gs} , I_{gs} , Q_{gd} , I_{gd} , τ . The values of v_{ds} and of the delayed v_{gs} , given by $_v5$ and $_v10$, were the controllers for the reading of the file that contained the parameters I_{ds}^{Iso} , f_D , f_G , f_{th} .

7.2 Tests of Large-Signal Model Verification

With the large-signal model implemented as an ADS[®] schematic, the model was verified through several tests. In the verifications tests, large-signal simulations were performed and compared with measurements carried out on the large-size studied devices.

Model verification results are reported in the next sections on different bias points and for different types of stimuli, i.e.: (i) S-parameters, (ii) pulsed-DC IV characteristics, (iii) power sweeps with a single input tone, and (iv) power sweeps with two input tones.

7.2.1 Verification Tests with S-Parameters

The developed large-signal models were implemented in ADS[®] and the S-parameters were simulated, then the received simulations were compared with measured S-parameters. The results of such comparison are shown in Figure 7.3 and Figure 7.4 for the studied large-size devices.

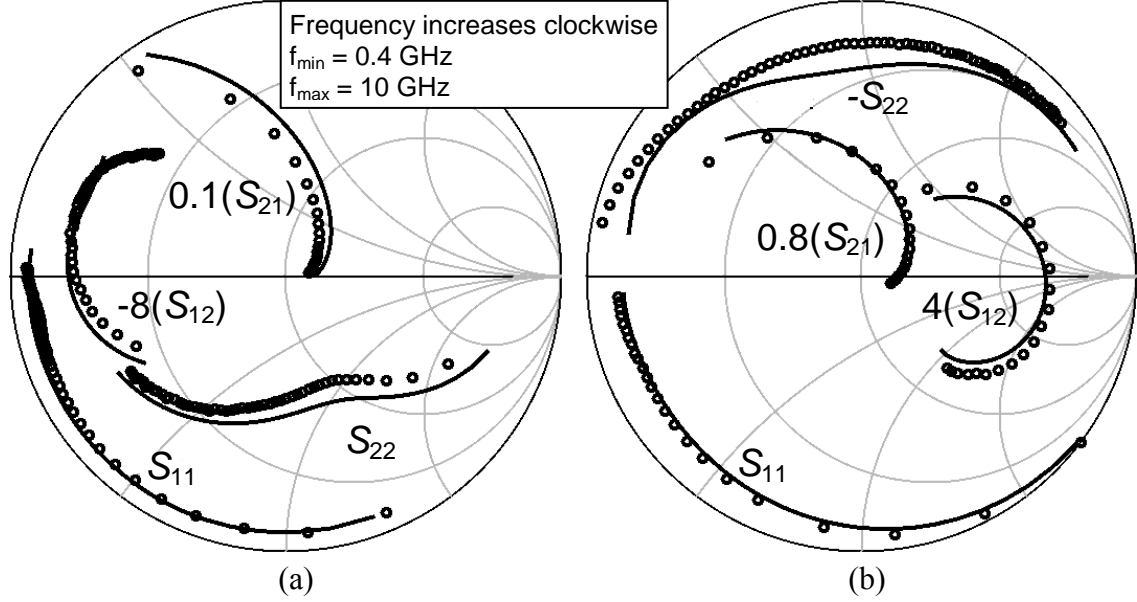


Figure 7.3 S-parameter measurements of the 3.2-mm device (circles) and simulations obtained with the large-signal model (lines) for bias points (a) in the saturation region, $V_{GS} = -3.2V$, $V_{DS} = 30V$, and (b) near the pinch-off region, $V_{GS} = -3.6V$, $V_{DS} = 55V$.

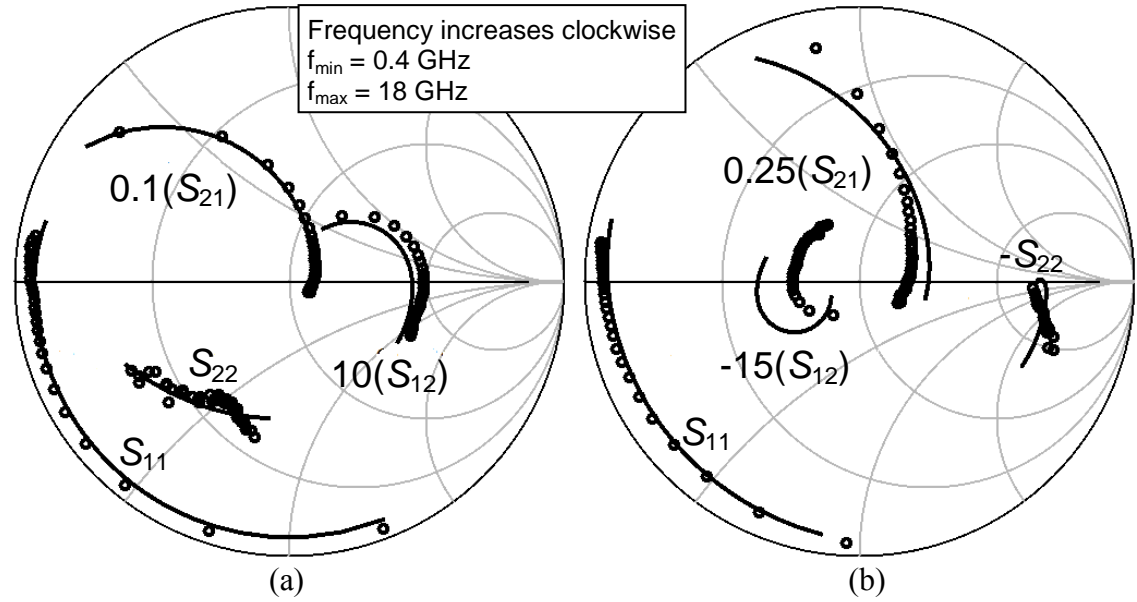


Figure 7.4 S-parameter measurements of the 2-mm device (circles) and simulations obtained with the large-signal model (lines) for bias points (a) in the ohmic region, $V_{GS} = -1.1V$, $V_{DS} = 5V$, and (b) in the high- V_{GS} low- V_{DS} region, $V_{GS} = +0.2V$, $V_{DS} = 4V$.

On one hand, the parameters R_{gd} , R_i , Q_{gs} , I_{gs} , Q_{gd} and I_{gd} have strong influence on the simulations of the device input impedance of the large-signal model. Those parameters were extracted on the basis of S-parameter measurements.

On the other hand, the I_{ds} -model parameters have strong influence on the simulations of the device transconductance and output impedance of the large-signal model. Those parameters were extracted on the basis of pulsed-DC IV measurements and thus are less connected to S-parameter measurements.

In consequence, simulations of the large-signal models were expected to produce closer model agreements with measurements for S_{11} , related to the simulated input impedance, than for S_{22} and S_{21} , related to the simulated output impedance and transconductance. These expectations corresponded to the results shown in Figure 7.3 and Figure 7.4, with comparatively better agreements of simulations with measurements for S_{11} than for S_{22} and S_{21} .

The generally good agreements of simulations and measured S-parameters verify the consistency between the large-signal and small-signal models adopted in this work. Excellent agreements were observed for bias points in the saturation and pinch-off regions, exemplified by the comparisons shown in Figure 7.3(a) and Figure 7.3(b).

For bias points in the ohmic region that are exemplified by the comparisons shown in Figure 7.4(a), the observed agreement declines, but only for S_{22} at the lowest frequencies. Nonetheless, the related 2-mm GaN device has a Si substrate and the difficulty to model low-frequency S_{22} of such devices was expected (as discussed at the end of section 5.2.2), so that in general the agreements of simulations and measurements presented in Figure 7.4(a) were very good.

For bias points in the high- V_{GS} low- V_{DS} region that are exemplified by the comparisons shown in Figure 7.4(b), the observed agreements decrease, mainly for S_{22} and S_{21} (note the magnification factor of 15 of S_{12} , i.e. it has very small values, so the observed agreement is adequate). But these decreased accuracy to simulate S-parameters for bias points in the high- V_{GS} low- V_{DS} region was expected (as discussed at the end of section 5.2.2), so the comparisons shown in Figure 7.4 (b) are considered adequate.

Influence of the location of the bias points on the large-signal model accuracy to simulate S-parameters matches the observed bias-dependency

of the small-signal model accuracy, which was reported in section 5.2.2. In such section, Figure 5.9 and Figure 5.10 showed excellent model accuracy for bias points outside the high- V_{GS} low- V_{DS} region.

The specific reduction of the small-signal model accuracy related to the high- V_{GS} low- V_{DS} region is considered to be transferred to the large-signal model via the extrinsic model parameters and R_{gd} , R_i , Q_{gs} , I_{gs} , Q_{gd} and I_{gd} , which directly connect the small and large-signal modeling stages.

7.2.2 Pulsed-DC IV Verification Tests

Comparisons of pulsed-DC IV measurements and simulations are shown in Figure 7.5 and Figure 7.6 for the 3.2-mm and 2-mm devices, respectively.

Results are presented only for *quiescent* bias points that were not employed to develop the I_{ds} -model. Similar results for *quiescent* bias points used in the I_{ds} -model parameter extraction, although comparatively more accurate, were considered less meaningful, and therefore, are not shown here.

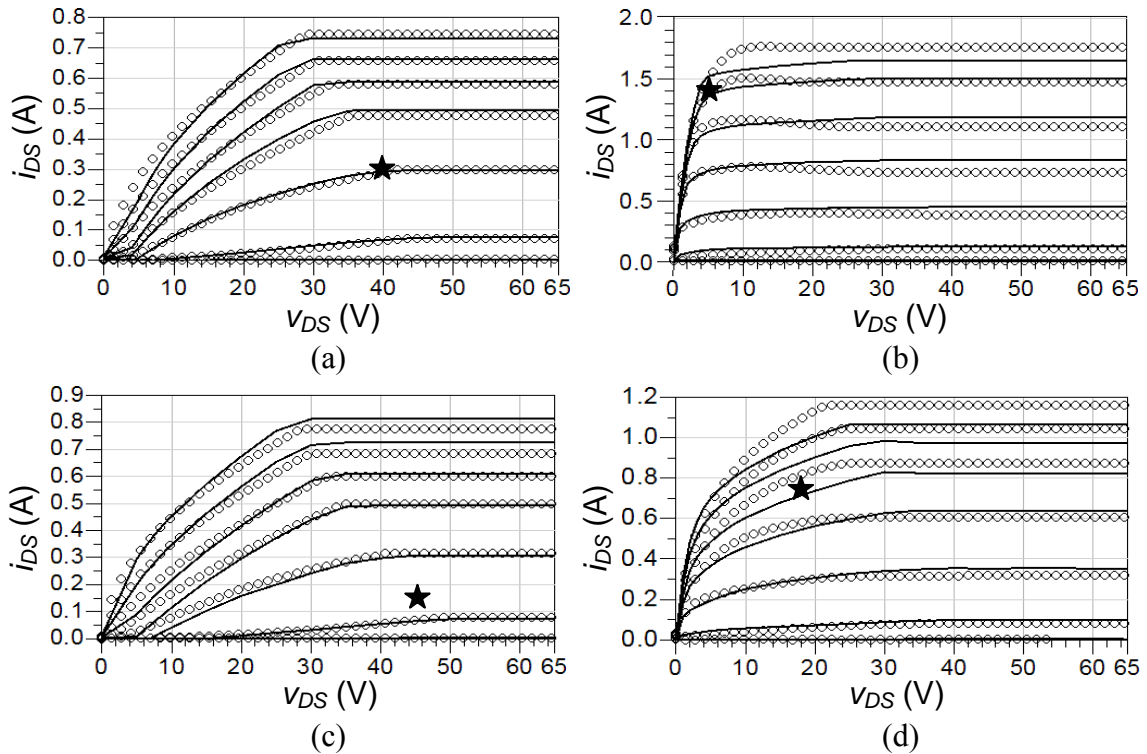


Figure 7.5 Pulsed-DC IV measurements (circles) and simulations (lines) of the 3.2-mm device on the *quiescent* bias points (stars): (a) $V_{GS} = -2.7V$, $V_{DS} = 40V$, $I_{DS} = 0.3A$, (b) $V_{GS} = -1V$, $V_{DS} = 5V$, $I_{DS} = 1.4A$, (c) $V_{GS} = -3.1V$, $V_{DS} = 45V$, $I_{DS} = 0.15A$ and (d) $V_{GS} = -1.7V$, $V_{DS} = 18V$, $I_{DS} = 0.76A$. v_{GS} curves from $-3.6V$ to $0V$ in steps of $0.6V$.

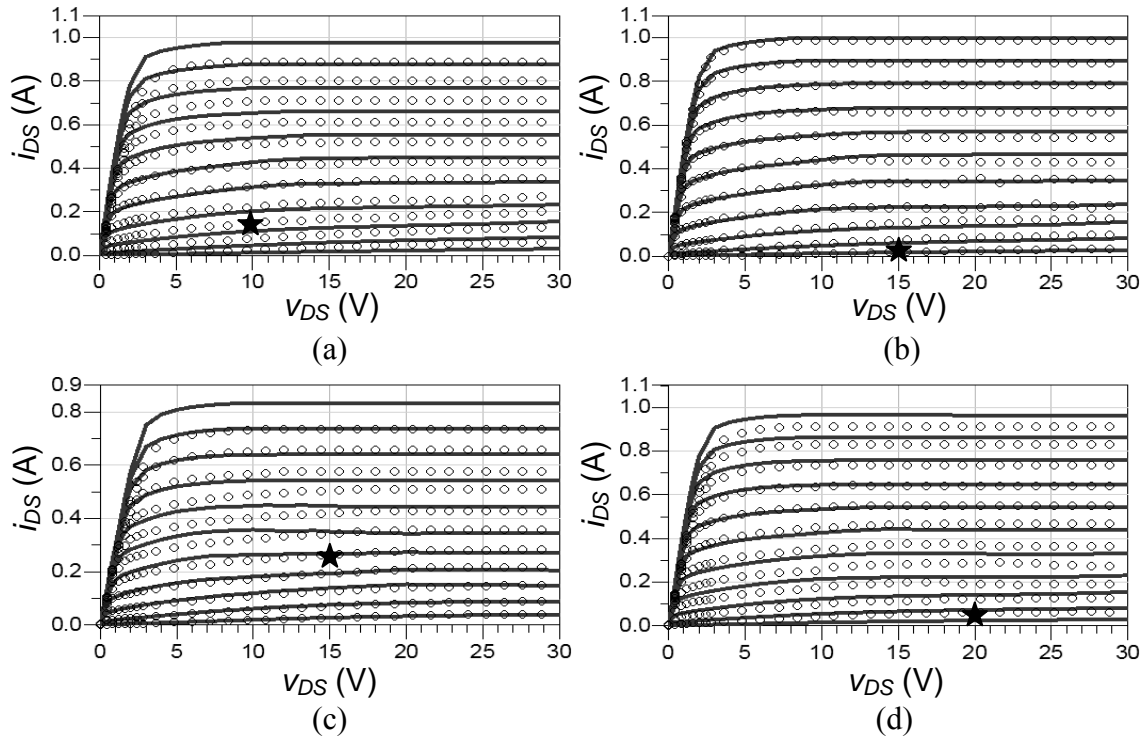


Figure 7.6 Pulsed-DC IV measurements (circles) and simulations (lines) of the 2-mm device on the *quiescent* bias points (a) $V_{GS} = -1.2\text{V}$, $V_{DS} = 10\text{V}$, $I_{DS} = 0.12\text{A}$, (b) $V_{GS} = -1.5\text{V}$, $V_{DS} = 15\text{V}$, $I_{DS} = 0.036\text{A}$, (c) $V_{GS} = -0.9\text{V}$, $V_{DS} = 15\text{V}$, $I_{DS} = 0.23\text{A}$ and (d) $V_{GS} = -1.5\text{V}$, $V_{DS} = 20\text{V}$, $I_{DS} = 0.043\text{A}$. v_{GS} curves from -2V to 0V in steps of 0.2V .

The pulse repetition rate and pulse width employed in the simulations correspond to the same values used in the measurements, i.e. $0.1\text{ }\mu\text{s}$ and 1 mS , respectively, giving 0.01% duty cycle.

For the 3.2-mm device model, the excellent agreements of simulations with measurements are exemplified by the results shown in Figure 7.5(a) and Figure 7.5(c).

These agreements indicate the ability of this large-signal model to accurately characterize low-frequency dispersive phenomena for *quiescent* bias points in the pinch-off and saturation regions, especially for operating points that are used in power amplifier design of classes A, AB, B or C ($I_{DS} < 75\%$ of I_{DSS}).

For the 2-mm device model, the very good agreements of simulations with measurements are illustrated by the results shown in Figure 7.6(b) and Figure 7.6(d).

These agreements highlight the accuracy of this large-signal model to represent low-frequency dispersive phenomena for *quiescent* in the pinch-

off and saturation regions, in particular at operating points that are used for power amplifier design in class AB, B and C (with $I_{DS} < 33\%$ of I_{DSS}).

For bias points with larger *quiescent* currents than those mentioned in the previous paragraphs, specifically corresponding to Figure 7.5(b), Figure 7.5(d), Figure 7.6(a) and Figure 7.6(c), the agreements of simulations with measurements decrease as the *pulsed-to* v_{GS} approaches 0V, i.e. the highest i_{DS} values. This is explained by the residual effect of the stabilization resistance that increases proportionally to the drain current flowing in the device.

In the high- V_{DS} high- V_{GS} region measurements are not available for the development of the model due to the high DC power implied. For that region all values of bias-dependent model parameters, and of simulation results, are unrelated to measurements or real device behaviour, and are therefore comparatively less meaningful.

Typically, the extrapolation finds those values merely extending (or repeating) the value of the nearest point in the direction of lower V_{DS} that complies with the DC power limitation (the nearest point actually related to measured data). Therefore, in essence, the inaccuracies on the high- V_{DS} high- V_{GS} region are reliably overlooked, and are only indication of inaccuracies of the low- V_{DS} high- V_{GS} region.

The low- V_{DS} region is the most difficult to model accurately. This is mainly due to the remapping and re-gridding of the bias voltages required in the model parameter extraction, which introduces inaccuracies in the simulation results.

7.2.3 Verification Tests with Single-Tone and Two-Tone Stimuli

Verification tests of single and two-tone stimuli offer a better insight of the large-signal effects accounted by the model.

The large-signal models for the studied large-size devices were developed considering their application to design power amplifiers for base station transmitters of UMTS, at operation bias points with V_{DS} between 45V and 50V and with I_{DS} up to 300 mA (≈ 100 mA/mm) for the 3.2-mm device. For the 2-mm device an application for high-efficiency power amplifiers was considered, with operations bias points that have V_{DS}

between 10V and 15V with I_{DS} up to 300 mA. In consequence, the verification tests with single-tone and two-tone stimuli were carried out with bias points close to those ranges.

The frequency of the fundamental tone for the single-tone test was selected in 2.15 GHz. This value is in the center of the frequency band assigned by ITU for the FDD variation of the UMTS communication channel in the base station, as explained in the first paragraphs of the introduction. For the tests with two-tone stimuli, the middle point between tones is also 2.15 GHz. The tone-spacing was selected on 200 kHz, the channel raster of FDD UMTS.

Figure 7.7 and Figure 7.8 report comparisons of large-signal simulations with single-tone measurements performed in a 50- Ω environment on the studied large-size devices. In the simulations, the power level of a sinusoidal source was swept and for each swept value model predictions were obtained of the output power at the frequencies f_0 , $2f_0$ and $3f_0$ (fundamental, 2nd- and 3rd-harmonics), of the power gain and of the power-added efficiency (calculated with model predictions of I_{ds} current at each sweep step).

In order to assure that the simulated condition agreed with the real situation presented by the measurement setup, the term P_{out} in Figure 7.7 and Figure 7.8 was calculated as equal to the power absorbed in the 50- Ω load, and the term P_{in} was calculated as equal to the difference between incident and reflected powers at the transistor input.

For output power of the fundamental and the first two harmonics the large-signal model shows predictions with relative accuracy around 10% in the selected bias range of focus (regarding the considered applications of the models).

For the model of the 2-mm device, the most accurate simulations of fundamental output power are reported in Figure 7.7(a) and (c) for bias points of class-A and AB power amplifier design (I_{DS} values around 50% and 33% of I_{DSS} , respectively). In such bias points, P_{out} was correctly predicted up to 37 dBm, approximately equivalent to 4.5W and 2.5 W/mm. The most accurate simulations of 2nd- and 3rd-harmonic powers correspond to Figure 7.7(b) on a bias point typically employed for class-AB power amplifier design (less than 10% of I_{DSS}).

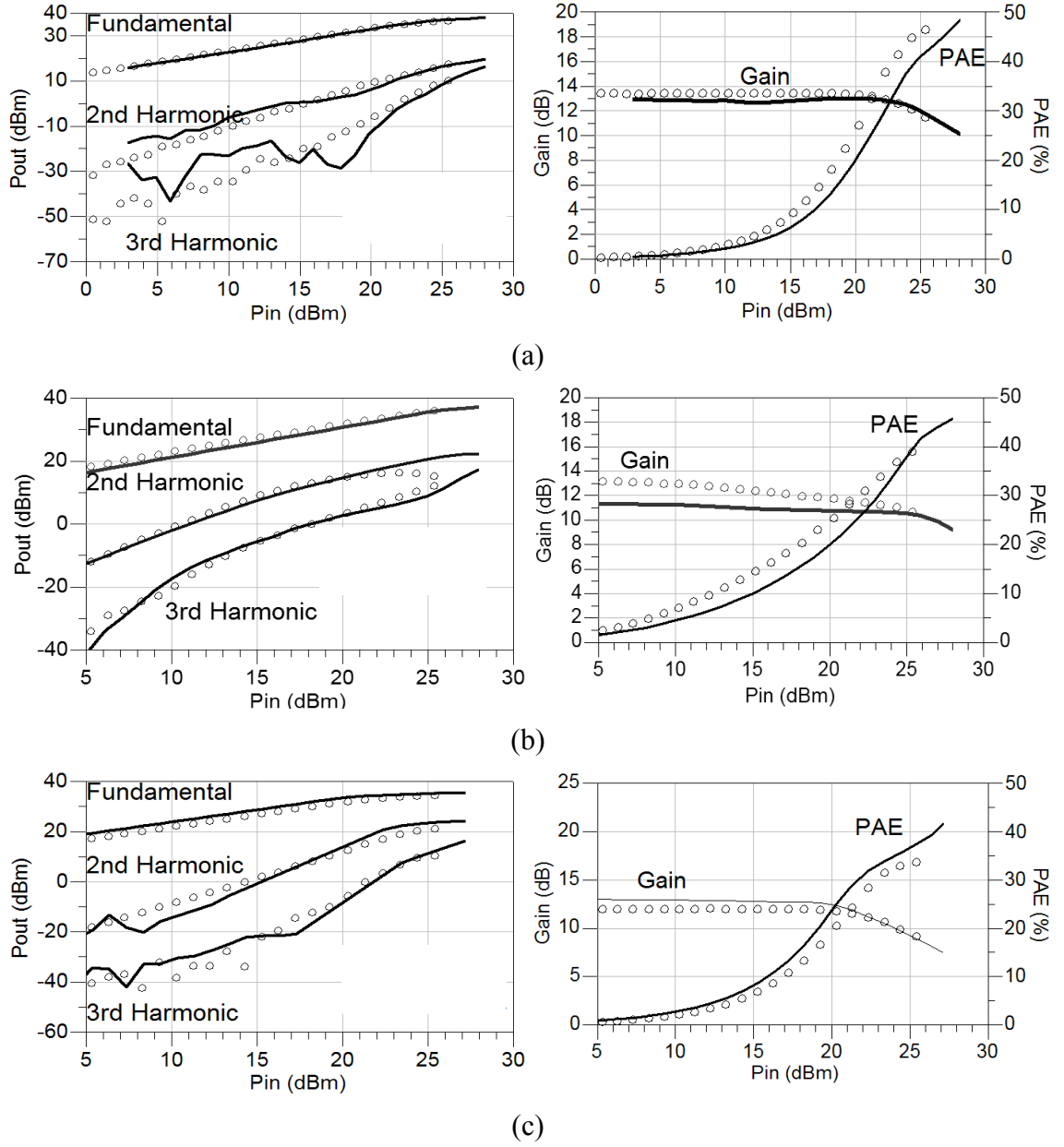


Figure 7.7 Comparison of single-tone measurements (circles) with simulations of the large-signal model (lines) for the 2-mm device on the bias points (a) $V_{GS} = -1.4V$, $V_{DS} = 15V$, $I_{DS} = 245$ mA, (b) $V_{GS} = -2.6V$, $V_{DS} = 15V$, $I_{DS} = 65$ mA and (c) $V_{GS} = -1.32V$, $V_{DS} = 10V$, $I_{DS} = 300$ mA.

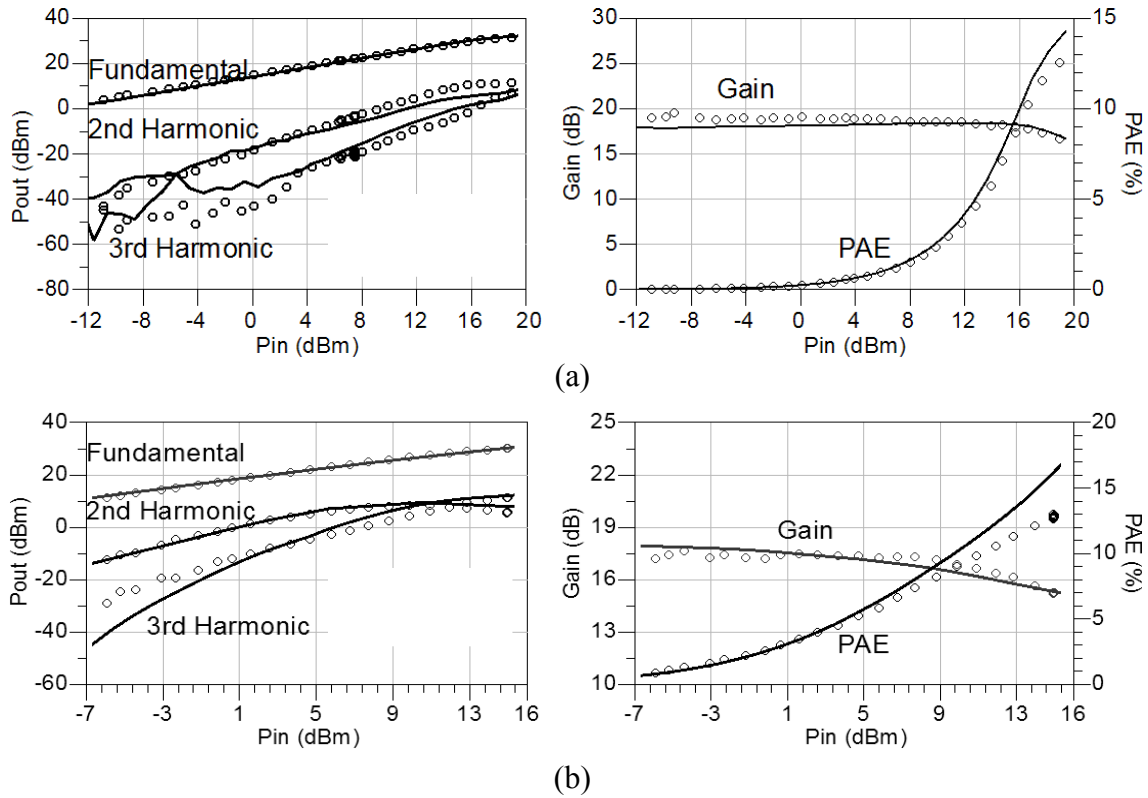


Figure 7.8 Comparison of single-tone measurements (circles) with simulations of the large-signal model (lines) for the 3.2-mm device on the bias points (a) $V_{GS} = -2.7\text{V}$, $V_{DS} = 45\text{V}$, $I_{DS} = 300\text{ mA}$ and (b) $V_{GS} = -3.475\text{V}$, $V_{DS} = 40\text{V}$, $I_{DS} = 60\text{ mA}$.

For the model of the 3.2-mm device, accurate simulations of fundamental output power are reported in Figure 7.8(a) and (b), for a bias points of class-AB and C power amplifier design (I_{DS} values nearly 20% and less than 5% of I_{DSS} , respectively). In such bias point, P_{out} was correctly predicted up to 36.5 dBm, approximately equivalent to 4W and 1.25 W/mm.

Accuracy of large-signal predictions decreased for 3rd-harmonic of the verification tests of Figure 7.7(a) and Figure 7.8(a) at low output powers, P_{out} lower than -10 and -30 dBm, respectively. These inaccuracies are a drawback of the look-up table implementation of the model parameters, as has been documented in [111]. When the power levels are small enough, the voltages controlling the reading of look-up-table files are lower than the point-spacing of the grid of the stored parameter values, and then, the simulator must interpolate. Combination of interpolating highly-nonlinear data and the high-order derivatives required to calculate output power of the high-order harmonics produces model predictions that show a high rippling behavior. These problems are diminished if the parameters are interpolated in a denser grid before being stored, but this is direct trade-off

with the simulation time and computing effort, since the managed files are larger (a twice-denser grid means 4-times larger files) and the look-up-table process turns slower.

The problematic high- V_{DS} high- V_{GS} region for values of the bias-dependent model parameters produces inaccuracies in the single-tone simulations mainly in the drain current predictions of the model, diminishing the agreement with measured results of the power-added efficiency for the highest output power levels.

However, the general agreement of the simulation results with the measures data is very good at the medium and high-power level. For example, as mentioned before, output powers of the fundamental tone were well predicted up to 4W for the 3.2-mm device, and up to 5W for the 2-mm device.

Regarding verification tests with two-tone stimuli, results of large-signal simulations were compared with measurements, and the results are presented in Figure 7.9 and Figure 7.10.

The terms P_{out} and P_{in} in those figures represent the same calculated powers as in single-tone simulations and they referred to the power of the lowest input tone.

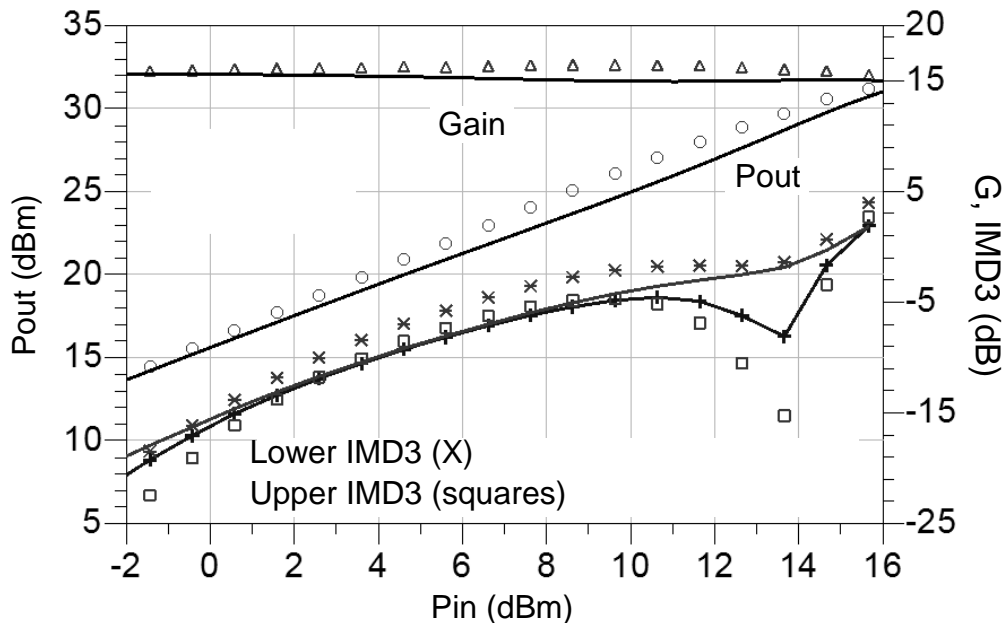


Figure 7.9 Comparison of two-tone measurements (markers) with simulations of the large-signal model (lines) for the 2-mm device on the bias point $V_{GS} = -1.5V$, $V_{DS} = 15V$, $I_{DS} = 40$ mA. The tone-spacing is 200 KHz.

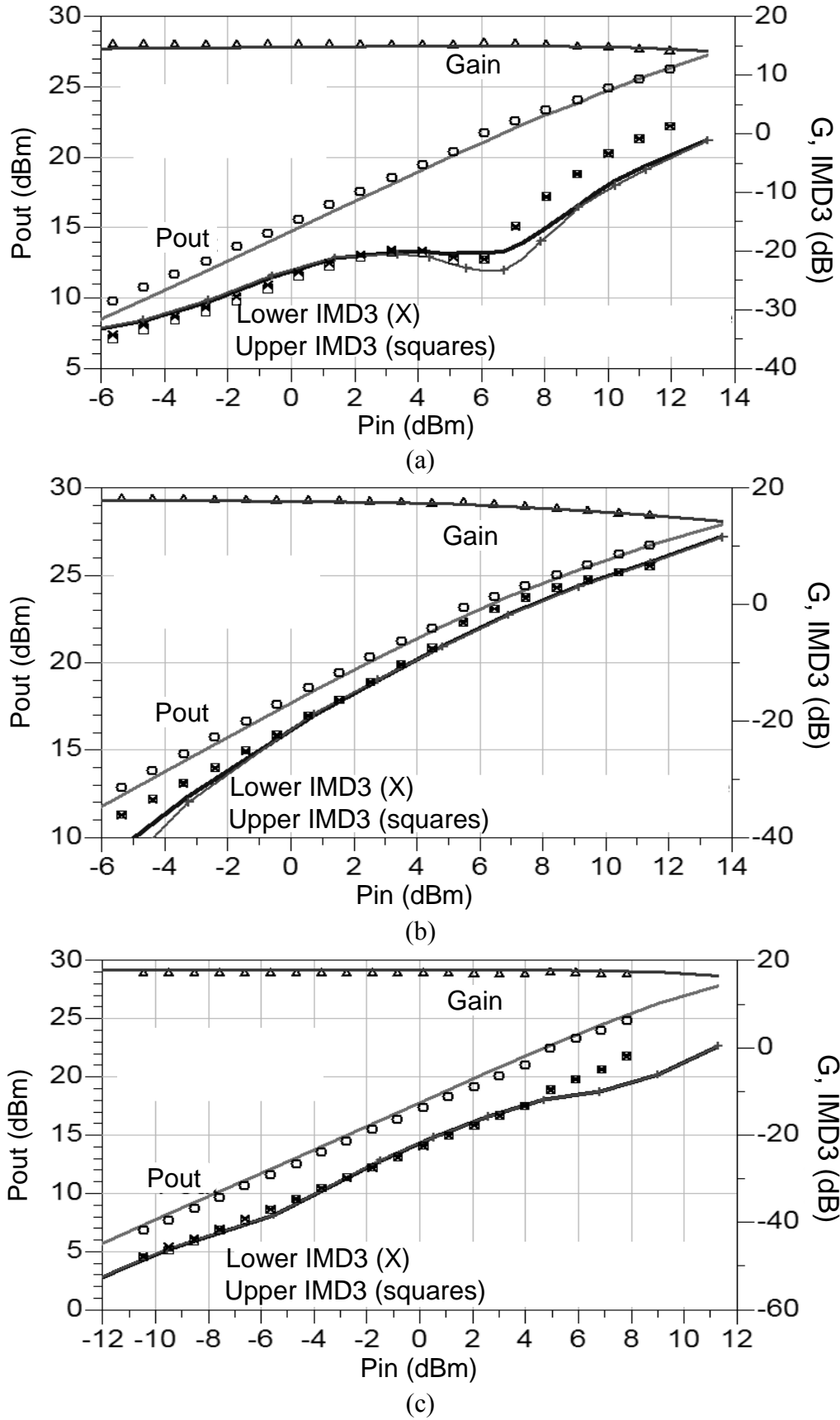


Figure 7.10 Comparison of two-tone measurements (markers) with simulations of the large-signal model (lines) for the 3.2-mm device on the bias points (a) $V_{GS} = -3.475V$, $V_{DS} = 40V$, $I_{DS} = 25$ mA, (b) $V_{GS} = -3.1V$, $V_{DS} = 45V$, $I_{DS} = 190$ mA and (c) $V_{GS} = -2.7V$, $V_{DS} = 40V$, $I_{DS} = 300$ mA. The tone-spacing is 200 KHz.

Verification tests shown in Figure 7.10 demonstrate the ability of the 3.2-mm device model to accurately simulate third-order intermodulation products, IMD3, for bias points of different power amplifier classes: in (a) I_{DS} was less than 5% of I_{DSS} , corresponding to class-C operation, in (b) V_{GS} was approximately V_{th} , corresponding to class-B operation, and in (c) I_{DS} was nearly 20% of I_{DSS} , corresponding to class-AB operation.

For the 2-mm device model, the verification test shown in Figure 7.9, showed accurate simulations of the IMD3 products for a bias point of class-AB power amplifier operation, where I_{DS} was less than 10% of I_{DSS} .

In concrete, correct simulations of IMD3 valleys or low-peaks (the so-called *sweet-spots*) at bias points with I_{DS} less than 10% of I_{DSS} represented a key feature of the presented models, towards their application in the design of highly-linear highly-efficient power amplifiers.

In the measurements reported in Figure 7.9 and Figure 7.10(a) the large-signal models predicted accurately the input powers and bias point ranges where *sweet spots* were measured.

As discussed in subsection 3.2.3.2, deviations between simulated and measured bias points were consequence of a residual error in calibrating the stabilizing element, during pulsed-DC IV measurements to acquire the I_{ds} -model database. Calibration of the stabilizing element was performed by the a built-in feature of the dynamic IV analyzer (DiVA[®]), which was found to let a residual error in the actual i_{DS} value reported as measured. In subsection 3.2.3.2, correction of this residual error was demonstrated with tuning of the simulated bias voltages within a 10%-range.

Although small, such 10% uncertainty of the bias points is considered to decrease the agreement between measured and simulated power of the IMD3 products, especially for bias points related to *sweet-spots*, because they are in the low- I_{DS} region, as in the cases of Figure 7.9 and Figure 7.10(a).

On other bias points (without appearance of *sweet spots*), simulated power of IMD3 products showed a close agreement with measurements, as exemplified in Figure 7.10(b) and (c). A maximum deviation of 5 dB between IMD3 simulations and measurements appeared only at extreme P_{in} and IMD3 values, like $P_{in} = -5$ dBm and IMD3 around -35 dB in Figure 7.10(b), and $P_{in} = +8$ dBm and IMD3 around 0 dB in Figure 7.10(c).

Decreased accuracy of simulated power of IMD3 products appearing in Figure 7.10(b) at low input power levels was attributed to the related low v_{GS} and v_{DS} values that control the reading of look-up-table files. If those voltage values are lower than the point-spacing of the voltage grid of the stored parameter values, then interpolation of the simulator decreases the model prediction accuracy. This decrease of accuracy related to low input powers was explained in [111], and a similar effect was discussed previously in the present section for the simulation of 3rd-harmonic output powers.

Chapter 8

Conclusions and Future Work

8.1 Conclusions from the Research Results

A large-signal modeling strategy to represent key effects of large-size advanced GaN HEMTs and produce accurate performance predictions for the design of UMTS power amplifiers has been presented, in accordance with the thesis main objective.

The proposed modeling strategy has applied empirical models with electrical equivalent circuits, following thus the premises of the thesis objectives regarding ease of implementation, generality and physical interpretation. The equivalent circuits have been directly implemented in CAD-software and the modeling has high generality of application because it has been based on electrical measurements and data accessible within typical device characterization facilities. Besides, the interpretations of model parameters and the extraction algorithms that have been presented preserve the physical meaning of the extracted parameter values, providing a valuable insight into the physics of the state-of-the-art GaN HEMTs.

Modeling of the drain current dispersive behavior observed in GaN devices has been undertaken with an empirical model based on pulsed-DC IV measurements. For the studied large-size devices, strong unstable operation appeared during pulsed-DC IV characterization, greatly reducing the acquirable database for modeling and subsequently the achievable model accuracy. These problems have been overcome applying a stabilization technique that effectively removed the constraints to the database. The applied stabilization technique makes possible pulsed-DC IV measurements on *quiescent* bias points with high DC dissipated power, e.g. P_{DS} up to nearly 3W/mm. Direct benefits of having a broad pulsed-DC IV database were the measurement-correlated I_{ds} -model parameter extraction that has been presented and the large-signal model accuracy for pulsed-DC IV verification tests that has been reported, even on *quiescent* bias points with high DC dissipated power, e.g. P_{DS} up to 12W.

The applied stabilization technique showed only one noticeable complication, related to calibration of the stabilizing element. The built-in feature of the dynamic IV analyzer DiVA[®] that calibrates the stabilization element did let a residual error in the I_{DS} value reported as measured, i.e. in the drain current of the bias point. However, such residual error was characterized to be small, accountable with a minor adjustment of the bias point voltages (a voltage adjustment of 10% or less with respect of the nominal values of the bias point). Moreover, noticeable effect of that small residual error has been observed only on two-tone verification tests at bias points with low I_{DS} (e.g. $I_{DS} \leq 10\%$ of I_{DSS}), where *sweet-spots* of IMD3 appear. The observed effect was that simulations of IMD3 at the *sweet-spots* were not as precise as at other IMD3 values. In any case, IMD3 predictions were considered good, since the large-signal models predict accurately the ranges of input power and bias where the *sweet-spots* occur.

Subchapters 6.3 and 6.4 sought to explain in detail the basic physical assumptions and definitions of the adopted I_{ds} model, which has allowed meaningful interpretations of the model parameters for charge-trapping and self-heating effects, including the time constants for the dynamics of these effects.

Clarification of the I_{ds} -model definitions and assumptions is considered important also for future model adaptations to represent more complex or different dispersion-inducing phenomena. For example: It was explained that the I_{ds} -model is a *linearization* (first-order series expansion) around an operating point with respect to the DC bias voltages and the channel temperature. But section 6.4.2 demonstrated that thermal states of the studied devices did not depend on the channel temperature (i.e. the dissipated power of the DC bias point) as linearly as assumed. Due to the understanding of the model assumptions, a possible future adaptation of the model is to consider 2nd-order terms of the series expansion with respect to the channel temperature (i.e. the dissipated power of the DC bias point).

Data from physics-based modeling, heat-transfer simulations of a 3.2-mm device for the calculation of τ_{th} and R_{th} , was available and has been used to exploit its typically improved accuracy with respect to purely empirical modeling. Then again, the I_{ds} -model parameter extraction has been demonstrated fully based on measurements, for a 2-mm device, including the time constants of charge-trapping and self-heating effects.

This is a key feature of the presented modeling strategy that emphasizes its empirical character.

In the model verification, the large-signal model has accurately predicted the low-frequency drain current on the pulsed-DC tests, as well as the RF drain current on the single-tone tests, where RF drain current is the key component of the predictions of power-added efficiency (PAE). Moreover, the dispersive I_{ds} -model has also predicted well the drain current in small-signal as demonstrated by the accuracy shown by the S-parameter tests.

The adopted large-signal model also accounts for the gate current, using conduction and displacement components related to the behavior of the charge under the gate. Frequency-dependent effects of the gate charge were represented with a non-quasi-static formulation. Accurate predictions of S-parameters obtained with the large-signal model have been presented as a good initial validation of the modeling of gate charge effects. Further validation has been provided by the accurate predictions for output power of the 2nd and 3rd harmonics in the single-tone tests of model verification.

The intrinsic part of the adopted large-signal equivalent circuit not only is physically meaningful but also directly compatible with the intrinsic transistor of the adopted small-signal equivalent circuit. Thus, intrinsic parameters of the large-signal model (other than I_{ds}) are obtained from measurement-correlated bias-dependent values of intrinsic parameters of the small-signal model.

All bias-dependent model parameters have been formulated in terms of intrinsic voltages, but obtained from data measured at the extrinsic device ports. Therefore, numerical processes of remapping and re-gridding have been required. The re-gridding has been shown to be especially critical, because the routine used to implement it (based on *b-splines*) produces unreliable extrapolated values, if it is not configured properly.

Appearance of unreliable extrapolated values has been eliminated with a simple numerical technique to represent the shifted *off-range* region of the voltage grids (the region where no measurements are available due to the DC power limit shifts with the voltage re-mapping). This numerical technique has been shown to avoid large errors in the voltage-dependent values of large-signal charge and current sources, without requiring case-specific obscure post-processing. This preserves the numerical quality of well-correlated data extracted from S-parameters measurements, for

example, for the look-up tables of the parameters R_i , R_{gd} and τ obtained in small-signal modeling and also employed in the large-signal model.

Increasingly large devices are designed to improve performance, but inevitably parasitic effects between the internal electrodes are also increased. Besides, field-plate structures of advanced GaN HEMTs have a strong influence on parasitic effects and basic considerations for the related modeling.

Both, the small and the large-signal model that were adopted use the same extrinsic parameters, a linear network wherein the intrinsic transistor is embedded, which represents the parasitic effects in the device.

In this thesis work a comprehensive network of 12 extrinsic elements has been adopted, which contains enough parameters to directly represent the most important parasitic effects expected in large-size GaN HEMTs. The direct connection of parasitic effects with extrinsic parameters was explained in detail, especially regarding the representation of device parasitic capacitive effects with the six extrinsic capacitance parameters. As far as could be traced in the literature of the field, this thesis presented for the first time direct expressions for those six parameters in terms of device physical structure.

The adopted comprehensive network of 12 extrinsic elements with six capacitance parameters requires a well-designed algorithm of parameter extraction to identify the required values from S-parameter measurements with the highest possible reliability, i.e. using mathematical optimization only for the last phase of refining with measurement-correlated high-quality starting values. The starting values found for the studied large-size devices generated accurate S-parameter predictions on the bias points employed for modeling, but also in bias points on the active IV region, producing intrinsic parameters with the expected frequency-independency. The similarity of the final optimized values of extrinsic parameters with starting values also proves the high-quality of the measurement-correlated extraction algorithm.

Those starting values were found adopting key ideas of the parameter extraction presented in [74], which was called TECR algorithm in this thesis. However, the basic assumptions of that algorithm were perfected in two ways. First, this thesis presented a method to evaluate the required capacitance ratio values with a high generality of application, using only

the physically-meaningful expressions derived for the capacitance parameters and top-view photographs of the device finger layout. In second term, the influence of physical features that can be expected in state-of-the-art large-size GaN HEMTs on capacitance ratio values has been taken into account for the derivation of reliable ratio values.

Table 4.2 presented in this thesis, provides a novel tool for the modeler. For the first time, it is indicated clearly which values of capacitance ratios is possible to assume reliably, from top-view images of the device, depending on the situation of the device finger layout, namely, on the absence or presence of field-plate structures or source air-bridges. That table represents a useful tool towards the general application of the adopted small-signal equivalent circuit and the related algorithm of parameter extraction.

Furthermore, the reliable extrinsic resistance parameter extraction has been presented in this thesis work in terms of S-parameters measurements with a simple linear fitting approximation, but circumventing the critical and case-specific *cold forward* condition. This is another point in favor of the generality of application of the extrinsic parameter extraction presented in this thesis work.

The high ratings of voltage, current or power of large devices eventually surpass the ratings of measurement equipment, limiting the accessible database for empirical modeling, and thus, the achievable model accuracy. In those cases, a scalable model is powerful tool to model large-size devices in an indirect way.

The scalability of the small-signal model derived with the parameter extraction presented in this thesis has been investigated. Scaling behavior of the extrinsic and intrinsic parameters observed a reasonably good agreement with the scaling of the gate width and in less extent with the scaling of the number of fingers. Only two device sizes were available to verify to the fullest extent the scalability in terms of the number of fingers, e.g., for extrinsic capacitance parameters related to capacitive effects of the contacting pads. Nonetheless, an indirect modeling of the large-size 3.2-mm device was carried out and the resulting scaled small-signal model presented an acceptable agreement of predictions with measured S-parameters, so that the scaled models represent a useful tool for large-size device performance prognosis, e.g. for device optimization.

8.2 Outlook of Future Work

The following are proposals of future work that outcome of work reported in this thesis. They are listed roughly in order of appearance of the related topic in the thesis:

- The reliable evaluation of capacitance ratio values employs top-view images and closed expressions in the form $C = \varepsilon \cdot A/d$. This equation is for the capacitance in homogenous dielectric material, whereas the material where actual parasitic capacitive effects of the device might be heterogeneous. 3D electromagnetic simulations should help assessing the deviation of the related capacitance ratio value from the ideal consideration of homogeneity to the real case. The deviation can be then expressed as a correction factor of the value obtained from the top-view images and the closed expressions derived from $C = \varepsilon \cdot A/d$.
- Investigation of model parameter scalability with respect to the number of gate fingers with devices in step sizes starting with more than 2 fingers.
- Investigation of existence of bias-dependency in the values of the extrinsic resistance parameters, particularly for the source and drain resistances [90, 100, 101], applying an appropriate at-bias extraction as in [77, 125, 126], suitably modified for the comprehensive extrinsic element network.
- Adaptation of the extrinsic elements of the employed equivalent circuits to account for substrate-related parasitic effects appearing on devices built over Si-substrates [69, 127, 128].
- Investigations of large-signal table-based empirical models employing pulsed-DC S-parameters and X-parameters.
- Investigations of large-signal table-based empirical models similar to the one employed in this thesis work but using ANN (artificial neural networks) to approximate, re-grid, interpolate and/or extrapolate the obtained bias-dependent values of the model parameters instead of the *spline* techniques employed in this thesis work.

On another hand, GaN HEMTs are being investigated for their application in switched-mode power amplifiers for novel transmitter architectures, like the class-S concept. For that, device modeling strategies

oriented to switched-mode amplifier design are still under development. Empirical models known as compact models can be used as an alternative for switched-mode amplifier design, which appear to be suitable for the required transient simulations in the four quadrants of the IV plane. This type of compact models should be investigated, like the Angelov model version presented in [129].

References

- [1] ITU, "The World in Facts and Figures" *International Telecommunication Union - Newsroom - Reports and Analysis*. Available Online: <http://www.itu.int/ITU-D/ict/material/FactsFigures2010.pdf>. Last time accessed on: 29/11/2011
- [2] ITU, "What Really Is a Third Generation (3G) Mobile Technology?" *2G / 3G / 4G*. Available Online: http://www.itu.int/ITU-D/imt-2000/DocumentsIMT2000/What_really_3G.pdf. Last time accessed on: 29/11/2011
- [3] D. W. Lee, K. Yoo, J. S. Kim, M. J. Kim, and J. H. Park, "Development of the Base Station Transceiver Subsystem in the CDMA Mobile System," *ETRI Journal*, Vol. 19, No. 3, pp. 116-140, 1997.
- [4] J. Häkkinen, "Integrated RF building blocks for base station applications," PhD Dissertation. University of Oulu, Finland, 2002.
- [5] R. J. Trew, "Wide Bandgap Semiconductor Transistors for Microwave Power Amplifiers," *IEEE Microwave Magazine*, Vol. 1, No. 1, pp. 46-54, 2000.
- [6] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Potheary, J. F. Sevic, and N. O. Sokal, "RF and Microwave Power Amplifier and Transmitter Technologies - Part 1," *High Frequency Electronics*, Vol. 2, No. 3, pp. 22-36, 2003.
- [7] EMRS-DTC of the United Kingdom Ministry of Defence, "Gallium Nitride Growth on Silicon for Microwave Heterojunction Field Effect Transistors" *EMRS-DTC Briefing Papers*. Available Online: <http://www.emrstdtc.com/downloads/pdf/ganigr.pdf>. Last time accessed on: 29/11/2011
- [8] J. Gao, *RF and Microwave Modeling and Measurement Techniques for Field Effect Transistors*: SciTech Publishing, 2010.
- [9] D. E. Root and S. Fan, "Experimental Evaluation of Large-Signal Modeling Assumptions Based on Vector Analysis of Bias-Dependent S-Parameter Data from MESFETs and HEMTs," *IEEE MTT-S. International Microwave Symposium Digest*, pp. 255-258, 1992.
- [10] L. F. Eastman and U. K. Mishra, "The Toughest Transistor Yet [GaN Transistors]?", *IEEE Spectrum*, Vol. 39, No. 5, pp. 28-33, 2002.
- [11] R. Crampton, "GaN-on-Si RF Power Transistors Combine High Performance and Affordability" Available Online: <http://www.mpdigest.com/issue/Articles/2008/Oct/nitronex/Default.asp>. Last time accessed on: 29/11/2011
- [12] B. Ozpineci, L. M. Tolbert, S. K. Islam, and M. Chinthavali, "Comparison of Wide Bandgap Semiconductors for Power Electronics," *Proceedings of the 10th European Conference on Power Electronics and Applications*, pp. 257-264, September 2003.

- [13] Y. Gurbuz , O. Esame, I. Tekin, W. P. Kang, and J. L. Davidson, "*Diamond Semiconductor Technology for RF Device Applications*," Solid-State Electronics, Vol. 49, No. 7, pp. 1055-1070, 2005.
- [14] T. Mimura, "*The Early History of the High Electron Mobility Transistor (HEMT)*," IEEE Transactions on Microwave Theory and Techniques, Vol. 50, No. 3, pp. 780-782, 2002.
- [15] G. Fischer, W. Eckl, and G. Kaminski, "*RF-MEMS and SiC/GaN as Enabling Technologies for a Reconfigurable Multi-Band/Multi-Standard Radio*," Bell Labs Technical Journal, Vol. 7, No. 3, pp. 169-189, 2003.
- [16] T. Lenka and A. Panda, "*Characteristics Study of 2DEG Transport Properties of AlGaN/GaN and AlGaAs/GaAs-Based HEMT*," Journal of Semiconductors, Vol. 45, No. 5, pp. 650-656, 2011.
- [17] U. K. Mishra, L. Shen, T. E. Kazior, and W. Yi-Feng, "*GaN-Based RF Power Devices and Amplifiers*," Proceedings of the IEEE, Vol. 96, No. 2, pp. 287-305, 2008.
- [18] C. E. Weitzel, "*RF Power Devices for Wireless Communications*," IEEE MTT-S. International Microwave Symposium Digest, pp. 285-288, 2002.
- [19] R. Borges, "*Gallium Nitride Electronic Devices for High-Power Wireless Applications*," RF Design, pp. 72-82, Sep 2001.
- [20] O. Hammi and F. M. Ghannouchi, "Comparative Study of Recent Advances in Power Amplification Devices and Circuits for Wireless Communication Infrastructure," *Proceedings of the 16th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 379-382, December 2009.
- [21] N. R. Mohapatra, H. Ruecker, K. E. Ehwald, R. Sorge, R. Barth, P. Schley, D. Schmidt, and H. E. Wulf, "A Complementary RF-LDMOS Architecture Compatible with 0.13-micron CMOS Technology," *Proceedings of the IEEE International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, pp. 1-4, June 2006.
- [22] K.-E. Ehwald, B. Heinemann, W. Roepke, W. Winkler, H. Rucker, F. Fuernhammer, D. Knoll, R. Barth, B. Hunger, H. E. Wulf, R. Pazirandeh, and N. Ilkov, "High Performance RF LDMOS Transistors with 5-nm Gate Oxide in a 0.25 μm SiGe:C BiCMOS Technology," *Proceedings of the International Electron Devices Meeting (IEDM)*, pp. 40.4.1-40.4.4, April 2001.
- [23] K. Matsunaga, K. Ishikura, I. Takenaka, W. Contrata, A. Wakejima, K. Ota, M. Kanamori, and M. Kuzuhara, "A Low-Distortion 230 W GaAs Power FP-HFET Operated at 22 V for Cellular Base Stations," *Proceedings of the International Electron Devices Meeting (IEDM)*, pp. 393-396 December 2000.
- [24] T. Palacios, A. Chakraborty, S. Rajan, C. Poblenz, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "*High-Power AlGaIn/GaN HEMTs for Ka-Band*

- Applications*," IEEE Electron Device Letters, Vol. 26, No. 11, pp. 781-783, 2005.
- [25] Y. Pei, R. Chu, N. A. Fichtenbaum, Z. Chen, D. Brown, L. Shen, S. Keller, S. P. DenBaars, and U. K. Mishra, "*Recessed Slant Gate AlGaIn/GaN High Electron Mobility Transistors with 20.9 W/mm at 10 GHz*," Japanese Journal of Applied Physics, Vol. 46-2, No. 46, pp. L1087-L1089, 2007.
 - [26] R. J. Trew, G. L. Bilbro, W. Kuang, Y. Liu, and H. Yin, "*Microwave AlGaIn/GaN HFETs*," IEEE Microwave Magazine, Vol. 6, No. 1, pp. 56-66, 2005.
 - [27] Y.-F. Wu, M. Moore, A. Abrahamsen, M. Jacob-Mitos, P. Parikh, S. Heikman, and A. Burk, "High-Voltage Millimeter-Wave GaN HEMTs with 13.7 W/mm Power Density," *Proceedings of the International Electron Devices Meeting, IEDM*, pp. 405-407, Dec 2007.
 - [28] Y.-F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, T. Wisleder, U. K. Mishra, and P. Parikh, "*30-W/mm GaN HEMTs by Field Plate Optimization*," IEEE Electron Device Letters, Vol. 25, No. 3, pp. 117-119, 2004.
 - [29] N. Rorsman, J. Olsson, C. Fager, L. Vestling, J. Ankarcrona, H. Zirath, and K. H. Eklund, "*1 W/mm RF Power Density at 3.2 GHz for a Dual-Layer RESURF LDMOS Transistor*," IEEE Electron Device Letters, Vol. 23, No. 4, pp. 206-208, 2002.
 - [30] C. E. Weitzel and K. E. Moore, "*Performance Comparison of Wide Bandgap Semiconductor RF Power Devices*," Journal of Electronic Materials, Vol. 27, No. 4, pp. 365-369, 1998.
 - [31] Y.-S. Lee, M.-W. Lee, and Y.-H. Jeong, "*Experimental Analysis of GaN HEMT and Si LDMOS in Analog Predistortion Power Amplifiers for WCDMA Applications*," Microwave and Optical Technology Letters, Vol. 50, No. 2, pp. 393-396, 2008.
 - [32] J. W. Chung, J.-K. Lee, E. L. Piner, and T. Palacios, "*Seamless On-Wafer Integration of Si(100) MOSFETs and GaN HEMTs*," IEEE Electron Device Letters, Vol. 30, No. 10, pp. 1015-1017, 2009.
 - [33] U. K. Mishra, P. Parikh, and W. Yi-Feng, "*AlGaIn/GaN HEMTs - An Overview of Device Operation and Applications*," Proceedings of the IEEE, Vol. 90, No. 6, pp. 1022-1031, 2002.
 - [34] A. Ramadan, "Active Antennas with High Input Impedance Low Noise and Highly Linear Amplifiers," PhD Dissertation. Universität der Bundeswehr München, 2005.
 - [35] U. K. Mishra, "Lessons in Compound Semiconductor Device Development," *Proceedings of the IEEE Lester Eastman Conference on High Performance Devices*, pp. 9-21, Aug 2002.

- [36] R. Chu, Z. Chen, P. Yi, S. Newman, S. P. DenBaars, and U. K. Mishra, "*MOCVD-Grown AlGa_N Buffer Ga_N HEMTs With V-Gates for Microwave Power Applications*," IEEE Electron Device Letters, Vol. 30, No. 9, pp. 910-912, 2009.
- [37] R. T. Green, I. J. Luxmoore, K. B. Lee, P. A. Houston, F. Ranalli, T. Wang, P. J. Parbrook, M. J. Uren, D. J. Wallis, and T. Martin, "*Characterization of Gate Recessed Ga_N/AlGa_N/Ga_N HEMTs Fabricated Using a SiCl₄/SF₆ Dry Etch Recipe*," Journal of Applied Physics, Vol. 108, No. 1, pp. 013711-013717, 2010.
- [38] J. R. Shealy, V. Kaper, V. Tilak, T. Prunty, J. A. Smart, B. Green, and L. F. Eastman, "*An AlGa_N/Ga_N High-Electron-Mobility Transistor with an AlN Sub-Buffer Layer*," Journal of Physics: Condensed Matter, Vol. 14, No. 13, pp. 3499-3509, 2002.
- [39] R. Chu, Z. Chen, P. Yi, S. Newman, S. P. DenBaars, and U. K. Mishra, "*MOCVD-Grown AlGa_N Buffer Ga_N HEMTs With V-Gates for Microwave Power Applications*," IEEE Electron Device Letters., Vol. 30, No. 9, pp. 910-912, 2009.
- [40] S. Karmalkar and U. K. Mishra, "*Enhancement of Breakdown Voltage in AlGa_N/Ga_N High Electron Mobility Transistors Using a Field Plate*," IEEE Transactions on Electron Devices, Vol. 48, No. 8, pp. 1515-1521, 2001.
- [41] R. J. Trew, G. L. Bilbro, W. Kuang, Y. Liu, and H. Yin, "*Microwave AlGa_N/Ga_N HFETs*," IEEE Microwave Magazine, Vol. 6, No. 1, pp. 56- 66, 2005.
- [42] W. Saito, Y. Kakiuchi, T. Nitta, Y. Saito, T. Noda, H. Fujimoto, A. Yoshioka, T. Ohno, and M. Yamaguchi, "*Field-Plate Structure Dependence of Current Collapse Phenomena in High-Voltage Ga_N-HEMTs*," IEEE Transactions on Microwave Theory and Techniques, Vol. 31, No. 7, pp. 659-661, 2010.
- [43] E. Kohn, I. Daumiller, P. Schmid, N. X. Nguyen, and C. N. Nguyen, "*Large Signal Frequency Dispersion of AlGa_N/Ga_N Heterostructure Field Effect Transistors*," Electronics Letters, Vol. 35, No. 12, pp. 1022-1024, 1999.
- [44] M. A. Khan, M. S. Shur, Q. C. Chen, and J. N. Kuznia, "*Current/Voltage Characteristic Collapse in AlGa_N/Ga_N Heterostructure Insulated Gate Field Effect Transistors at High Drain Bias*," Electronics Letters, Vol. 30, No. 25, pp. 2175-2176, 1994.
- [45] S. C. Binari, P. B. Klein, and T. E. Kazior, "*Trapping Effects in Wide-Bandgap Microwave FETs*," IEEE MTT-S. International Microwave Symposium Digest, Vol. 3, pp. 1823-1826, 2002.
- [46] R. Quay, *Gallium Nitride Electronics*: Springer-Verlag, 2008.

- [47] T. Goudon, V. Miljanovi, and C. Schmeiser, "*On the Shockley–Read–Hall Model: Generation-Recombination in Semiconductors*," SIAM Journal on Applied Mathematics, Vol. 67, No. 4, pp. 1183-1201, 2007.
- [48] J. C. Bourgoin, H. J. von Bardeleben, and D. Stiévenard, "*Native Defects in Gallium Arsenide*," Journal of Applied Physics, Vol. 64, No. 9, pp. R65-R81, 1988.
- [49] W. S. Yan, R. Zhang, Z. L. Xie, X. Q. Xiu, P. Han, H. Lu, P. Chen, S. L. Gu, Y. Shi, Y. D. Zheng, and Z. G. Liu, "*A Thermodynamic Model and Estimation of the Experimental Value of Spontaneous Polarization in a Wurtzite GaN*," Applied Physics Letters, Vol. 94, No. 4, pp. 042106-042109, 2009.
- [50] J. R. Shealy, J. Wang, and R. Brown, "*Methodology for Small-Signal Model Extraction of AlGaN HEMTs*," IEEE Transactions on Electron Devices, Vol. 55, No. 7, pp. 1603-1613, 2008.
- [51] Nitronex©, "AN-011: Substrates for GaN RF Devices" *GaN Essentials*. Available Online: www.nitronex.com/pdfs/AN-011%20GaN%20Substrates.pdf. Last time accessed on: 29/11/2011
- [52] R. Lossy, N. Chaturvedi, P. Heymann, K. Köhler, S. Müller, and J. Würfl, "*Large Area AlGaIn/GaN HEMTs Grown on Insulating Silicon Carbide Substrates*," Physica Status Solidi, Vol. 194, No. 2, pp. 460-463, 2002.
- [53] C. L. Tan, H. Wang, and K. Radhakrishnan, "*Hot-Electron-Induced Degradation in BCB- and SiN-Passivated Al_{0.25}Ga_{0.75}As/In_{0.2}Ga_{0.8}As PHEMTs*," IEEE Transactions on Device and Materials Reliability, Vol. 7, No. 3, pp. 438-446, 2007.
- [54] G. Kompa, *Practical Microstrip Design and Applications*: Artech House, 2006.
- [55] Agilent Technologies Inc ©, "Basics of DC and AC Characterization of Semiconductors" *Presentation on AC and DC Characterization of Semiconductors*. Available Online: <http://cp.literature.agilent.com/litweb/pdf/5989-9034EN.pdf>. Last time accessed on: 29/11/2011
- [56] G. Kompa and M. Novotny, "Frequency-Dependent Measurement Error Analysis and Refined FET Model Parameter Extraction Including Bias-Dependent Series Resistors," in *International IEEE Experimentally Based FET Device Modeling and Related Nonlinear Circuit Design Workshop*, University of Kassel, Germany, pp. 6.1-6.16, 1997.
- [57] Agilent Technologies Inc ©, "Application Note - Network Analyzer Basics," 5301 Stevens Creek Blvd., Santa Clara, CA 95052 USA, 2004.
- [58] Hewlett-Packard Company, "System Manual of the HP8510B Network Analyzer," P/N 08510-90074, Santa Rosa, CA., 1987.

- [59] G. Kompa and M. Novotny, "*Highly Consistent FET Model Parameter Extraction Based on Broadband S-Parameter Measurements*," IEEE MTT-S. International Microwave Symposium Digest, Vol. 1, pp. 293-296, 1992.
- [60] S. S. Lu, C. Meng, T. W. Chen, and H. S. Chen, "*The Origin of the Kink Phenomenon of Transistor Scattering Parameter S_{22}* ," IEEE Transactions on Microwave Theory and Techniques, Vol. 49, No. 2, pp. 333-340, 2001.
- [61] V. Camarchia, F. Cappelluti, M. Pirola, S. Donati Guerrieri, and G. Ghione, "*Self-Consistent Electrothermal Modeling of Class A, AB, and B Power GaN HEMTs Under Modulated RF Excitation*," IEEE Transactions on Microwave Theory and Techniques, Vol. 55, No. 0, pp. 1824-1831, 2007.
- [62] CREE®, "Datasheet of the GaN HEMT with product number CGH60030D " Available Online: <http://www.cree.com/products/pdf/CGH60030D.pdf>. Last time accessed on: 29/11/2011
- [63] M. Fernandez-Barciela, P. J. Tasker, Y. Campos-Roca, M. Demmler, H. Massler, E. Sanchez, M. C. Curras-Francos, and M. Schlechtweg, "*A Simplified Broad-Band Large-Signal Nonquasi-Static Table-Based FET Model*," IEEE Transactions on Microwave Theory and Techniques, Vol. 48, No. 3, pp. 395-405, 2000.
- [64] A. Jarndal, "Large-Signal Modeling of GaN Device for High Power Amplifier Design," Doctoral Thesis. Department of High-Frequency Technique, University of Kassel, Kassel, Germany, 2006.
- [65] E. S. Mengistu, "Large-Signal Modeling of GaN HEMTs for Linear High Power Amplifier Design," Doctoral Thesis. Department of High-Frequency Technique, University of Kassel, Kassel, Germany, 2008.
- [66] A. Santarelli, V. Di Giacomo, A. Raffo, P. A. Traverso, G. Vannini, and F. Filicori, "*A Nonquasi-Static Empirical Model of Electron Devices* " IEEE Transactions on Microwave Theory and Techniques, Vol. 54, No. 12, pp. 4021-4031, 2006.
- [67] R. G. Brady, C. H. Oxley, and T. J. Brazil, "*An Improved Small-Signal Parameter-Extraction Algorithm for GaN HEMT Devices*," IEEE Transactions on Microwave Theory and Techniques, Vol. 56, No. 7, pp. 1535-1544 2008.
- [68] G. Chen, V. Kumar, R. Schwindt, and I. Adesida, "*A Low Gate Bias Model Extraction Technique for AlGaIn/GaN HEMTs*," IEEE Transactions on Microwave Theory and Techniques, Vol. 54, No. 7, pp. 2949-2953, 2006.
- [69] G. Crupi, D. P. Xiao, D. M. M.-P. Schreurs, E. Limiti, A. Caddemi, W. De Raedt, and M. Germain, "*Accurate Multibias Equivalent-Circuit Extraction for GaN HEMTs*," IEEE Transactions on Microwave Theory and Techniques, Vol. 54, No. 10, pp. 3616-3622, 2006.
- [70] Accent Optical Technologies Inc. ©, "Dynamic I(V) Analyzer Applications Manual. Issue 1.0," 131 NW Hawthorne Bend, Oregon 97701, 2004.

- [71] E. R. Srinidhi, R. Ma, and G. Kompa, "Application Rules for Accurate IMD Characterization in GaN HEMTs," *Proceedings of the German Microwave Conference (GeMIC)*, pp. 171-174, March 2008.
- [72] B. Wittwer, E. R. Srinidhi, G. Kompa, and A. Bangert, "ACP and IMD3 Measurement and Comparison Using a Novel Load-Pull System," *Proceedings of the European Microwave Conference (EuMC)*, pp. 1568-1571, September 2010.
- [73] A. Jarndal, "Genetic Algorithm Based Extraction Method for Distributed Small-Signal Model of GaN HEMTs," *Proceedings of the IEEE International Conference on Semiconductor Electronics (ICSE)*, pp. 41-44, June 2010.
- [74] A. Jarndal and G. Kompa, "A New Small-Signal Modeling Approach Applied to GaN Devices," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 53, No. 11, pp. 3440-3448, 2005.
- [75] A. Jarndal and G. Kompa, "A New Small Signal Model Parameter Extraction Method Applied to GaN Devices," *IEEE MTT-S. International Microwave Symposium Digest*, Vol. 2, pp. 1423-1426, 2005.
- [76] A. Jarndal and G. Kompa, "An Accurate Small-Signal Model for AlGaIn-GaN HEMT Suitable for Scalable Large-Signal Model Construction," *IEEE Microwave and Wireless Components Letters*, Vol. 16, No. 6, pp. 333-335, 2006.
- [77] Q. Fan, J. H. Leach, and H. Morkoc, "Small Signal Equivalent Circuit Modeling for AlGaIn/GaN HFET: Hybrid Extraction Method for Determining Circuit Elements of AlGaIn/GaN HFET," *Proceedings of the IEEE*, Vol. 98, No. 7, pp. 1140-1150, 2010.
- [78] A. Zarate-de Landa, J. Zuniga-Juarez, J. Loo-Yau, J. Reynoso-Hernandez, M. Maya-Sanchez, and J. del Valle-Padilla, "Advances in Linear Modeling of Microwave Transistors," *IEEE Microwave Magazine*, Vol. 10, No. 2, pp. 100-111, 146, 2009.
- [79] M. Berroth, E. Chigaeva, I. Dettman, N. Wieser, W. Vogel, H. Roll, F. Scholz, and H. Schweizer, "Advanced large-signal modeling of GaN-HEMTs," *Proceedings of the IEEE Lester Eastman Conference on High Performance Devices*, pp. 172-180, August 2002.
- [80] E. Chigaeva, W. Walther, D. Wiegner, M. Grozing, F. Schaich, N. Wieser, M. Berroth, O. Breitschadel, L. Kley, B. Kuhn, F. Scholz, H. Schweizer, O. Ambacher, and J. Hilsenbeck, "Determination of Small-Signal Parameters of GaN-Based HEMTs," *Proceedings of the IEEE/Cornell Conference on High Performance Devices*, pp. 115-122, August 2000.
- [81] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A New Method for Determining the FET Small-Signal Equivalent Circuit," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 33, No. 7, pp. 1151-1159, 1988.

- [82] R. Lossy, N. Chaturvedi, P. Heymann, K. Köhler, S. Müller, and J. Würfl, "AlGaN/GaN HEMTs on Silicon Carbide Substrates for Microwave Power Operation," *Proceedings of the International Conference on Compound Semiconductor Manufacturing Technology, GaAs ManTech*, pp. 327-330, May 2003.
- [83] N. Mwema, "A Reliable Optimisation-Based Model Parameter Extraction," Doctoral Thesis. Department of High-Frequency Technique, University of Kassel, Kassel, Germany, 2002.
- [84] M. Teng, H. Yue, C. Chi, and M. Xiaohua, "A New Small-Signal Model for Asymmetrical AlGaN/GaN HEMTs," *Journal of Semiconductors*, Vol. 31, No. 6, pp. 064002 1-5, 2010.
- [85] Z. G. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, K. L. Teo, S. C. Foo, and V. Sahmuganathan, "Comprehensive Study on the Bias-Dependent Equivalent-Circuit Elements Affected by PECVD SiN Passivation in AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, Vol. 58, No. 2, pp. 473-479, 2011.
- [86] T. Mizutani, Y. Ohno, M. Akita, S. Kishimoto, and K. Maezawa, "A Study on Current Collapse in AlGaN/GaN HEMTs Induced by Bias Stress," *IEEE Transactions on Electron Devices*, Vol. 50, No. 10, pp. 2015-2020, 2003.
- [87] Y. Tajima, "100 W GaN HEMT Modeling," *Microwave Journal*, Vol. 50, No. 5, pp. 204-215, 2007.
- [88] A. Koudymov, V. Adivarahan, J. Yang, G. Simon, and M. Asif Khan, "Mechanism of Current Collapse Removal in Field-Plated Nitride HFETs," *IEEE Electron Device Letters*, Vol. 26, No. 10, pp. 704-706, 2005.
- [89] S. Sriram, H. Hagleitner, D. Namishia, T. Alcorn, T. Smith, and B. Pulz, "High-Gain SiC MESFETs Using Source-Connected Field Plates," *IEEE Electron Device Letters*, Vol. 30, No. 9, pp. 952-953, 2009.
- [90] G. Kompa, "Reliable Extraction of Small-Signal Elements of a Generalized Distributed FET Model " *IEEE MTT-S. International Microwave Symposium Digest*, Vol. 1, pp. 291-294 1998.
- [91] K. L. Kotzebue, "Maximally Efficient Gain: A Figure of Merit for Linear Active 2-Ports," *Electronics Letters*, Vol. 12, No. 19, pp. 490-491, 1976.
- [92] M.-Y. Jeon, B.-G. Kim, Y.-J. Jeon, and Y.-H. Jeong, "A Technique for Extracting Small-Signal Equivalent-Circuit Elements of HEMTs " *IEICE transactions on electronics (Special Issue on High-Frequency/Speed Devices in the 21st Century)*, Vol. 82, No. 11, pp. 1968-1976, 1999.
- [93] J. Lu, Y. Wang, L. Ma, and Z. Yu, "A New Small-Signal Modeling and Extraction Method in AlGaN/GaN HEMTs," *Solid-State Electronics*, Vol. 52, No. 1, pp. 115-120 2008.

- [94] S. Manohar, A. Narayanan, A. Keerti, A. Pham, J. Brown, R. Borges, and K. Linthicum, "*Characteristics of Microwave Power GaN HEMTs on 4-Inch Si Wafers*," IEEE MTT-S. International Microwave Symposium Digest, pp. 449-452, 2002.
- [95] A. Caddemi, G. Crupi, and N. Donato, "*Microwave Characterization and Modeling of Packaged HEMTs by a Direct Extraction Procedure Down to 30 °K*," IEEE Transactions on Instrumentation and Measurement, Vol. 55, No. 2, pp. 465-470, 2006.
- [96] R. Goyal, *Monolithic Microwave Integrated Circuits: Technology and Design*: Artch House, 1989.
- [97] J. Wood and D. E. Root, "*Bias-Dependent Linear Scalable Millimeter-Wave FET Model*," IEEE Transactions on Microwave Theory and Techniques, Vol. 48, No. 12, pp. 2252-2260, 2000.
- [98] J. Liu, Y. Zhou, J. Zhu, Y. Cai, K. M. Lau, and K. J. Chen, "*DC and RF Characteristics of AlGaIn/GaN/InGaIn/GaN Double-Heterojunction HEMTs* " IEEE Transactions on Electron Devices, Vol. 54, No. 1, pp. 2-10, 2007.
- [99] F. van Raay, R. Quay, R. Kiefer, M. Schlechtweg, and G. Weimann, "*Large Signal Modeling of AlGaIn/GaN HEMTs with $P_{sat} > 4$ W/mm at 30 GHz Suitable for Broadband Power Applications*," IEEE MTT-S. International Microwave Symposium Digest, Vol. 1, pp. 451-454, 2003.
- [100] F. Kharabi, J. R. F. McMacken, and J. M. Gering, "A Verilog-A Large-Signal GaN HEMT Model for High Power Amplifier Design," *Proceedings of the IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, pp. 1-4, October 2010.
- [101] R. J. Trew, Y. Liu, L. Bilbro, W. Kuang, R. Vetry, and J. B. Shealy, "*Nonlinear Source Resistance in High-Voltage Microwave AlGaIn/GaN HFETs* " IEEE Transactions on Microwave Theory and Techniques, Vol. 54, No. 5, pp. 2061-2067, 2006.
- [102] R. Vetry, N. Q. Zhang, S. Keller, and U. K. Mishra, "*The Impact of Surface States on the DC and RF Characteristics of AlGaIn/GaN HFETs*," IEEE Transactions on Electron Devices, Vol. 48, No. 3, pp. 560-566, 2001.
- [103] S. Dahmani, E. S. Mengistu, and G. Kompa, "Electro-Thermal Modeling of Large-Size GaN HEMTs " *Proceedings of the German Microwave Conference (GeMIC)*, pp. 1-4, March 2008.
- [104] S. Dahmani, E. S. Mengistu, and G. Kompa, "Thermal Model Extraction of GaN HEMTs for Large-Signal Modeling," *Proceedings of the European Microwave Integrated Circuits Conference (EuMIC)*, pp. 226-229, October 2008.
- [105] J. J. Paulos and D. A. Antoniadis, "*Limitations of Quasi-Static Capacitance Models for the MOS Transistor*," IEEE Electron Device Letters, Vol. 4, No. 7, pp. 221-224, 1983.

- [106] N. Gauthier, "*Displacement Current, Transport Current, and Charge Conservation*," American Journal of Physics, Vol. 51, No. 2, pp. 168-170, 1983.
- [107] O. Soo-Young, D. E. Ward, and R. W. Dutton, "*Transient Analysis of MOS Transistors*," Japanese Journal of Applied Physics, Vol. 15, No. 4, pp. 636-643, 1980.
- [108] M. E. Zahn, "*Calculation of the Turn-on Behavior of MOST*," Solid-State Electronics, Vol. 17, No. 8, pp. 843-854, 1974.
- [109] J. W. Haslett and F. N. Trofimenkoff, "*Small-Signal, High-Frequency Equivalent Circuit for the Metal-Oxide-Semiconductor Field-Effect Transistor*," Proceedings of the IEE, Vol. 16, No. 5, pp. 699-702, 1969.
- [110] G. Kompa, "*Modeling of Dispersive Microwave FET Devices Using a Quasi-Static Approach*," International Journal of Microwave and Millimeter-Wave Computer-Aided Engineering, Vol. 5, No. 3, pp. 173-194, 1995.
- [111] A. Jarndal and G. Kompa, "*Large-Signal Model for AlGaIn/GaN HEMTs Accurately Predicts Trapping- and Self-Heating-Induced Dispersion and Intermodulation Distortion*," IEEE Transactions on Electron Devices, Vol. 54, No. 11, pp. 2830-2836, 2007.
- [112] MathWorks[®], "1-D data interpolation (table lookup)" *Product Documentation of Matlab[®] R2011b*. Available Online: <http://www.mathworks.de/help/techdoc/ref/interp1.html>. Last time accessed on: 29/11/2011
- [113] A. Santarelli, V. Di Giacomo, A. Raffo, F. Filicori, G. Vannini, R. Aubry, and C. Gaquière, "*Nonquasi-Static Large-Signal Model of GaN FETs Through an Equivalent Voltage Approach*," International Journal of RF and Microwave Computer-Aided Engineering, Vol. 18, No. 6, pp. 507-516, 2008.
- [114] J.-P. Teyssier, D. Barataud, C. Charbonniaud, F. De Groote, M. Mayer, J.-M. Nébus, and R. Quéré, "*Large-Signal Characterization of Microwave Power Devices*," International Journal of RF and Microwave Computer-Aided Engineering, Vol. 15, No. 5, pp. 479-490, 2005.
- [115] F. Filicori, G. Vannini, A. Santarelli, A. M. Sanchez, A. Tazon, and Y. Newport, "*Empirical Modeling of Low-Frequency Dispersive Effects Due to Traps and Thermal Phenomena in III-V FET's*," IEEE Transactions on Microwave Theory and Techniques, Vol. 43, No. 12, pp. 2972-2981, 1995.
- [116] M. Chaibi, T. Fernandez, J. Rodriguez-Tellez, J. L. Cano, and M. Aghoutane, "*Accurate Large-Signal Single Current Source Thermal Model for GaAs MESFET/HEMT*," Electronics Letters, Vol. 43, No. 14, 2007.
- [117] K. Jeon, Y. Kwon, and S. Hong, "*A Frequency Dispersion Model of GaAs MESFET for Large-Signal Applications*," IEEE Microwave and Guided Wave Letters, Vol. 7, No. 3, pp. 78-80, 1997.

- [118] A. Raffo, V. Vadala, G. Vannini, and A. Santarelli, "A New Empirical Model for the Characterization of Low-Frequency Dispersive Effects in FET Electron Devices Accounting for Thermal Influence on the Trapping State," IEEE MTT-S. International Microwave Symposium Digest, pp. 1421-1424, 2008.
- [119] T. Roh, Y. Kim, Y. Suh, W. Park, and B. Kim, "A Simple and Accurate MESFET Channel-Current Model Including Bias-Dependent Dispersion and Thermal Phenomena," IEEE Transactions on Microwave Theory and Techniques, Vol. 45, No. 8, pp. 1252-1255, 1997.
- [120] P. McGovern, J. Benedikt, P. J. Tasker, J. Powell, K. P. Hilton, J. L. Glasper, R. S. Balmer, T. Martin, and M. J. Uren, "Analysis of DC-RF Dispersion in AlGaIn/GaN HFET's Using Pulsed I-V and Time-Domain Waveform Measurements," IEEE MTT-S. International Microwave Symposium Digest, Vol. 2, pp. 4-8, 2005.
- [121] J. Rodriguez-Tellez, T. Fernandez, A. Mediavilla, and A. Tazon, "Characterization of Thermal and Frequency-Dispersion Effects in GaAs MESFET Devices," IEEE Transactions on Microwave Theory and Techniques, Vol. 49, No. 7, pp. 1352-1355, 2001.
- [122] E. S. Mengistu and G. Kompa, "A Large-Signal Model of GaN HEMTs for Linear High Power Amplifier Design " *Proceedings of the European Microwave Integrated Circuits Conference (EuMIC)*, pp. 292-295, September 2006.
- [123] V. Di Giacomo, A. Santarelli, F. Filicori, A. Raffo, G. Vannini, R. Aubry, and C. Gaquière, "Low-Frequency Dynamic Drain Current Modeling in AlGaIn-GaN HEMTs," *Proceedings of the European Microwave Integrated Circuits Conference (EuMIC)*, pp. 68-71, October 2007.
- [124] S. Dahmani, *Private Communications*, Kassel University, Kassel, Germany, 2011.
- [125] D. Di Santo and C. R. Bolognesi, "At-Bias Extraction of Access Parasitic Resistances in AlGaIn/GaN HEMTs: Impact on Device Linearity and Channel Electron Velocity," IEEE Transactions on Electron Devices, Vol. 53, No. 12, pp. 2914-2919, 2006.
- [126] S. Manohar, A. Pham, and N. Evers, "Direct Determination of the Bias-Dependent Series Parasitic Elements in SiC MESFETs," IEEE Transactions on Microwave Theory and Techniques, Vol. 51, No. 2, pp. 597-600, 2003.
- [127] E. M. Chumbes, A. T. Schremer, J. A. Smart, Y. Wang, N. C. MacDonald, D. Hogue, J. J. Komiak, S. J. Lichwalla, R. E. Leoni, III., and J. R. Shealy, "AlGaIn/GaN High Electron Mobility Transistors on Si(111) Substrates," IEEE Transactions on Electron Devices, Vol. 48, No. 3, pp. 420-426, 2001.
- [128] A. Jarndal, A. Z. Markos, and G. Kompa, "Improved Modeling of GaN HEMTs on Si Substrate for Design of RF Power Amplifiers " IEEE Transactions on Microwave Theory and Techniques, Vol. 59, No. 3, pp. 644-651, 2011.

- [129] L. Dunleavy, C. Baylis, W. Curtice, and R. Connick, "*Large-Signal Modelling and Comparison of AlGaIn/GaN HEMTs and SiC MESFETs*," IEEE Microwave Magazine, Vol. 11, No. 6, pp. 82-96, 2010.

This work presents a comprehensive modeling strategy for advanced large-size AlGaIn/GaN HEMTs. A 22-element equivalent circuit with 12 extrinsic elements, including 6 capacitances, serves as small-signal model and as basis for a large-signal model. Analysis of such capacitances leads to original equations, employed to form capacitance ratios.

Basic assumptions of existing parameter extractions for 22-element equivalent circuits are perfected:

A) Required capacitance ratios are evaluated with device's top-view images.

B) Influences of field plates and source air-bridges on these ratios are considered.

The large-signal model contains a gate charge's non-quasi-static model and a dispersive- I_{DS} model. The extrinsic-to-intrinsic voltage transformation needed to calculate non-quasi-static parameters from small-signal parameters is improved with a new description for the measurement's boundary bias points. All I_{DS} -model parameters, including time constants of charge-trapping and self-heating, are extracted using pulsed-DC IV and I_{DS} -transient measurements, highlighting the modeling strategy's empirical character.

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