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An Enhanced Quasi-Monolithic Integration Technology for Microwave and Millimeterwave Applications

Mojtaba Joodaki

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To my Parents

for their love and kindness

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Mojtaba Joodaki

Contents

Abstract

RF/Microwave technology is shifting from large centralized and long range systems (with a large RF transmit power) to smaller distributed and shorter range systems (with relatively modest RF power) and also many new smaller systems must be mobile or hand-held. Trend in RF design is to shift from premium devices to more affordable and integrable technology, which gives a greater degree of RF functionality per unit volume.

In this way RF, microwave and millimeterwave packaging is becoming more and more important considering the significant growth of commercial and military applications in wireless communication and sensing. Huge changes are underway in wireless communications and consumer electronics. Excellent representations of these are handheld devices that have real-time Internet access, video, voice and sensing capability.

Packaging strongly affects performance, cost, reliability and lifetime and it is a determining factor in the growth of these applications. Generally, wireless subsystems consist of different components such as high frequency transceivers, digital processors and may include microelectromechanical systems (MEMS). Microwave transceivers are composed of both integrated circuits (ICs) and passive devices including filters and power combiners that are not integrated on the semiconductor substrate. These components are based on different materials and technologies.

On the other hand, in the past decades, there have been tremendous improvements in fabrication and characteristics of electronic devices and MEMS, and many new components have been invented. The development of III-V compound semiconductors such as GaAs, InP, and related ternary compounds has permitted microwave and millimeterwave devices with excellent noise and power performance to be developed. The progress has been rapid due to advances in both fabrication technology and materials. Today, RF performance of field-effect transistors extends well into the millimeterwave region, and frequency response greater than 300 GHz has been reported for the InP-based compound semiconductor HEMT. RF micromachining and MEMS have been identified as a technology that has the potential to make a major impact on existing RF architectures in sensors (radar) and communications by reducing weight, cost, size and power dissipation.

Thus, the necessary technologies are now mature and available, opening a wide field of deployment areas. These have provided us with many high performance components, which should be integrated and packaged without hindering their performance. All of these advanced features confirm required shifts in microwave packaging to address integration of a system-on-a-package (SOP).

The multilayer organic multi chip module (MCM) is a potential candidate for integration an SOP at microwave and millimeterwave frequencies. This technology has been utilized to package high-speed memory ICs and transceivers for communications, and packaging of MEMS devices in this technology has been recently demonstrated.

In this dissertation two different structures for earlier concept of quasi-monolithic integration technology (QMIT) have been introduced and along with the standard structure of QMIT, proposed by Wasige [122], have been investigated in details and further required developments have been addressed. To fulfill these requirements and reach a flexible technology owning several advantages, two new fabrication processes for QMIT named the enhanced QMIT for the coplanar and microstrip circuit realizations have been introduced. The enhanced QMIT can be considered as an organic deposited MCM, which uses common thin-film interconnection for the first level of packaging (device-to-package) for RF, microwave and millimeterwave applications.

In the enhanced QMIT large-area high-Q passive elements can be fabricated on a low cost silicon substrate covered by organic multiplayer dielectrics. Beside many other advantages such as small size and weight, good lifetime and reliability, capability of MCM integration, using active devices based on different materials, good control of parasitic elements, compatibility with coplanar waveguides without using thin devices and broad-band performance, the extremely low thermal resistance and direct electrical interconnects to the embedded active devices giving minimum parasitic effects, are unique advantages of this technology.

The body of this dissertation contains six chapters followed by a chapter of conclusion. In the first chapter after introduction to RF and microwave packaging and determining the position of the enhanced QMIT, the earlier concept of QMIT and its shortcomings are described. In the chapter 2, technological issues and material properties are discussed.

Chapter 3 covers the novel fabrication process, electrical characteristics of the embedded active devices in this technology and advantages of the new technology. The new technology not only fulfils the requirements for high frequency design, but also is cost effective, reliable and reproducible. Two fabrication processes for coplanar and microstrip realizations are introduced. To confirm the fabrication processes, a low noise Ka-band GaAs-based AFP02N3 p-HEMT and a power GaAs-based AFM08P2 MESFET from Alpha Industries were successfully integrated into a silicon substrate and the microwave characteristics of the low noise p-HEMT measured up to 40 GHz using an HP 8510B network analyzer.

To optimize the new structure and material properties, investigate the reliability and lifetime of the packaging and achieve an accurate model for the active devices in this technology, the thermal and thermo-mechanical stress simulations and measurements in

the earlier concept and enhanced QMIT and neural modeling of microwave active devices in the enhanced QMIT were performed in detail in chapters 4, 5 and 6, respectively.

To confirm the thermal simulation results and the transistor model used in chapter 4, the first successful application of a thermal nano-probe integrated into a piezoresistive atomic force microscopy (AFM) cantilever for two-dimensional thermal imaging of microwave active devices has been presented. Near-field, infrared measurement and nonlinear three-dimensional simulation have been performed for a KT1305T power UHF-band GaAs-MESFET of from OKI Electronic Components. The simulation and measurements confirm the high capability of the thermal nano-probe for these applications.

A novel method to achieve the thermo-mechanical stress distribution under different temperatures for the different QMIT structures has been discussed. A closed-loop temperature measurement system consisting of a Pt-100 temperature sensor, a Peltier-element and a digitally controlled current source implemented allowing temperature measurements with a resolution of better than 0.1 °C. The surface profiles on the silicon substrate around the active devices have been measured using scanning probe microscopy (SPM), DEKTAK or white-light interferometery. Great agreement between calculated and measured results was demonstrated. In comparison with the earlier concept, the simulation results confirm an excellent thermal resistance and a much lower induced thermo-mechanical stress for the enhanced QMIT.

Further, as a first attempt to the modeling of high frequency active devices in the QMIT environment, a systematic approach is presented to achieve a reliable neural model for microwave active devices with a different number of training data used for training the neural network. The method is implemented for a small-signal bias dependent modeling of p-HEMT (AFP02N3 from Alpha Industries) in two different environments: on a standard test-fixture and in the enhanced QMIT. The errors for different number of training data have been compared and show that by using this method a reliable model is achievable even though the number of training data is considerably small. The method aims at constructing a model, which can satisfy the criteria of minimum training error, maximum smoothness and simplest neural network structure.

Zusammenfassung

Trends in der heutigen Mikrowellentechnik sind dadurch gekennzeichnet, daß große zentral gelegene und weitreichende Systeme (mit einer hohen Sendeleistung) durch kleinere verteilte Nahbereichssysteme (mit relativ geringen Hochfrequenzleistungen) ersetzt werden. Weiterhin müssen diese kleineren Einheiten vielfach mobil und handgerecht sein. Die Entwicklung erfordert im allgemeinen eine Steigerung der Leistungsfähigkeit der erforderlichen Bauelemente und eine Integrationstechnologie, die einen höheren Grad an Funktionalität pro Volumeneinheit ermöglicht**.**

In diesem Zusammenhang erlangt das Packaging von Mikrowellen- und Millimeterwellen-Bauelementen und Schaltkreisen wachsende Bedeutung für kommerzielle und militärische Anwendungen in Bereichen der Funkübertragung und Hochfrequenzsensorik. Große Fortschritte werden heutzutage in der drahtlosen Kommunikationstechnik und im Bereich der Konsumerelektronik sichtbar. Wichtige Beispiele hierfür sind Handgeräte, die einen Echtzeit-Internetzugang haben, Video- und Tonübertragung ermöglichen und sensorische Fähigkeiten aufweisen.

Das Packaging beeinflusst insbesondere Leistung, Kosten, Zuverlässigkeit und Lebensdauer, und ist somit ein entscheidender Faktor in der Entwicklung dieser Geräte. Normalerweise bestehen drahtlose Übertragungssysteme aus verschiedenen Elementen wie z.B. einer Sende-/Empfangseinheit, Digitalprozessoren und gegebenenfalls auch mikroelecktromechanishe Systems (MEMS). Mikrowellen-Sende-/Empfangseinheiten bestehen aus integrierten Schaltungen (ICs) und passiven Elementen (u.a. Filter und Leistungsteiler), die nicht auf dem Substrat integriert sind. Diese Komponenten bestehen aus verschiedenen Materialien und Technologien.

Weiterhin wurde in der letzten Dekade ein bedeutender Fortschritt in der Herstellung und Charakterisierung von elektronischen Bauelementen und MEMS erzielt, und viele neue Komponenten eingeführt. Durch die Entwicklung von III-V Halbleitern wie z.B. GaAs, InP und entsprechende ternäre Halbleitermaterialien wurden Mikrowellen- und Millimeterwellenbauelemente mit exzellenten Rausch- und Leistungseigenschaften entwickelt. Diese raschen Forschritte basieren auf der Entwicklung neuer Herstellungstechniken und Materialien. Heute erzielen Feldeffekttransistoren beträchtliche Hochfrequenzleistungen im Millimeterwellenbereich; es konnte mit einem InP-basierten HEMT eine Frequenzantwort oberhalb von 300 GHz erzielt werden. Hochfrequenz-Mikromechanik (RF micromachining) und MEMS werden als Technologien erachtet, die in sich das Potenzial tragen, einen maßgeblichen Einfluss auf bestehende Hochfrequenz-Architekturen im Bereich der Sensorik (Radar) und Kommunikationstechnik durch Reduzierung von Gewicht, Kosten, Größe und Verlustleistung auszuüben.

Die notwendigen Technologien sind nun entwickelt und verfügbar, und öffnen somit ein weites Feld von Anwendungsgebieten. Sie haben uns zahlreiche leistungsfähige Komponenten zur Verfügung gestellt: Diese sollten dann ohne Einbuße hinsichtlich ihrer Leistungsdaten integriert und gehäust werden können. All diese fortschrittlichen Aspekte führen zu einer neuen Sichtweise des Mikrowellen-Packaging, nämlich der Realisierung eines Systems in einem Gehäuse (system-on-a-package (SOP)).

Die Technologie der organischen Mehrschicht-Multichip-Module (MCM) ist eine potentielle Möglichkeit, eine SOP-Komponente bei Mikrowellen- und Millimeterwellenfrequenzen herzustellen. Die Technologie wurde verwendet, um Hochgeschwindigkeitsspeicher-ICs und Transceiver für Kommunikationszwecke aufzubauen sowie MEMS zu integrieren.

In der vorliegenden Dissertation werden zwei verschiedene Strukturen nach dem herkömmlichen Konzept der quasi-monolithischen Integrationstechnologie (QMIT) vorgestellt und zusammen mit der QMIT-Standardstruktur von Wasige [122] im Detail untersucht und weitere erforderliche Verbesserungen durchgeführt. Um diese Erfordernisse zu erfüllen und eine flexible Technologie mit besonderen Vorteilen zu realisieren, wurden neue verbesserte QMIT-Herstellungstechniken für Schaltkreisrealiserungen in Koplanar- and Mikrostreifenleitungstechnik verfolgt. QMIT kann als organisches abgeschiedenes MCM angesehen werden, welches Dünnfilm-Verbindungen für das erste Niveau des Packaging verwendet.

Mit dem verbesserten QMIT-Prozeß können großflächige Elemente hoher Güte auf preisgünstigem Siliziumsubstrat hergestellt werden, die mit organischem Dielektrikum bedeckt werden. Neben anderen Vorteilen wie Größe, Gewicht, hohe Lebensdauer, Zuverlässigkeit, Fähigkeit der MCM-Integration, Verwendbarkeit aktiver Elemente aus verschiedenen Materialien, gute Kontrolle über die parasitären Elemente, Kompatibilität zu Koplanarleitungen ohne Verwendung von Dünnfilm-Bauelementen sowie ihre Breitbandeigenschaft, ihr extrem niedriger thermischer Widerstand und die direkten induktionsarmen elektrischen Verbindungen zu den eingebetteten aktiven Bauelementen, dies alles sind eindeutige Vorteile dieser Technologie.

Die Abhandlung dieser Dissertation enthält sechs Kapitel, gefolgt von einem zusammenfassenden Kapitel. Im ersten Kapitel werden nach einer Einführung des Packaging im Hochfrequenz- und Mikrowellenbereich die Begriffe des verbesserten und herkömmlichen QMIT-Konzepts erläutert und ihre Nachteile beschrieben.

Kapitel 3 befasst sich mit dem neuen Herstellungsprozess, den elektrischen Eigenschaften der eingebetteten aktiven Bausteine in dieser Technologie, sowie den Vorteilen der neuen Technologie. Die neue Technologie erfüllt nicht nur die Anforderungen für hochfrequenztaugliches Design, sondern ist auch kostengünstig,

zuverlässig und reproduzierbar. Zwei Herstellungsprozesse für Koplanar- und Mikrostreifenleitungstechnik werden vorgestellt. Um die Herstellungsprozesse zu verifizieren, wird ein rauscharmer Mikrowellentransistor für das Ka-Band (GaAs AFP02Ne p-HEMT) und ein GaAs-MESFET-Leistungstransistor vom Typ AFM08P2 von Alpha Industries in ein Siliziumsubstrat integriert und die Mikrowelleneigenschaften des rauscharmen p-HEMTs bis 40 GHz mit einem HP 8510B Netzwerkanalysator gemessen.

Um die neuen Strukturen und die Materialeigenschaften zu optimieren, wurde die Zuverlässigkeit und die Lebensdauer des Packaging untersucht und ein genaues Modell des aktiven Bauelements in dieser Technologie erstellt. Thermische und Thermospannungssimulationen und Messungen wurden für eingebettete Chips nach dem verbesserten und herkömmlichen QMIT-Konzept durchgeführt und ein neuronales Modell des aktiven Mikrowellenbausteins für die verbesserte QMIT-Umgebung erstellt, was in den Kapiteln 4,5 und 6 beschrieben wird.

Zur Bestätigung der thermischen Simulationsresultate und des Transistormodells in Kapitel 4, wurde erstmals eine thermische Nanosonde erfolgreich verwendet. Diese war in den piezoresistiven Cantilever eines Atomkraftmikroskops (AFM) integriert und ermöglichte eine zweidimensionale thermisches Abtastung von aktiven Mikrowellenbauelementen. Nahfeld- und Infrarotmessungen sowie eine nichtlineare dreidimensionale Simulation wurde für einen UHF GaAs Leistungs-MESFET vom Typ KT1305T von OKI Electronic Components durchgeführt. Die Simulationen und Messungen bestätigen die vielversprechende Leistungsfähigkeit solcher thermischen Nanoproben für diese Anwendungen.

Eine neue Methode, die thermomechanische Spannungsverteilung bei verschiedenen Temperaturen zu erhalten, wurde diskutiert. Ein geschlossenes Temperaturmesssystem, bestehend aus einem Pt-100 Temperatursensor, einem Peltier-Element und einer digital kontrollierten Stromquelle, erlaubt Temperaturmessungen mit einer Auflösung von besser als 0,1 ^{o}C. Die Oberflächenprofile auf dem Siliziumsubstrat in der Umgebung des aktiven Elements wurden mit Hilfe von Abtastmikroskopie (SPM), DEKTAK oder Weißlicht-Interferometrie gemessen. Es konnte eine grosse Übereinstimmung zwischen berechneten und gemessenen Resultaten erzielt werden. Im Vergleich mit dem herkömmlichen QMIT-Konzept bestätigen die Simulationsergebnisse einen exzellenten thermischen Widerstand und eine stark verringerte thermomechanische Spannung für das verbesserte QMIT-Konzept.

Weiterhin wird erstmalig ein Ansatz vorgestellt, einen Hochfrequenztransistor in einer QMIT-Umgebung zu modellieren. Der systematische Ansatz führt zu einem zuverlässigen neuronalen Modell für aktive Mikrowellenelemente unter Verwendung einer unterschiedlichen Anzahl von Trainingsdaten zum Training des neuronalen

Netwerks. Die Methode wird für die Herleitung eines arbeitspunktabhängigen Kleinsignalmodells eines p-HEMTs (AFP02N3 von Alpha Industries) in zwei unterschiedlichen Umgebungen verwendet: in einer Standard-Testfixture und in der verbesserten QMIT-Einbettungssituation. Die Fehler bei einer unterschiedlichen Anzahl von Trainingsdaten sind gering und zeigen, dass diese Methode ein verlässliches Modell liefert, sogar dann, wenn die Anzahl der Trainingsdaten vergleichsweise gering ist. Diese Methode zielt darauf ab, ein Modell zu generieren, welches Kriterien wie minimalen Trainingsfehler, optimales Fitting der Kurven und eine einfache neuronale Netzwerkstruktur erfüllt.

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Frequently used nomenclatures

Symbol	*Meaning*	*Unit*
α	Penalty factor	-
β_l	The smoothing factor in layer l	-
ΔE_c	Conduction band discontinuity	eV
ΔE_H	Band gap energy change related to hydrostatic strain	eV
ΔE_S	Band gap energy change related to shear strain	eV
$\Delta w_{pq,l}(n+1)$	The change of weights between adjacent layers	-
$\delta_{q,l}$	The error term of neuron q between target and actual outputs of layer l	-
ε_{AlGaAs}	Dielectric constant of doped AlGaAs	-
ε	Strain	-
ε_r	Dielectric constant	-
ε_{rad}	Emissivity	-
$\varepsilon_{radsolid}$	Emissivity of solid	-
$\varepsilon_{r\sim GaAs}$	Dielectric constant of GaAs	-
$\varepsilon_{r\sim GaAs0}$	Dielectric constant of GaAs at 300 K	-
ϕ_b	Schottky barrier energy	eV
Γ	Direct band in GaAs	-
Γ_q *or* Γ_T	Represent a surface	m^2
η	Learning rate	-
η_l	The learning rate in layer l	-
$\lambda(t)$	Instantaneous failure rate	s^{-1}
ν	Poisson's ratio	-
θ, ϕ, ψ	Euler's angles	degree
ρ	Density	kgm^{-3}
ρ_c	Conduction band density of states	cm^{-3}
σ	Normal stress	MPa
σ_0^2	Error variance	-
σ_F	Fracture strength	MPa
σ_{SB}	Stefan-Boltzmann's constant (5.669E-8)	$Wm^{-2}K^{-4}$
τ	Shear stress	MPa
τ_e	Energy relaxation time	ns
τ_m	Momentum relaxation time	ns

Ω	Represents a domain	m^3
A	Area	m^2
AFM	Atomic force microscopy	-
Ag	Silver	-
Al	Aluminum	-
AlN	Aluminum nitride	-
ANN	Artificial neural network	-
Au	Gold	-
BCB	Benzocyclobutene	-
BeO	Beryllium oxide or beryllia	-
BiCMOS	Bipolar-complementary metal oxide semiconductor	-
c	Specific heat	
C	Compliance coefficient	GPa
CAD	Computer aided design	-
C_i	Correlation of the normalized drain and gate noise currents	-
CMP	Chemical mechanical polishing	-
CPW	Coplanar waveguide	-
Cr	Chromium	-
Cu	Copper	-
CVD	Chemical vapor deposition	-
d	Thickness of AlGaAs layer	nm
DEKTAK	A type mechanical nano-meter surface profiler	-
DOE	Design of experiment	-
DT	Temperature difference	K
E	Energy	J or eV
F_e	Electric field	V/m
$\hat{E}$	Elastic modulus (Young's mogulus)	GPa
E_a	Activation energy	eV
$E_{a\sim dev}$	Device activation energy	eV
EBP	Error back propagation	-
E_c	Conduction band	eV
E_D	Energy level of deep traps	eV
E_F	Fermi-level	eV
EF	Error function	-
E_{FO}	Fermi-level for electrons in AlGaAs layer at equilibrium	eV
E_g	Energy gap	eV
$E_{g\sim GaAs}$	GaAs energy gap	eV
EM	Electromagnetic	-

f	Frequency	GHz
$F(t)$	The probability that a system fails in [0, t]	-
$f_c(E)$	Fermi-Dirac distribution function	-
FDTD	Finite-difference time-domain	-
FEM	Finite-element method	-
FET	Field effect transistor	-
FIT	Failure in time	10^{-9}hour^{-1}
$f_p(t)$	The probability of failure around a point in time t	-
FR-4	An epoxy-glass with self-extinguishing resin system	-
f_s	Sigmoid function	-
f_T	Cutoff frequency	GHz
g	Degeneracy factor of the deep donor level	-
GaAs	Gallium arsenide	-
GaN	Gallium nitride	-
g_{NN}	Equivalent to the NN function	-
g_s	Equivalent to the NN function	-
H	Heat transfer coefficient	Wm^{-2}K^{-1}
h ($\hbar = h/2\pi$)	Plank's constant (6.62617E-34)	Js
HBT	Heterojunction bipolar transistor	-
HEMT	High electron-mobility transistor	-
HFSS	High frequency structure simulator	-
HTCC	High temperature cofired ceramic	-
ICs	Integrated circuits	-
I_d (I_{ds})	Drain current	mA
ILD	Interlayer dielectric	-
i_{nd}	Normalized drain noise current	-
i_{ng}	Normalized gate noise current	-
InP	Indium phosphide	-
k	Thermal conductivity	Wm^{-1}K^{-1}
k_B	Boltzmann's constant (8.617E-6)	eV/K
k_{epoxy}	Thermal conductivity of epoxy	Wm^{-1}K^{-1}
K_{lc}	Fracture toughness	MPam$^{1/2}$
k_n	The number of coefficients in a network	-
KOH	Potassium hydroxide	-
l_1, l_2, l_3	The direction cosines	-
l_c	Defect length	-
LOR	Lift-off resist	-
LPCVD	Low pressure chemical vapor deposition	-
l_r	Defect radius	nm

LTCC	Low temperature cofired ceramic	-
m_n^{Γ}	Electron's effective mass in the Γ band of GaAs	kg
M_{Γ}, M_{L}, M_{L}	Numbers of the equivalent minima in the Γ, L and X bands	-
m^*	Effective mass	kg
m^*_n	Electron's effective mass	kg
m^*_p	Hole's effective mass	kg
m_1, m_2, m_3	The direction cosines	-
MCM	Multichip module	-
MCM-C	Ceramic multichip module	-
MCM-D	Deposited multichip module	-
MCM-L	Laminated multichip module	-
MEMS	Microelectromechanical systems	-
MESFET	Metal semiconductor field effect transistor	-
MIM	Metal insulator metal	-
m_n^L	Electron's effective mass in the L band of GaAs	kg
MLP	Multilayer perceptrons	-
MMIC	Microwave monolithic integrated circuit	-
MoM	Method of momentum	-
MOS	Metal oxide semiconductor	-
MPSE	Modified prediction squared error	-
$\mathrm{MPSE}_{\mathrm{min}}$	Minimum modified prediction squared error	-
MTTF	Mean time to failure	-
$\mathrm{MTTF}_{\mathrm{ref}}$	Mean time to failure at a specific reference temperature	hour
m_n^X	Electron's effective mass in the X band of GaAs	kg
N	Available number of measured data for training the neural network	-
$\vec{n}$	Normal vector to a boundary	m
N_d^+	Total ionized donor density	cm^{-3}
N_d	Density of the shallow donors	cm^{-3}
N_{dT}	Density of deep traps	cm^{-3}
n_e	Electron density	cm^{-3}
N_i	Number of neuron inputs	-
n_i	Intrinsic carrier density	cm^{-3}
N_L	Number of hidden layer neurons	-
N_M	Number of output neurons	-
$O_{p,l}$	The actual output of neuron p in layer l	-
p	Neural potential	-
P{a}	The probability that the event *'a'* will occur	-

PDF	Probability density function	-
PDS	Product design specification	-
PECVD	Plasma enhanced chemical vapor deposition	-
p-HEMT	Pseudomorphic high electron-mobility transistor	-
PR	Positive resist	-
Pt	Platinum	-
PTFE	Polytetrafluorethylene	-
q	Electronic charge	Q
Q	Rate of heat flow	W
$\overline{q}$	Heat flux	Wm^{-2}
Q2D	Quasi-2-dimensional	-
$R(\Delta t \mid t)$	The conditional reliability of a system of age t	-
$R(t)$	The probability that a system survives until time t	-
RF	Radio frequency	GHz
RFIC	Radio frequency integrated circuit	-
RIE	Reactive ion etch	-
r_r	Reaction rate	$moles/m^2s$
$r_{r\sim ref}$	Reaction rate at a reference temperature	$moles/m^2s$
S	Output of the neuron (the state)	-
SEM	Scanning electron microscopy	-
S_i^H	The states of the hidden neurons	-
S_i	Input of neural networks	-
Si	Silicon	-
SiC	Silicon carbide	-
SiGe	Silicon germanium	-
SiLK	A commercial spin-on aromatic hydrocarbon polymer	-
SiO_2	Silicon dioxide	-
SOP (SIP)	System on a package (system in a package)	-
SPM	Scanning probe microscopy	-
SU8	An epoxy based negative photoresist	-
t	Time	s
T	Temperature	K
TAB	Tape automatic bonding	-
T_{device}	Device temperature	K
T_e	Electron temperature	K
Teflon AF	A kind of amorphous copolymers from Dupont	-
t_f	Time to failure	hour
T_f	Temperature of fluid	K
T_g	Glass temperature	K

Ti	Titanium	-
t_{infant}	Infant lifetime	hour
$t_{operation}$	Operation lifetime	hour
T_{room}	Room temperature	K
T_s	Temperature of solid	K
TSE	Training squared error	-
t_{useful}	Useful lifetime	hour
$\vec{u}$	Velocity field	ms^{-1}
UHF	Ultra high frequency	-
V_1	Light-hole band	eV
V_2	Heavy-hole band	eV
VCO	Voltage controlled oscillator	-
V_{ds}	Drain-source voltage	V
V_{gs}	Gate-source voltage	V
v_n	Electron velocity	m/s
V_{th}	Threshold voltage	V
w	Represents weights in neural networks	-
W_g	The distance between active device and silicon sidewalls	μm
w_i^H	Weights form hidden layer to output	-
w_{im}^H	Weights form input to hidden layer	-
w_i	Connection weights in neural networks	-
$\hat{w}_i^I$, $\hat{w}_m^H$	Offset or bias weights	-
$w_{pq,l}(n)$	The weight from neuron p in layer l to neuron q in layer (l+1) at step n	-
X	Indirect band in GaAs	-
$x^{(r)}$	Input training data	-
$\bar{y}$	Mean value of all the experimental data	-
$y^{(r)}$	Output training data	-
Y_g	Dimensionless parameter that depends on the geometry of the flaw	-
y_i	The ith target of the output node	-
$\hat{y}_i$	The ith output of output node	-
$\hat{y}_{i,j}$	The jth estimated output of the ith experiment	-
$y_{i,j}$	The jth measured output of the ith experiment (target)	-

Chapter 1

Introduction

RF, microwave and millimeterwave packaging is becoming more and more important due to the significant growth of commercial and military applications in wireless communication and sensing. Huge changes are underway in wireless communications and consumer electronics. Excellent representations of these are handheld devices that have real-time Internet access, video, voice and sensing capability. Packaging strongly affects performance, cost, reliability and lifetime and it is a determining factor in the growth of these applications. Generally, wireless subsystems consist of different component such as high frequency transceivers, digital processors and may include microelectromechanical systems (MEMS). Microwave transceivers are composed of both integrated circuits (ICs) and passive devices including filters and power combiners that are not integrated on the semiconductor substrate. These components are based on different materials and technologies [13], [16], [26], [62], [78], [88], [89].

On the other hand, in the past decades, there has been tremendous improvements in fabrication and characteristics of electronic devices and MEMS, and many new components have been invented [16], [62], [85]. The development of III-V compound semiconductors such as GaAs, InP, and related ternary compounds has permitted microwave and millimeterwave devices with excellent noise and power performance to be developed. The progress has been rapid due to advances in both fabrication technology and materials. Today, RF performance of field-effect transistors extends well into the millimeterwave region, and frequency response greater than 300 GHz has been reported for the InP-based compound semiconductor high electron-mobility transistor (HEMT) [26].

Recently research groups at Cornell University and University of California at Santa Barbara both fabricated GaN transistors capable of sustaining power densities above 10 W/mm of gate width, while amplifying signals at 10 GHz. For comparison, ordinary silicon-based transistors can efficiently amplify signals only up to 2-3 GHz. As for silicon carbide, experimental devices at Cree Inc. (Durham, N.C.) recently achieved 7.2 W/mm, but at frequencies not higher than 3.5 GHz. GaAs-based transistors can handle 10 GHz but withstand a power density of less than 1 W/mm at that frequency [64], [81], [125]. Such a high power application requires a proper low thermal resistance packaging, which is comparatively much cheaper than pure monolithic GaN-based circuits.

SiGe-based BiCMOS technology has become a key technology for radio frequency integrated circuit (RFIC) design as evidenced by product and technology announcements from several companies. In this technology, an f_T of 50 GHz is currently typical and f_T's of 100 GHz are beginning to appear [10]. Compared to GaAs technologies, SiGe HBTs have several favorable attributes. For example, the minimum noise figures are close to those of a 0.5 μm MESFET technology and better than those of the GaAs HBT technology [27]. The low noise frequency corner in SiGe HBTs make them an excellent technology choice for VCOs and power amplifiers, in addition to allowing very complex custom designs using mixed signal methodology [94], [96].

RF micromachining and MEMS have been identified as a technology that has the potential to make a major impact on existing RF architectures in sensors (radar) and communication by reducing weight, cost, size and power dissipation [17], [29], [62], [88], [96].

Thus, the necessary technologies are now mature and available, opening a wide field of deployment areas. These have provided us with many high performance components, which should be integrated and packaged without hindering their performance. All of these advanced features confirm required shifts in microwave packaging to address integration of a system-on-a-package (SOP) [13], [16], [80], [88], [89].

The multilayer organic multichip module (MCM) is a potential candidate for integration an SOP at microwave and millimeterwave frequencies. This technology has been utilized to package high-speed memory ICs and transceiver for communications and packaging of MEMS devices in this technology has been recently demonstrated [5], [88].

The new generation quasi-monolithic integration technology (QMIT) can be considered as an organic deposited multi chip module (MCM-D), which uses common thin-film interconnection for the first level of packaging (device-to-package) for RF, microwave and millimeterwave applications.

In this technology large-area high-Q passive elements can be fabricated on a low cost silicon substrate covered by organic multiplayer dielectrics. Beside many other

advantages such as small size and weight, good lifetime and reliability, capability of MCM integration, using active devices based on different materials, good control of parasitic elements, compatibility with coplanar waveguides without using thin devices and broad-band performance, the extremely low thermal resistance and direct electrical interconnects to the embedded active devices giving minimum parasitic effects, are unique advantages of this technology.

Although wire bonding occupies major part of the market, flip-chip frequently has been utilized for microwave and millimeterwave designs. Low cost, high-density, and short transition interconnects are considered to be the main advantages of the flip-chip technique [6], [37], [73], [134]. This assembly is well known for its difficulty in removing heat from the chip and a thermal bump has been introduced to help removing heat [24]. Thermal expansion coefficient mismatching of materials involved in this technology is another issue on which many attempts have been made to [84]. Although in comparison with wire bonding the short electrical interconnect (bumps heights of 20 to 100 μm) is a great advantage of this technology, in comparison to the new generation QMIT, which provides direct interconnect to the active devices, is a disadvantage.

After several years of research and struggling in department of High Frequency Engineering headed by Prof. Dr.-Ing. G. Kompa with cooperation of departments of Technological Electronics headed by Prof. Dr. H. Hillmer and Technological Physics headed by Prof. Dr. R. Kassing at University of Kassel, the new generation QMIT is a promising low-cost high-performance organic MCM-D RF packaging, which can be potentially used for integrating an SOP [50]-[61], [68], [70], [119]-[122].

In next section, RF and microwave packaging will be discussed shortly and position of the new generation QMIT will be determined. The earlier concept of QMIT and its different structures are introduced in section 1.2. Section 1.3 covers a brief of research objectives in this dissertation.

1.1 RF and microwave packaging and position of the enhanced QMIT

In a typical microwave and millimeterwave system, signals are generated by an oscillator and transmitted from an antenna driven by an amplifier. The signals are received by another antenna and propagated to a receiver. There are many transmission line components to interconnect theses basic devices. In many cases, the transmission line is a part of the circuits. The trend is to integrate all the devices and components more and more using microwave monolithic integrated circuits (MMICs) and advanced packaging technologies. High integration could eliminate layers of interconnects for cost reduction

and performance enhancement [23], [35]. An RF package could be in the form of a single-chip or an MCM. A summary of different forms of packaging is introduced below.

1.1.1 Single-chip packaging

In a single-chip package, an RF device is connected to a package substrate through wire bonding or flip-chip soldering/bonding. Usually there are lines on the substrate. The lines are connected to the external ports through feedthroughs or vias. The external ports are connected to the next level board assembly. There are many different packaging approaches such *metal wall package*, *ceramic wall package*, *glass ceramic package* and *plastic package* [131]. The kind of packaging will be determined according to RF performance and characteristics, thermal and mechanical aspects, size, weight, shape, test, validation and overall cost including assembly, rework as well as package manufacturability.

1.1.2 Multi chip module

MCM technologies are being applied to design and manufacture RF and microwave modules. In this technology there is substrate of dielectric and conduction layers, on which integrated circuits ("chip") and passive components are mounted directly on (or inside) the substrate, without separate packaging for most of active components. The whole of MCM may be placed in a hermetic package like a large single-chip package, or may be directly covered with a sealant material to protect the components from physical damage.

MCM technologies are emerging as a cost-effective technology for next-generation devices because of their advantages in small size, performance enhancement, better reliability, low power consumption, package cost reduction and potential overall cost reduction for high-volume applications. It is the predominant approach for millimeterwave modules with frequencies higher than 30 GHz [29], [44], [46], [89]. Different types of MCM are described below.

1.1.2.1 Laminate MCM

Laminate MCM's (MCM-L's) are manufactured through the lamination of sheet layers of organic dielectric, and are very similar to traditional printed circuit board technology; in fact, the dielectric layers and the interconnects are developed in much the same way as for laminated printed circuit boards. The line geometries and via diameters are typically half or less the size of those found in traditional circuit boards. These MCM's exhibit very low line losses up to relatively high frequencies because the lines are thick and wide; however, the vias are typically quite tall and also much wider than the lines, thus

causing substantial impedance discontinuities and wavefront reflections for frequency components above 500 MHz [21].

1.1.2.2 Ceramic MCM

Ceramic MCM's (MCM-C's) are manufactured by stacking unfired layers of ceramic dielectric (i.e., in their flexible, unfired state), onto which liquid metal lines are "silk screened" using a metal ink process. The individual inked layers are then aligned, pressed together, and "cofired" at 800 to 900 °C, or 1500 to 1600 °C (depending on the composition of the ceramic material) into a solid planar structure, onto which integrated circuits can be installed. These MCM's can, if fabricated with excellent dimensional tolerance control, exhibit low line losses for the same reasons as for the MCM-L's. Unfortunately, as will be discussed later, like the MCM-L's, their vias are also tall and wide, resulting in substantial impedance discontinuities and wavefront reflections for frequency components above 500 MHz [21].

1.1.2.3 Deposited MCM

Deposited MCM (MCM-D's) are manufactured through the deposition of organic or inorganic dielectrics onto a silicon or alumina support substrate. After each dielectric layer is deposited, one of several techniques is used to pattern metal lines as well as metal "vias" which penetrate the dielectric layers to connect adjacent metal layers. The chips are then installed on the upper surface, and attached electrically through wire bonds or other means such as tape automated bond structures, or even by mounting the chips face down on the surface, with metal balls serving as the electrical connections between the chip and matching pads on the MCM's. The MCM-D line cross sections are typically smaller than for MCM-C's or MCM-L's, resulting in higher resistive line losses; however, their via heights are typically quite small, and their via cross sections are equivalent to the line-widths, resulting in low levels of impedance discontinuity and wave-front reflections, in comparison to the MCM-L's and MCM-C's [21].

The new generation QMIT locates in this category of MCM's. In this technology chips are placed into wet-etched holes through the silicon substrate and fixed either by deposited amorphous-silicon or electroplated gold layer. A low ε_r spin-on organic dielectric layer used for planarization and substrate for copper interconnects. The technology perfectly handles fabrication of multilayer interconnects [50].

1.1.3 The first assembly technologies

The first level (device-to-package) assembly technologies are wire bonding, tape automated bonding (TAB) and flip-chip. The earlier concept and new generation of QMIT also belong to this group.

1.1.3.1 Wire bonding

Wire bonding technology is the earliest and by far the most prevalent technology (>90%) in use today. In a typical wire bonding process, a ball or wedge gold wire with 10 to 25 µm diameter bonded to gold-plated die and the substrate bond pads, Fig. 6-1. The very narrow wires are highly inductive at higher frequencies and variations in wire lengths and loop shapes cause different performance from module to module. Length and impedance control are critical issues [9], [15].

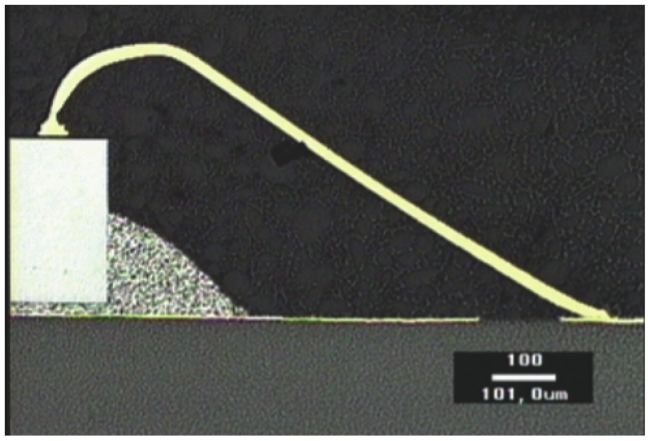


Figure 1-1: Cross-section of wire bond between die and substrate, the loop form [15].

1.1.3.2 Tape automated bonding

TAB technology is commonly used only in commercial product requiring lightweight and thin packaging. TAB is typically a reel-to-reel process using solid copper tape or copper prepatterned on a polyimide film. The inner leads of the tape are bumped and bonded to the die pads. Finally, the bonded assembly is encapsulated and the outer leads are bonded to a printed wiring board. The coplanar film carrier can be made for TAB RF packaging, which has an insertion loss of less than 0.2 dB/mm without resonance over the frequency range from dc to 30 GHz [79], [114].

1.1.3.3 Flip-chip

Flip-chip technology provides a direct metallurgical interconnect between die bond pads and the substrate. Solder-bumped die are soldered or bonded directly to the substrate, providing an excellent electrical connection, Fig. 6-2. The thermal path is through the solder connection to the substrate. In the case of high-power GaAs-MMICs, without the use of thermal bumps, this thermal path is usually inadequate for reliable operation [24]. Another issue is the thermal expansion coefficients mismatching of materials involved, which limits strongly the lifetime the packaging [84]. However, flip-chip assembly is becoming more and more important with several advantages such as automated assembly, compact modules, minimum interconnect length, low inductance and

discontinuity, compatibility with coplanar waveguide without the use of thin devices and acceptable thermal management with the use of thermal bumps.

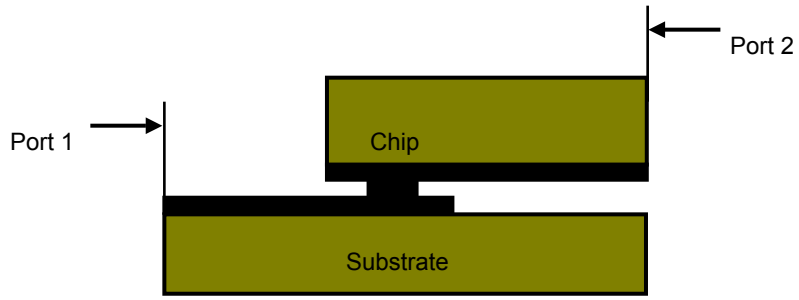


Figure 1-2: Side-view of the bump configuration in flip-chip technology.

1.2 The earlier concept of QMIT

1.2.1 General

Since RF/Microwave technology is shifting from large centralized and long range systems (with a large RF transmit power) to smaller distributed and shorter range systems (with relatively modest RF power) and also many new smaller systems must be mobile or hand-held, trend in RF design is to shift from premium devices to more affordable and integrable technology which gives a greater degree of RF functionality per unit volume.

The superiority of the III-V semiconductor compounds over silicon for high frequency semiconductor device fabrication due to their higher carrier mobility and lower parasitics, has been well known for many years [26]. During the last few years silicon micromachining has been greatly developed for realization of microwave and millimetrewave passive components [17], [94]. On the other hand, high cost and high thermal resistance of the standard MMICs and parasitics and non-reproducible wire bonding in the hybrid circuits demand a new approach for realization of high frequency circuits.To gain the advantages of silicon micromachining and III-V based active devices and to avoid the disadvantages of the standard hybrid and monolithic circuits, quasi-monolithic integration of III-V chips into the silicon substrate is of utmost importance.

The earlier concept of QMIT is an alternative to monolithic circuit fabrication of microwave and millimeterwave integrated circuits [68], [70], [122]. In this technology commercial devices such as microwave FETs are embedded in a micromachined low cost high resistivity silicon substrate on which the passive circuit is fabricated. Interconnects between the active devices and passive components are realized using thin-film technology [120]. The technology allows the fabrication of planar high frequency circuits, which exhibit advantages of both MMICs and hybrids. The use of micromachining and thin-film technology ensures fabrication of reproducible

interconnects with very low parasitic inductance and capacitance. Passive devices, which usually require large chip areas, are fabricated on a low cost silicon substrate.

The earlier concept of QMIT was introduced to alleviate the problems of pure MMICs and of the conventional hybrid circuits. In spite of several advantages such as:

- Using active devices based on different materials (Si, GaAs, InP, GaN...)
- Smaller size and weight than hybrid technology
- Better control of parasitic elements than hybrid technology
- Reproducible interconnections
- Broader frequency performance than hybrid technology
- Large area passive elements on a low cost Si-substrate
- Possible realization of high-Q passive element
- Possibility of batch processing
- Compatibility with coplanar interconnect without use of thin devices

and realization of a few circuits containing low power active devices in this technology [119], [121], the technology has suffered several shortcomings. The shortcomings are described in section 1.2.3.

1.2.2 The fabrication process and other possible structures

The whole of the earlier fabrication process of QMIT can be summarized in two parts, fabrication steps for embedding the GaAs-chips into the holes and fabrication steps up to creating the air bridges. Fig. 1-3 shows the fabrication steps for embedding the chips into the holes. At the first to mask the whole of Si-wafer from KOH etchant a 2 μm thickness of silicon dioxide has been created using thermal oxidation process. After etching the holes in the wafer, oxide is removed gently and chips are placed in the holes using an adhesive film. Then the gap between Si-sidewalls and chip should be filled out with the glue carefully. To fix the chips the glue is cooked according to the manufacturer's data sheet [18]. Fig. 1-4 covers the rest of the standard fabrication process of the earlier concept of QMIT. Fig. 1-4(a) illustrates the process step after the first gold metallization and spinning of the first layer of photoresist for lift off process. Then the second layer of photoresist spun, etched and smoothed using oxygen plasma etching. In the next step, Al is deposited by using a low temperature electron-beam evaporation process. After a normal process of photolithography the desired air-bridges are fabricated. Fig. 1-5 illustrates an embedded GaAs-FET in this technology with on-wafer probe compatible coplanar contacts.

Fig. 1-6(a) shows the final standard structure of earlier concept of QMIT. Fig. 1-6(b) and Fig. 1-6(c) depict the other possible structures of the earlier concept of QMIT using a full dry etching and a combination of dry etching and wet etching, respectively.

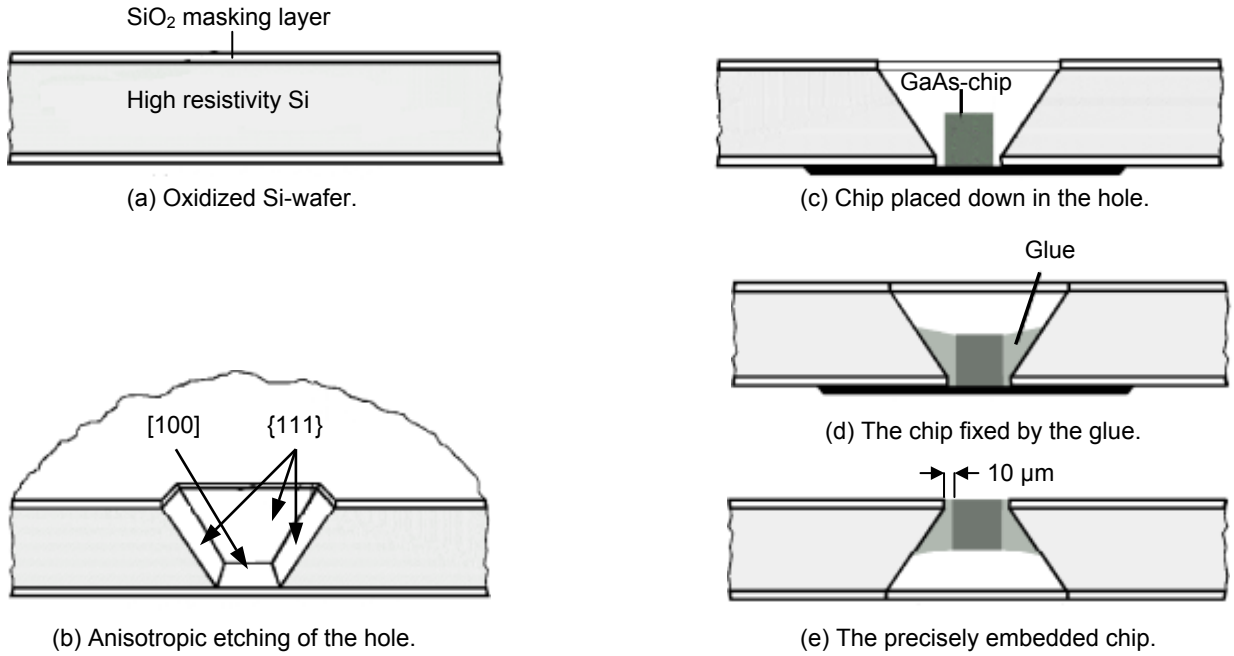


Figure 1-3: Fabrication process for embedding the chips into the wet-etched holes in Si-wafer.

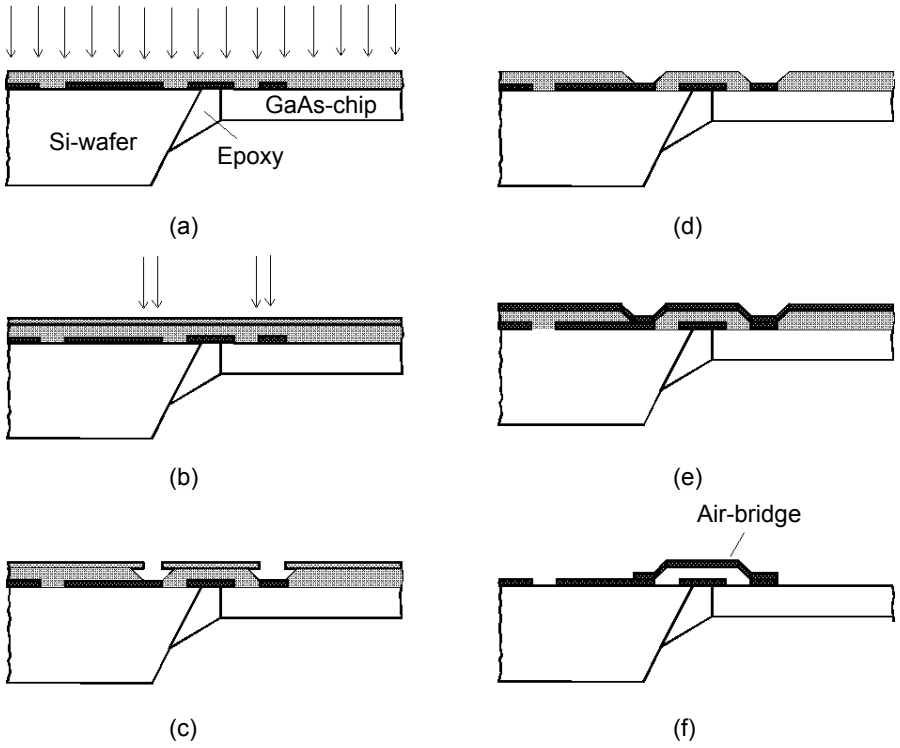


Figure 1-4: Fabrication process for the earlier concept of QMIT after embedding the chips in the holes.

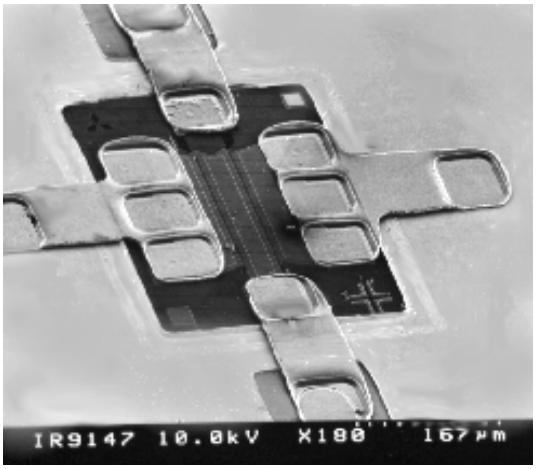
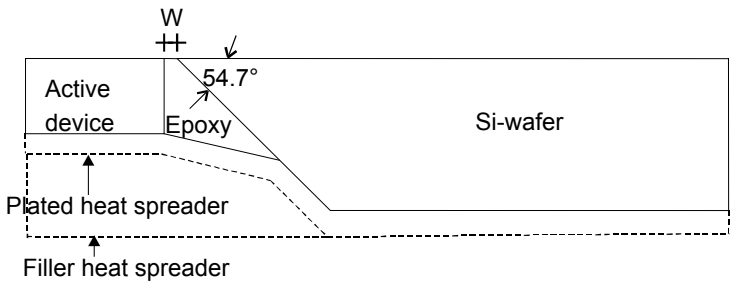
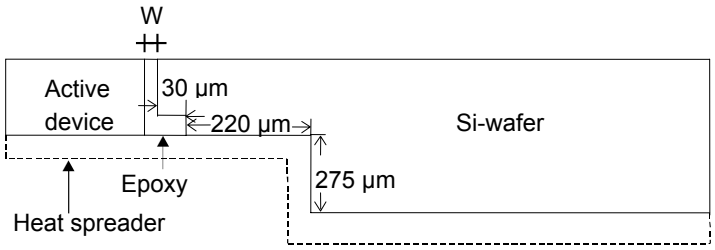


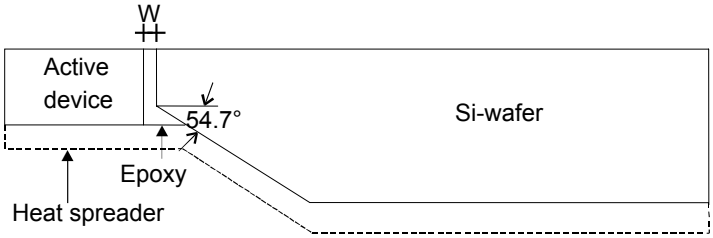
Figure 1-5: Fabricated microtest-fixture with on-wafer probe compatible coplanar contacts for accurate GaAs-FET characterization in the earlier concept of QMIT [122].



(a) The standard structure of the earlier concept of QMIT.



(b) The second structure of the earlier concept of QMIT.



(c) The third structure of the earlier concept of QMIT.

Figure 1-6: Three possible structures of the earlier concept of QMIT.

1.2.3 The attained state of the art and further requirements

Although a few circuits containing low power active devices have been realized [70], [119], the technology has suffered several shortcomings.

- The thermally conductive epoxy glue used to fix the GaAs-chips in the wet etched holes has a low glass temperature of 100 °C and a large expansion coefficient of 30E-6 K^{-1}. The low glass temperature limits the working environment temperature to values well below the 100 °C and restricts the fabrication process to a very low temperature process. This renders the realization of some passive elements such as MIM capacitors in this technology impossible.
- The large thermal expansion coefficient induces very high thermo-mechanical stress, which significantly decreases the lifetime of packaging [58].
- Considering the difficulties in removing the baked epoxy, cleaning it from the surface of the transistor or other parts was very difficult, if not impossible.
- Thermal conductivities of the available non-electrical conductive epoxies are not adequate for the power applications, so a thick gold electroplated backside heat spreader was suggested [52].
- On the other hand, defects occur during scribing of the chips by manufacturers. Some of these defects are in the form of protruding structures, which hinder the proper placement of the device in the etched holes.
- Proper realization of the air-bridges requires the gap between GaAs-chips and silicon side-walls to 10 and 20 μm. Considering a common 5% tolerance in the thickness of the silicon wafers from the same company, having hole dimensions using a standard silicon wet etching with this accuracy is a hard task.

To overcome the above-mentioned problems, a new fabrication process named “enhanced quasi-monolithic integration technology” is introduced in the chapter 3. The advantages, outlined in the chapter 3, of the new generation of QMIT over the earlier concept, considering the other common advantages of both technologies confirm it as an excellent alternative with unique advantages for microwave and millimeterwave monolithic integrated circuits.

1.3 Research objectives

To develop any new technology for fabrication of microwave and millimeterwave circuits, careful considerations must be paid that “the fabrication process not only should fulfill high frequency designs requirements but also should be cost effective, reliable, and reproducible”.

In this dissertation I seek to introduce a new fabrication process, which fulfils high frequency designs requirements and is cost effective, reliable and reproducible. Thus, in addition to the practical part of fabrication, to optimize the new structure and material properties and investigate the reliability and lifetime of the packaging and achieve an accurate model for the active devices in this technology, the research also consists of theoretical parts such as simulation, design and modeling. Different steps of the fabrication process should be selected taking into account the cost considerations and avoiding using expensive materials. Fabrication steps must be compatible with facilities in a standard clean room for semiconductor fabrications.

To investigate the packaging reliability of the new technology thermal and thermo-mechanical stress studies need to be performed deeply. In this part of the research, effects of several parameters of fabrication process, material properties and geometrical structure of the novel technology should be considered.

To have a reliable design in the new technology, characterization and modeling of the active and passive devices in the new environment are highly required. Although a complete solution needs much more research, as the first attempt to the problem, a neural based model for the high frequency active devices in the new generation QMIT has been constructed, which can be used for highly accurate, fast and flexible design. Fig. 1-7 shows the basic structure of the dissertation.

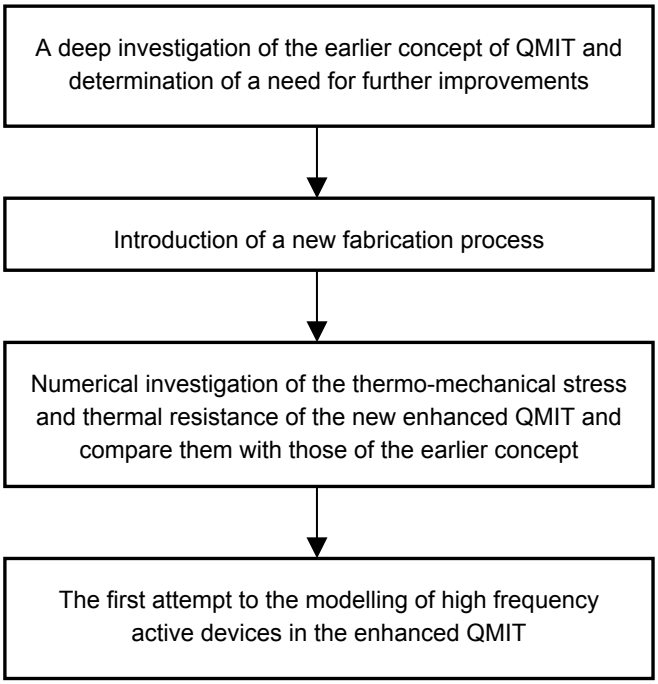


Figure 1-7: The structure of the dissertation.

1.3.1 Overview of the dissertation chapters

The body of this dissertation contains six chapters followed by a chapter of conclusion. In the chapter 2, technological issues and material properties are discussed. Chapter 3 dedicated to the novel fabrication process, electrical characteristics of the embedded active devices in this technology and advantages of the new technology. Chapter 4 covers the thermal analysis and management in the both the earlier concept and new generation of QMIT. The results have been compared and a great improvement in the thermal resistance is obtained. To confirm robustness of transistor thermal model used in the simulations and capability of the sensor for the specific applications, the first application of a novel thermal nano-probe for two-dimensional thermal mapping of the surface of a microwave GaAs-MESFET is demonstrated. Thermo-mechanical stress analysis and measurements and extremely improvement of the packaging lifetime are described in chapter 5. In the chapter 6, a new small-signal bias-dependent neural based model for a low noise GaAs-based p-HEMT in the new generation QMIT environment is developed, which is fast, flexible and accurate. Chapter 7 draws conclusions about the enhanced QMIT and proposes directions for the future researches.

Chapter 2

Technological Issues and Material Properties

2.1 Introduction

Two important issues in introducing any new technology are the selection of the proper materials and method of the fabrication. These directly affect product performance, cost and reliability. In the enhanced QMIT one is faced by a selection of two issues: substrate and interconnects.

Microstrip transmission line and coplanar waveguide are the most common forms of interconnect in the microwave and millimeterwave integrated circuit designs. Although microstrip transmission lines do not require air-bridges - to suppress the odd mode propagated electromagnetic wave at junctions and discontinuities - and have a lower resistance loss than coplanar wavegiudes and can handle higher power, in these last years researchers have shown a great deal of attention in coplanar waveguides for MMICs design due to many advantages compared with the conventional microstrip design. Coplanar waveguide has inherently low dispersion due to power transferring through the air and exhibits relatively small parasitic effects in discontinuities and reduce coupling between adjacent elements. In coplanar waveguides, via holes are not necessary and fragile semiconductors need not be made excessively thin. Ground connections can conveniently be made at top of the substrate, which is well suited for use with microwave and millimeterwave transistors, especially at millimeterwave frequency where RF ground must be very near to the device [33], [34], [75], [101].

Available substrate for RF and microwave MCM and reasons for selection of silicon as substrate material for this work are described in section 2.2. As far as the metal concerned, copper (Cu) will clearly be the material of choice for future interconnection technologies. The candidates for future low dielectric constant (ε_r) interlayer dielectrics (ILD) fall into a set of inorganic and organic materials, which are represented in the section 2.3. Chapter 2.4 is an overview of the fundamentals of semiconductor technology used for fabrication of MCMs. Properties of materials involved in the enhanced QMIT are presented in section 2.5.

2.2 Available substrates for MCM technology for microwave applications

There are two types of substrate material for RF packaging: soft and hard substrate. The most important to RF packaging are described below. The most important criteria for selection of a substrate for RF packaging are cost and good RF, mechanical and thermal properties.

2.2.1 Alumina and glass alumina

Alumina and glass alumina are common substrates for MCMs. The fabrication of alumina substrate usully employs low temperature cofired ceramic (LTCC) and high temperature cofired ceramic (HTCC). LTCC and HTCC are alumina/glass systems that differ in glass content (50% vs. 4%) and firing temperature (850 °C vs. 1500 °C). The LTCC firing temperature permits the use of silver, gold and copper as conductors, while HTCC is limited to use of a higher melting point refractory alloy, such as tungsten and molybdenum. LTCC substrates thus have lower sheet resistance but higher dielectric loss tangent. Their mechanical strengths and thermal conductivities are also lower than those of HTCC substrates. Alumina and glass alumina substrates have good RF and mechanical properties and can be used to fabricate multilayer structures but their thermal conductivities usually are poor [67], [76].

2.2.2 Beyllium oxide

Beryllium oxide or beryllia (BeO) is an alternative substrate material an excellent thermal conductivity of 260 W/mK. However, it is not widely used because of toxicity of outgasing during substrate fabrication. Its thermal expansion coefficient (9E-6 K^{-1}) is very different than GaAs's thermal expansion coefficient and they can be used for multilayer structures fabrications [67], [76].

2.2.3 Aluminum nitride

Aluminum nitride (AlN) with high thermal conductivity of 150 W/mK, is becoming an appealing alternative to alumina. Its thermal expansion coefficient is 4.7E-6 K^{-1}, which is near to those of GaAs and silicon. It can be used for multilayer structures fabrications. AlN substrate also utilizes refractory metallizations, firing at 1800 °C. AlN powders are more expensive than alumina and result in higher substrate cost and electrical loss could be high [67], [76].

2.2.4 Soft substrate

The typical soft substrates are PTFE, FR-4 and polyimide. Normally their thermal expansion coefficient is quite far from those of silicon and GaAs and their thermal conductivity is very poor [67], [76].

2.2.5 GaAs

Semi-insolating GaAs substrate has very low substrate loss, can be micromachined and has a perfect matching of thermal expansion coefficient with GaAs-based devices. However, it has not been used very commonly because of their poor thermal conductivity and higher cost than silicon. Also, defects occurred during the growth of GaAs are higher than those of silicon and this affects the mechanical properties of the GaAs substrate [38].

2.2.6 Silicon

Silicon technology is mature, both for the production of uniformly polished high purity substrates and for device fabrication and integration (using Si-micromachining and MEMS). High resistivity silicon offers constant thickness and high dielectric constant, which is stable with frequency. In addition, polished silicon wafer substrates are very cost effective, and it has been reported that transmission lines on silicon substrate material have acceptable RF losses in the microwave and millimeterwave frequency regime [25], [33], [34]. Even it is reported that high resistivity silicon substrates have losses comparable with semi-insolating GaAs substrates [95]. Silicon has a thermal expansion coefficient close to that of GaAs and a high thermal conductivity (three times of GaAs's thermal conductivity). All these confirm silicon substrate as an excellent choice for MCMs [29].

In comparison with low resistivity Si-substrates, high resistivity Si substrates are rather expensive and metal layer on a Si-substrate construct a Schottky contact or a metal oxide semiconductor (MOS) structure which lead to slow-wave mode propagation on coplanar waveguide (CPW) [75]. To avoid these disadvantages and improve the performance of microwave circuits, Si-micromachining frequently has been used to

realize the passive elements for high frequency applications. The first advantage is improving circuit performance by increasing generated power and decreasing the loss and cost. The second and third are attaining additional functionality using mature silicon technology and the new integration capability [17], [94].

2.3 Copper on low dielectric interlayer interconnect technology

Several factors contribute to the performance of a particular interconnect, including its architecture and the properties of the materials involved.

In traditional interconnect technologies the metal of choice has been aluminum (Al) and the ILD has been SiO_2. This material system has some unique advantages compared to potential replacements. Al technology has matured over a long period of time, and extensive experience has been accumulated with the material in the semiconductor industry. Al reacts with SiO_2 to form a strong interface (an excellent adhesion), and the native oxide layer on Al also provides self-passivation with respect to further reaction. On the other hand, ressitivity is 2.7 μΩ cm which is higher than those of Cu, silver (Ag) and gold (Au). Al is alloyed often with silicon and/or Cu for reasons of stability with respect to the interaction with silicon and for improved electromigration resistance. Furthermore, in many applications a thin high resistivity layer is used as a barrier between the metal and ILD or silicon. These modifications may result in an increased effective resistivity for the Al interconnect lines of typically about 3.3 μΩ cm [111].

It is apparent already that for the only possible options in replacing Al are Cu, Ag and Au and the only practical option really is Cu. Not only do costs, manufacturability and device reliability favor Cu, but also in terms of improved resistivity the additional gain in going from Cu (1.7 μΩ cm) to Ag (1.6 μΩ cm) is minimal. It should be mentioned that Cu has some difficulties in pattering with plasma etching for ICs fabrications [87].

In contrast to the situation with the metals, the choices for the best ILD are much more open, and it is unclear at this point whether there will be a single winner in the end. Some of the generic issues to be resolved in connection with the introducing a new ILD are as below [111]:

- Electrical: low ε_r overall, controlled anisotropy, low dissipation and leakage, high dielectric strength.
- Chemical: chemical resistance, ability to be patterned, low moisture absorption, no metal corrosion.
- Mechanical: adhesion (ILD-Cu, ILD-ILD and ILD-substrate), low stress, high strength.

- Thermal: stability up to required temperature, low coefficient of thermal expansion coefficient, low thermal shrinking, high thermal conductivity.

The candidates for future low-ε_r fall into two classes of materials. The first one is comprised of a set of inorganic, silica-based oxides such as doped SiO_2, porous SiO_2, silica with air-gaps, hydrogen silsesquioxane. The second class of prospective ILD's involves a variety of organic polymers, for example: benzocyclobutene (BCB), SiLK, SU8 negative photoresist, spin on Teflon AF and various poyimide, etc. Among all these options BCB [43], [113], polyimide [66], [87] and SU8 [12], [92] are more common for RF and microwave applications and Teflon AF is an excellent option for future applications because of its lowest dielectric constant (ε_r = 1.7) of any known polymer. Teflon AF materials are currently under investigation for a wide variety of applications that require their unusual properties [111].

BCB has been commercialized under the name Cyclotene™ (Dow Chemical). These polymers are noted for their high glass transition temperature (>350°C), low moisture uptake (0.2% in 85°C at 85% relative humidity), low dielectric constant (ε_r = 2.6). Like polyimides, photoimagable Cyclotene™ materials have found wide acceptance in microelectronic, semiconductor and RF packaging. BCB materials can be made either photosensitive or non-photosensitive. One of the premier applications for non-photosensitive BCB is planarization over high aspect ratio substrate topographies. Because of the unique flow characteristics, the chemical-mechanical polishing (CMP) step can usually be eliminated [111].

The polyimides are one of the fastest growing categories of electronic polymers. They were first developed at DuPont in the 1950's. During the past 20 years, there has been tremendous interest in this material for electronic applications. The superior thermal (stability up to 500 °C), mechanical and electrical properties of polyimide have made its use possible in many high performance applications, including RF packaging. In addition, polyimides show very low electrical leakage in surface or bulk. They form excellent interlayer dielectric insulators and also provide excellent step coverage, which is very important in fabrication of the multilayer structures. Polyimides also offer excellent solvent resistance and ease of application [31].

Because all spin on polymers of BCB, polyimides and SU8 show good RF and mechanical properties, they can be used as dielectric layer underneath the Cu metallization in the enhanced QMIT fabrication process without facing any main difficulties. In this work a PI2811 type polyimide from HD MicroSystems is chosen because of its excellent thermal expansion coefficient of 3E-6 K^{-1} and planarization [31].

Cu-Polyimide multi-level thin film structures have been used over the past two decades in packaging of chips for MCM's [91]. To maintain structural integrity good adhesion is required between the various interfaces. Cu diffusion has also been reported on

polyimides [87]. The diffused Cu can increase the dielectric constant of the polyimide and degrade its mechanical and thermal properties. When Cu is deposited on cured polyimide, an adhesion and barrier layer, typically chromium (Cr), is used prior to Cu deposition. The Cr layer thickness is between 10 nm and 50 nm, and is deposited by sputtering or evaporation. For better adhesion, the polyimide surface is pretreated by either an oxygen based plasma cleaning or a light RF cleaning prior to the sputtering of the Cr/Cu metals [87].

2.4 Fundamentals of semiconductor technology used

In this section a very short survey of semiconductor technology useful for fabrication of MCMs has been presented in four subsections of micromachining, thin-film technology, photolithography and gold electroplating.

2.4.1 Micromachining

2.4.1.1 Bulk micromachining

The distinguishing characteristic of bulk micromachining is that it fabricates micromachined devices out of the bulk of a substrate. In recent years, several variants of this procedure have appeared that utilize different etching and patterning techniques. In this part, a brief overview on bulk micromachining will be offered that will include the most prevalent processing techniques.

Bulk micromachining begins with a single crystal substrate. A thin film of material that is inert to the chemical etchants, is then deposited on the substrate. For silicon substrates, silicon oxide or nitride are most commonly used as an etch mask. Then the film is patterned so that the undesired portions of the film are removed. This leaves the bare substrate exposed. At this point, the bulk material is etched. The etching of the bulk material can either be performed with a wet or a dry chemical etching. Since the processes associated with these etchings are substantively distinct, they will be individually addressed [109].

2.4.1.1.1 Bulk micromachining with wet etching

This anisotropic etch occurs in diagonal direction. This is a common feature of wet anisotropic etches. Since the early 1960s, alkaline solutions have been used to etch silicon along crystalline planes. The etch rate is slowest in the <111> direction and fastest in the <100> and <110> directions. The result of this uneven etch rate is that the bulk material is etched at an angle of 54.74°, which is the angle between the (100) surface and the four {111} planes. The ratio between the etching in the desired directions and the

etching in the undesirable directions is defined as the selectivity. An etchant that has a better selectivity will yield a more defined, and hence better, finished structure.

There are several characteristics of anisotropic etches that leads to important design considerations. The major constraint is that, designed features must be bounded by the {111} planes and this the resulting structures are necessarily rectangular, with sidewalls sloping away at 54.74 °. The use of less popular <110> oriented Si-wafers yields vertical sidewalls but the planar features can only be long parallel strips on the substrate, which have limited use. In recent years a number of groups have begun exploring dry etching processes that offer the possibility of anisotropic etchings.

One problem with using wet etching is that it creates sharp corners in silicon. These corners are natural stress concentration points that will weaken the strength of a structure. The use of chemical etchants can also lead to rough features on the surfaces of processed structures. The features, called hillocks in the literature, are a periodic undulation in the silicon. The presence of hillocks, which have been measured as high as 10 μm, precludes many electrostatic devices from operating properly. Furthermore, hillocks create natural stress concentration points that are more likely to fragment over time, which can create destructive free particulates in the MEMS device [79].

2.4.1.1.2 Bulk micromachining with dry etching

Bulk micromachining involving dry etching is performed in much the same way as bulk micromachining with a wet etch. There are several methods employed to produce finished devices through a reactive ion etch (RIE). While the processes vary by research group, all employ a deep reactive ion etch that can create aspect ratios higher than 20:1. It is the ability to produce these high aspect ratio structures, which can have higher mass and capacitance per silicon surface area than many other MEMS technologies that has helped to drive the development of RIE in MEMS production.

Dry etching can have reliability problems caused by the reactive ion etch. While the sidewalls created by these etches are intended to be vertical, they often have irregular features. Poor control over the conditions inside the etching machine can lead to unintended geometric effects on finished devices. One positive feature of using an RIE system is that it produced more rounded corners than wet etching. As a result, these structures are not as prone to fracturing as wet etched devices [104].

2.4.1.1.3 Wafer bonding

Wafer bonding has been used in recent years for both sealing microsensors and for the construction of composite sensors. There are several kinds of wafer bonding techniques commonly employed, which are discussed below.

Anodic or **electrostatic bonding** is a process that bonds a conductive substrate, which is usually silicon, to a sodium rich glass substrate. This is done by putting the two substrates into a direct contact. They are then heated to between 350-400 °C, which mobilizes the sodium ions in the glass. Then a voltage of 400-700 V is applied between the two substrates, with the glass substrate being made negative with respect to the silicon wafer. This repels the sodium ions from the interface and creates a ion-depletion region about 1 μm thick with electric fields on the order of 7E+6 V/m. This creates an electrostatic pressure of several atmospheres, which pulls the two wafers together while a thin layer of SiO_2 is formed. The end result of this process is a hermetically sealed bond with a strength that exceeds that of the individual substrates.

There are several reliability concerns in producing these bonds. The high temperature at which the bond is formed can induce thermal mismatch warping in a processed device. There can also be warping at the bonding interface from unmatched thermal coefficients of expansion. Another concern is the introduction of the large voltages and electric fields inherent to the bonding process. It is possible to destroy device in the bonding process if these factors are not considered [109].

Low-temperature glass bonding offers a viable alternative to anodic bonding for applications where high voltages are unacceptable. In this process, the bonding interface is covered with a thin-film of low-temperature glass. The wafers are placed into contact under pressure and heated to create the bond. The low-temperature glass then either melts or crystallizes, depending upon the actual glass used, which bonds the two substrates. In general, these bonds are not as strong, and thus less reliable, as anodic bonds [109].

Fusion bonding is a technique that fuses two materials together through high temperature. This process is used commonly in the production of silicon-on-insulator devices and pressure sensors. It is accomplished by taking two clean wafers and placing them on top of one another. This bonds the two wafers through Van der Waals forces. They are then placed into a furnace to create the final bond at temperatures in excess of 1000 °C.

While this process creates strong bonds it has some serious drawbacks. High furnace temperature, prohibit the use of active devices in the wafer prior to bonding. Furthermore, the weak initial bond makes the final bond strength very sensitive to the surface topology of the wafers and the presence of contaminants. For these reasons, these bonds are not always the most reliable and are often difficult to use [109].

2.4.1.2 Surface micromachining

Surface micromachining is a process that offers many advantages and disadvantages different from bulk micromachining. Surface micromachining differs from bulk processes in that devices are fabricated entirely out of thin film materials. One of the

most attractive features of this process is that it, like reactive ion etching, does not suffer from the 54.7° feature enlargement common to bulk micromachining with wet etchants. A key design feature of surface micromachining is the choice of structural and sacrificial thin films.

2.4.2 Thin-film technology

2.4.2.1 Evaporation

One way to place a thin-film material on a wafer is to evaporate them from a hot source. The evaporation system uses a vacuum chamber, which is pumped down to 10^{-6} to 10^{-7} Torr. A crucible is then heated or an electron beam is used to flash-evaporate material onto a sample. This process is controlled by a shutter, which limits the amount of time that the wafer is exposed to the crucible. The thickness of the film is governed by the length of time that the shutter is open and is also a function of the vapor pressure of the material. Thus materials with a high melting point, such as tungsten, require high temperatures to evaporate, which can burn organic films that are on the wafer.

Since evaporated films originate from a point source and the vaporized materials travel in a straight path, they suffer from shadowing effects that yield non-uniform thickness and poor step coverage [20]. A second factor affecting the coverage is the surface mobility of the species on the substrate. As a general rule, evaporated films are highly disordered, which causes a large residual stress and limits the thickness of the films.

2.4.2.2 Sputtering

Sputtering is a thin film growth technique that eliminates many of the problems inherent to flash-evaporation. Sputtering works by inserting a wafer into a vacuum chamber that is subsequently pumped down to between 10^{-6} and 10^{-8} Torr. Then an inert gas of a few mTorr of pressure is introduced into the system, which is then ignited into a plasma. The highly energetic ions of the plasma strike a target of sample material and tear atoms off its surface. These atoms then form a thin film across the wafer. This process creates a continuous planar flux of the species landing on the wafer, which makes preferable for mass production [109].

Another desirable aspect of sputtering is that the high-energy plasma does not have the same temperature problems inherent to evaporation. Most elements and many inorganic and organic compounds can be sputtered. Refractory materials that are difficult to evaporate can be easily sputtered as well.

Sputtering can also be done with more than one target, which allows control of the atomic composition of thin-film alloys. Sputtered films have better step coverage and uniformity than evaporated films, but they are disorganized structures whose mechanical properties and residual stresses are sensitive to sputtering conditions. Problems also arise from the inert gas used in the sputtering process, which can become trapped in the film and cause inconsistencies in the mechanical properties of the films [7].

2.4.2.3 Reactive growth

Reactive growth differs from the previously mentioned methods in that it utilizes chemical reactions with the substrate to construct thin films on wafers. The most common example of this process is the growth of oxide films on silicon wafers. In this process, a wafer is placed into a furnace with oxygen gas (dry oxidation) or steam (wet oxidation). The silicon is gradually oxidized at a highly predictable rate that depends upon temperature and crystalline orientation. Reactively grown films are usually of excellent quality but suffer from large residual stresses due to volume changes in the processed sample. In silicon dioxide growth, there is a volume change of about 45%, which causes mechanical warping [20].

2.4.2.4 Chemical vapor deposition (CVD)

CVD involves thermally breaking down gaseous compounds into their components. When they impact a wafer, some of these components nucleate onto it, which grows a thin film. CVD is limited by both the mass transport and reaction-limited processes, with the latter method being preferable due to its better uniformity. This process can be used to deposit many common semiconductor materials, including silicon dioxide, silicon nitride, polycrystalline silicon, and refractory metals. In low pressure thermal CVD (LPCVD) films with the most desirable mechanical properties are produced. Unlike other methods, conformal CVD films can be deposited on a sample. This property allows CVD films to seal cavities, which can be advantageous in many devices. The stresses and mechanical properties of CVD films can be controlled through the deposition conditions and subsequent annealing. A CVD process called epitaxial growth can be utilized to grow single crystal films on crystalline substrates [20].

2.4.2.5 Plasma deposition

Plasma-induced reactions are commonly used for the deposition of inorganic and organic materials. The decomposition of gaseous compounds into reactive species can be induced by the presence of plasma. This process is known as plasma-enhanced CVD (PECVD).

This process utilizes plasma that contains many ionized species. Some of these species are then deposited on the substrate, which form a solid film. PECVD films are

deposited at a faster rate and require a lower deposition temperature than thermal CVD films, which permits deposition on low melting point substrates. The organic films deposited through PECVD can be used as resists for no planar substrates. However, PECVD films contain cracks and pinholes. Accurate control of the stoichiometry is difficult as these films contain trapped byproducts from the reaction (especially H_2) that affect the film's mechanical integrity and residual stress [128].

2.4.3 Photolithography

Lithography is the process of defining features on the wafer according to a specified pattern or mask level. A radiation sensitive material commonly called resist is used to record the pattern. The resist may be positive or negative tone depending if it is removed or remains after the development of the irradiated regions. The development may be carried out with wet chemical etching, by dry plasma etching or by conversion to volatile compounds through the exposure radiation itself. The exposure radiation may be in the form of visible, deep ultraviolet or X-ray photons, or electron or ion beams of particles. The exposure can be made by a parallel process such as contact or projection printing from a mask or by serially scanning of one or more beams. Among all these technologies optical lithography (photolithography) holds the leading position in nowadays' semiconductor technology mainly because of its high wafer throughput. Important steps in photoresist processing are illustrated in Fig. 2-1 [20].

2.4.3.1 Optical systems

There are two categories of optical exposure tools. The two shadow methods of *contact* and *proximity printing* are the simplest and least expensive techniques, but they are not suited for industrial high volume production because of their high defect generation. For this reason the image forming technique of *projection printing* is predominantly used in today's semiconductor manufacturing. Both systems rely on a massively parallel approach, i.e., the entire mask or at least a large portion is imaged at once [20].
A totally different method is the optical scanning beam technique that serially synthesizes the pattern by moving a Gaussian elemental beam spot across the wafer. The basic principle of scanning beams remains the same, independent of the physical composition of the beam. The main concerns about this method are its low throughput and long time of scanning the wafer.

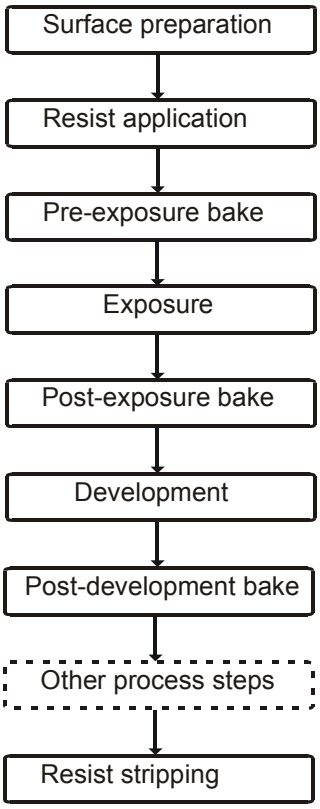


Figure 2-1: Important steps in photoresist processing.

2.4.3.2 Masks fabrication

Normally photolithographic masks are made using electron beam lithography because of high spatial resolution required. For fabrication processes with a larger minimum feature size the quartz mask is generated by photolithography as well. This processes utilizes a glass plate with Cr or emulsion patterns and entails the use of a computerized mask-making machine. It starts with a pattern for the mask being entered into the computer through commercially available CAD tools. The pattern is then broken down into small rectangular regions transferred to a mask-making machine. Then a glass plate coated with light blocking Cr or emulsion and photoresist is exposed. The mask maker to position the mask and determine the size of a variable aperture shutter on the ultraviolet light source uses the data on the computer. Each of the rectangular boxes is then individually exposed onto the plate. After this exposure step, the photoresist is developed and the Cr or emulsion patterns are etched [7].

2.4.3.3 Alignment and exposure

In processes that require multiple masks, each mask layer must perfectly match the features on the substrate. This is done by aligning the mask to special features, called alignment keys, on the wafer prior to exposure. A typical mechanical alignment utilizes a sample, mask holder, a stereoscopic microscope, an ultraviolet light source and a

precision positioning stage. This can either be done with a stepper aligner, which exposes one die at a time, or with a contact aligner, which exposes the whole wafer at once. Often in micromachining, the fabrication process requires photolithography to be performed on both sides of a wafer. To accomplish this, two masks are aligned to each other inside a secure assembly. Then the wafer is inserted and aligned to one of the two masks before being exposed to the ultraviolet light source. There is also an alternative method employed that uses an infrared microscope to locate alignment keys on the back-side, which could offer better alignment precision [20].

2.4.3.4 Etching and patterning techniques

After a pattern has been transferred onto a wafer, it is often necessary to strip away the unwanted sections of materials. This process, called etching, determines the dimensions of a fabricated device. There are several standard etching and patterning techniques, which are discussed below.

2.4.3.4.1 Lift-off

Lift-off is a simple patterning technique. It is accomplished by depositing a layer of sacrificial material, like photoresist, on a substrate. This layer is then patterned, which usually involves the photolithographic processes discussed above. Then a layer of structural film is evaporated onto the substrate. The pattern on the sacrificial layer is then transferred to the structural layer by removing the sacrificial layer. This has the effect of removing all of the structural material that is on top of the sacrificial layer, thus leaving a patterned structural film [128].

2.4.3.4.2 Wet etching

Wet etching involves immersing a wafer patterned with photoresist or other etching masks in a chemical bath. The chemical etchant selectively removes material not covered with the mask. The exact profile of the patterning depends on the anisotropy of the etching process. Wet etchants all exhibit a degree of isotropic behavior. This has the effect of undercutting the patterned structure, making it smaller than the resist mask. The degree to which the etchants etch the <100>:<110>:<111> directions is responsible for determining the maximum aspect ratio of many structures. Another important aspect of many etchants is their ability to selectively etch one material over the other. Called selectivity, this ratio determines how thick etch stops must be and provides dimensional limits on many technologies.

There are several different chemicals used in wet etching. Acidic etchants are used for isotropic release etchings. These are usually completely isotropic etchants that designed to separate suspended structures from the underlying substrate. Common acidic etchants

are HF, HNO_3, and CH_3COOH. These chemicals etch from 50 to 150 μm/h. For an anisotropic etch, alkaline etchants are commonly used. These exhibit different degree of selectivity and etch rates. Typically these chemicals etch <111> planes much slower than the <100> and <110> planes. Some etchants can also be influenced by the introduction of boron into the bulk material, which can greatly reduce the etch rate. It is also possible to influence etch rates in a process known as electrochemical etching, which involves applying a voltage across a p-n junction [79].

2.4.3.4.3 Dry etching

Dry etching, also referred to as RIE, involves using etchants in a gaseous state. The etchant is converted to a highly ionized plasma. Dry etching is performed in a chamber pumped down to a pressure between 10 mTorr and 1 Torr. A wafer is placed between two electrodes, which are then exposed to an RF voltage, which creates plasma in the chamber. Etching occurs when highly reactive free radicals in the plasma react with the solid-phase material of the film. The anisotropy of the etch is a result of the chemical reaction being preferentially enhanced on the side of the wafer parallel to the electrodes by bombardment from ions in the plasma. The ions impinge the surface of a film and expose underlying material, which is then etched away by the gas. The ions accelerate the etching process considerably, which means that the vertical sidewalls of the wafer, which do not interact with the ions, are not affected by dry etching.

GaAs anisotropic etching is usually performed in chlorinated gasses. One of the problems with GaAs etching is that, due to differences in the etch rates of group III and group V alides, the speed of etching in GaAs varies with crystal planes. In low power high pressure Cl_2 gasses, significant faceting can occur. There are several methods that can be used to avoid this problem. It is possible to add certain compounds to form polymers in the plasma and passivate the sidewalls, thus preventing the problem. Another possibility is to use hydrides to etch arsenic and methane to etch gallium. A mixture of AsH_3 and between 5 to 25% methane has been shown to be an effective anisotropic etchant [7].

One of the major drawbacks to RIE is residual damage caused by the etching. With ion fluxes of 10^{15} ions/cm^2 delivered at 300 to 700 eV, substrate damage and chemical contamination are serious issues to consider. Another problem is gas phase particle deposition and metallic impurities originating from the RIE chamber and electrodes. Several more complex techniques have been derived to remove these problems, but they come at added expense and preparation time. It is also known that the RIE can drive impurities into the bulk material to depths of 30 nm, which can affect the fracture strength of a structure [7].

2.4.4 Gold electroplating

Most of gold plating baths, utilize a gold cyanide complex. Gold plating compositions may also include other ingredients such as buffers, brighteners, current carrying species and chelating agents. Buffers stabilize the chemistry and increase conductivity. Brighteners promote grain refinement, resulting in a brighter appearance (all brighteners tend to decease the density of the deposits). Chelating agents increase conductivity, improve uniformity of the deposits, or serve as inhibitors for deposition of any base metals present.

Cyanide gold plating baths are of three types: unbuffered alkaline, buffered neutral and buffered acidic. Gold plating baths for microelectronic purposes are usually the acidic type. In the nonalkaline (acidic or neutral) baths, the flexibility in the pH allows freer use of photoresists for masking substance in plating operation. Acidic baths can also produce the purest gold deposit.

Plating bath are usually operated near 60 °C, and agitation is recommended. Acidic baths readily plate alloys, so contaminants must be rigorously excluded. Plating current may be dc, ac or ac superimposed on a dc bias. The ac methods generally yield decreased grain size. However, the pure gold films and acidic baths used in microelectronics tend to result in fine grains and ordinary dc plating is commonly used.

Another issue in gold plating is use of a strike or seed to initiate plating. The seed is a very thin, plated layer used to prepare the surface for subsequent normal plating. In general, such strikes are used to seal a surface (to prevent contamination of the plating solution) and to enhance adhesion. The seed layer for gold electroplating usually is a two-level metallization such as Cr/Au, Ti/Au or Pt/Au for good adhesion. Good electrical contact to the wafer is necessary, and the surface to be plated must be very clean.

In some applications, a useful approach is to plate gold simply by immersing the part into an appropriate solution, without use of electrical currents. Electroless processes are especially appropriate for plating nonconductive materials, such as semi-insolating GaAs. Such a process has been used to plate via holes and the backside of GaAs-MMICs. These techniques can be complex and troublesome, requiring surface activation by compound such as $PdCl_2$ [128].

2.5 Materials involved properties

The enhanced QMIT structure is constructed from a silicon substrate (Si-(100)), a GaAs-chip (GaAs-(100)), a spin on polyimide layer and either a PECVD layer of amorphous silicon or an electroplated gold layer [50], [122] .

Semiconductor properties remarkably change with temperature and crystal direction [4]. Considering these facts, properties of the materials involved have been presented in

tables I to IV. It is assumed that the silicon substrate and GaAs-chip exhibit elastic anisotropy and the rest of the materials are isotropic.

Table I

Properties of materials involved

Material	Amorphous-Si	Si-(100)	GaAs-(100)	Polyimide [31]	Gold
Young modulus (Pa)	100E9 [39]	-	-	6.6E9	78E9
Poisson ratio	0.27 [39]	-	-	0.35	0.44
Thermal expansion coefficient (1/K)	Table II	Table II	Table II	3E-6	14.2E-6
Thermal conductivity (W/mK)	Table II	Table II	Table II	0.14651	320
Elastic constants	-	Table III	Table IV	-	-

Table II

Temperature dependent thermal conductivity and thermal expansion coefficients of silicon and GaAs [40]

Temperature (K)	200	300	400	500	600	700
Silicon thermal conductivity (W/mK)	188.85	131.26	97.48	75.67	60.65	49.80
GaAS thermal conductivity (W/mK)	75.44	46.00	32.38	24.67	19.75	16.36
Silicon thermal expansion coefficient (1/K)	1.56E-6	2.63E-6	3.27E-6	3.6E-6	3.86E-6	4.0E-6
GaAs thermal expansion coefficient (1/K)	0.56E-5	0.57E-5	0.59E-5	0.6E-5	0.62E-5	0.63E-5

Table III

Temperature dependent second order elastic constants of Si-(100) [40]

Temperature (K)	200	300	400	500	600	700
C_{11} (Pa)	16.185E10	16.050E10	15.885E10	15.805E10	15.705E10	15.520E10
C_{12} (Pa)	5.880E10	5.825E10	5.800E10	5.695E10	5.615E10	5.600E10
C_{44} (Pa)	8.355E10	8.150E10	7.955E10	7.885E10	7.858E10	7.815E10

Table IV

Temperature dependent second order elastic constants of GaAs-(100) [40]

Temperature (K)	200	300	400	500	600	700
C_{11} (Pa)	11.955E10	11.825E10	11.696E10	11.501E10	11.355E10	11.195E10
C_{12} (Pa)	5.385E10	5.305E10	5.205E10	5.192E10	5.155E10	5.125E10
C_{44} (Pa)	6.015E10	5.925E10	5.865E10	5.759E10	5.625E10	5.569E10

Chapter 3

The Enhanced Quasi-Monolithic Integration Technology

3.1 Introduction

As outlined in the first chapter, the earlier concept of QMIT was introduced to overcome the problems of pure MMICs and of the conventional hybrid circuits and use the advantages of both alternatives. Although a few circuits containing low power active devices have been realized [119], the technology has suffered several shortcomings. Two major shortcomings of the earlier concept was high thermal resistance of the structure and the high induced thermo-mechanical stress, which results in an extremely low throughput [58]. In this chapter two novel fabrication processes, coplanar and microstrip circuit realizations, are introduced for QMIT, which not only overcome these problems, but also minimize the parasitics and enable the realization of the passive elements in this technology.

The enhanced QMIT fabrication processes, electrical characteristics of a high frequency active device embedded in this technology and the advantages of the novel technology are presented in detail in following sections.

3.2 The novel fabrication processes

Two different kinds of commercial GaAs-chips are available; with and without via hole grounding through substrate. The chips with via hole grounding are suitable for microstrip circuit realizations, while those without grounding scheme are suitable for

coplanar circuit realizations. Therefore two fabrication processes are introduced in this chapter.

For power applications, microstrip transmission lines are preferred to coplanar ones, and normally the power-chips have via hole grounding, microstrip circuit realization of the enhanced QMIT is an excellent solution for power applications but it uses high resistivity silicon substrate. Coplanar circuit realization of the enhanced QMIT can be used for both low noise and high power applications while using a low cost low resistivity silicon substrate.

3.2.1 Fabrication process for the coplanar circuit realization

Steps 1a to 15a in Fig. 3-1 show the whole fabrication process for coplanar circuit realization of the new generation QMIT. In the first step a 2 μm silicon-dioxide layer is grown using wet and dry thermal oxidation. Silicon dioxide is patterned by photolithography and the holes are made through the wafer by standard KOH wet etching. In the third step the residual silicon dioxide is removed. In the fourth step, a silicone gel layer is attached to the front side of the wafer and the transistor is placed using a fine placer machine within an accuracy of ±2 μm in the horizontal plane. In step 5a lift-off photoresist (LOR) is used to fix the transistor temporarily. The photoresist should be cured very gently from room temperature to 120 °C and kept at this temperature for 5 to 10 min. Now the silicone gel can be removed gently and the LOR baked for a further 5 to 10 min at temperatures between 140 and 180 °C. This ensures that the LOR does not intermix with the next positive photoresist and can be easily removed with standard developers [11].

Fig. 3-2 illustrates the white light interferometery two-dimensional mapping of a transistor fixed in the hole after step 6a. Only a quarter of the transistor is shown. Fig. 3-3 shows the profile measurement along the line A-A in Fig. 3-2. As is shown the transistor can be fixed in the plane of the silicon substrate within an accuracy of ± 1.5 μm, which is quite adequate for the rest of the process.

In step 7a, a positive photoresist is spun on and baked at 90 °C for 10 to 15 min. As there is no intermix between the two photoresists, the LOR can be washed away by a developer easily. In the next step 9a, 5 to 10 μm of amorphous silicon is deposited using PECVD at the low temperatures between 60 and 200 °C. A higher temperature gives a higher deposition rate and better quality and a minor increase in thermo-mechanical stress because of difference in the thermal expansion coefficients of silicon and GaAs. The photoresist is then washed away by acetone. In this step the transistor is successfully integrated and fixed by the amorphous silicon layer. PI2611 type polyimide, which has a low ε_r of 2.9 and a thermal expansion coefficient of 3E-6 K^{-1} (very near to silicon and GaAs) is spun on and cured according to the manufacturers data sheet. A dry-etching

mask such as an aluminum layer is deposited and patterned and the polyimide removed by oxygen plasma etching. The coplanar waveguide metals (2 µm copper on a 20 nm chromium adhesion layer as is used in our process) are then deposited and patterned. At the end, to decrease the thermal resistance of the structure, the holes can be filled out by diamond-filled PI2611 polyimide. This gives an excellent thermal path (because of the diamond) and does not induce a high thermo-mechanical stress. However, this step is not necessary for low and medium power applications. Fig. 3-4 shows the scanning electron microscopy (SEM) of the embedded low noise GaAs-based p-HEMT in the coplanar circuit realization of the enhanced QMIT.

In this technology it is possible to use other dielectrics such as SU8 photoresist or BCB instead of PI2611 type polyimide for the planarization and as a dielectric layer underneath the coplanar waveguide. SU8 is an organic negative photoresist, which has an excellent adhesion to silicon substrate and can be easily patterned with a standard chemical wet etching. This makes the fabrication process simpler and steps 11a and 12a are eliminated. The low thermal expansion coefficient of the PI2611 type polyimide used ensures a lower thermo-mechanical stress in the enhanced QMIT structure.

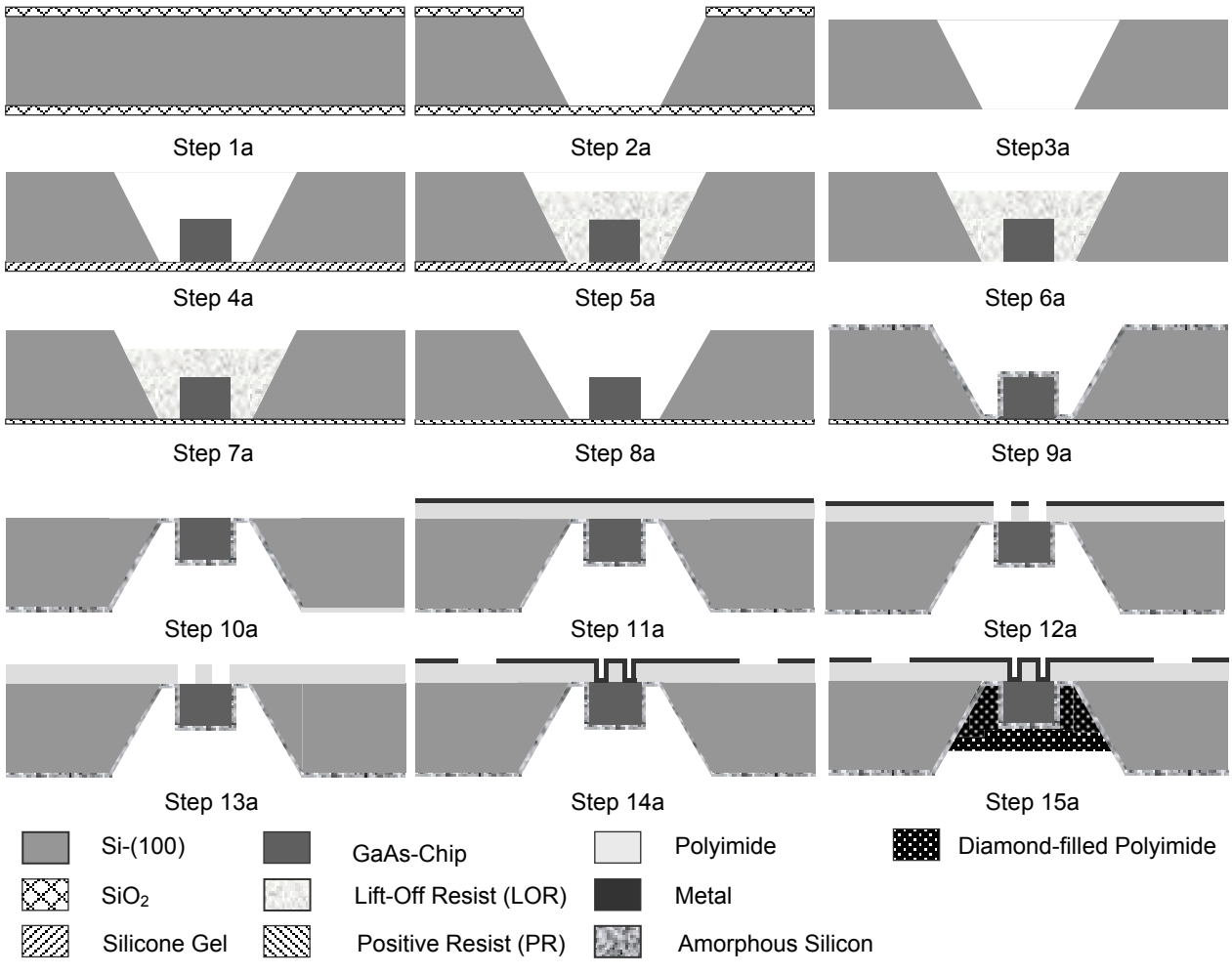


Figure 3-1: Process steps for the coplanar circuit realization in the enhanced QMIT.

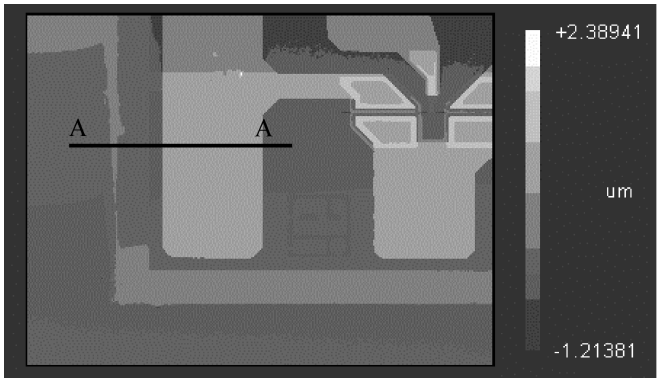


Figure 3-2: White-light interferometery mapping a transistor fixed in the hole using LOR photoresist after step 6a. Only a quarter of the transistor is shown.

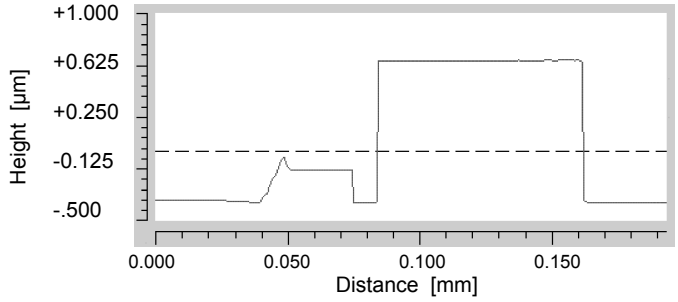


Figure 3-3: Profile measurement along the line A-A in Fig. 2-2.

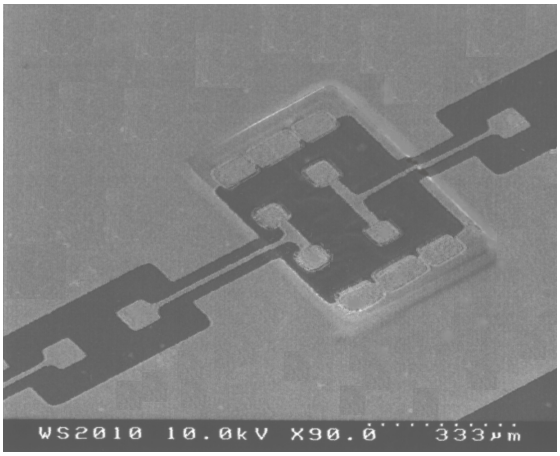


Figure 3-4: SEM of the fabricated microtest-fixture for the coplanar circuit realization in the new QMIT.

3.2.2 Fabrication process for microstrip circuits realization

Steps 1b to 15b in the Fig. 3-5 show the whole fabrication process for microstrip realization of the new generation QMIT. Most of the steps in this process are similar to those for the coplanar realization, but there are two main differences. First, transitions from microstrip to coplanar waveguides are realized using vias for ground contacts for on-wafer measurements. Secondly, instead of the amorphous silicon a gold layer is electroplated. The gold layer fixes the transistor in the hole and is used as a ground plane for the microstrip transmission line. For this realization a high resistivity silicon substrate

should be used. The process is compatible with power transistors with vias for the source terminals. From experience, 3 to 5 μm thick plated gold is enough for these purposes.

Special attention has been paid to the realization gold electroplated layer. A very thin layer of metal with a good adhesion should be deposited to prepare the substrate for electroplating. A thin layer of e-beam evaporated Ti (20 nm)/Pt (50 nm) was used, which gives an excellent adhesion. This layer should cover the backside of the transistor and the holes completely. For this reason, the wafer is rotated around its axis and kept inclined to the direction of evaporation with a suitable angle during the metallization. Because of difference in thermal expansion coefficient of the thin layer metal and the positive photoresist, there are very narrow cracks, which separate the metal deposited on photoresist and the metal on the backside of the transistor and the silicon wafer but these cracks are small and are eliminated after some seconds of electroplating. To avoid the cracks, instead of the positive photoresist a thin layer of amorphous silicon can be used for fixing the transistor from the top. This is more time consuming than the handling of the positive photoresist.

To connect the front-side metal to the backside metal the polyimide at the top of the holes is etched away in the step 12b. Fig. 3-6 illustrates the backside view of the embedded power transistor fixed by the electroplated gold and Fig. 3-7 shows the front-side view of the transistor after step 12b. Fig. 3-8 depicts the front-side view of the wafer on a via for transition of the microstrip to the coplanar waveguides after step 13b.

3.3 Electrical characteristics of an embedded Ka-band low noise GaAs-based p-HEMT in the enhanced QMIT

DC characteristics of a Ka-band low-noise AFP02N3 p-HEMT from Alpha industries in the coplanar waveguide realization is shown in the Fig. 3-9. The transistor is fixed by an 8 μm thick PECVD amorphous silicon layer without diamond-filled polyimide in the backside.

On-wafer bias-dependent S-parameter measurements (0.1-40 GHz) for the same sample have been made using an HP 8510B network analyzer. Fig. 3-10 presents of magnitude and phase plots of the measured S-parameters for of V_{gs} = 0.1 V and V_{ds} = 1.8 V. The measurements include the effect of coplanar waveguide.

An acceptable agreement between the measured dc and ac characteristics and the data given in the manufacturers data sheet was found. The dc current gain is 8.5% smaller and the S_{21} is 7% higher than those for the particular case given in the manufactures data sheet. This can be explained by the direct connection between the source terminal and the ground plane as compared to the four 200 μm long and 17 μm diameter gold wire-bonding in the manufacturers measurements.

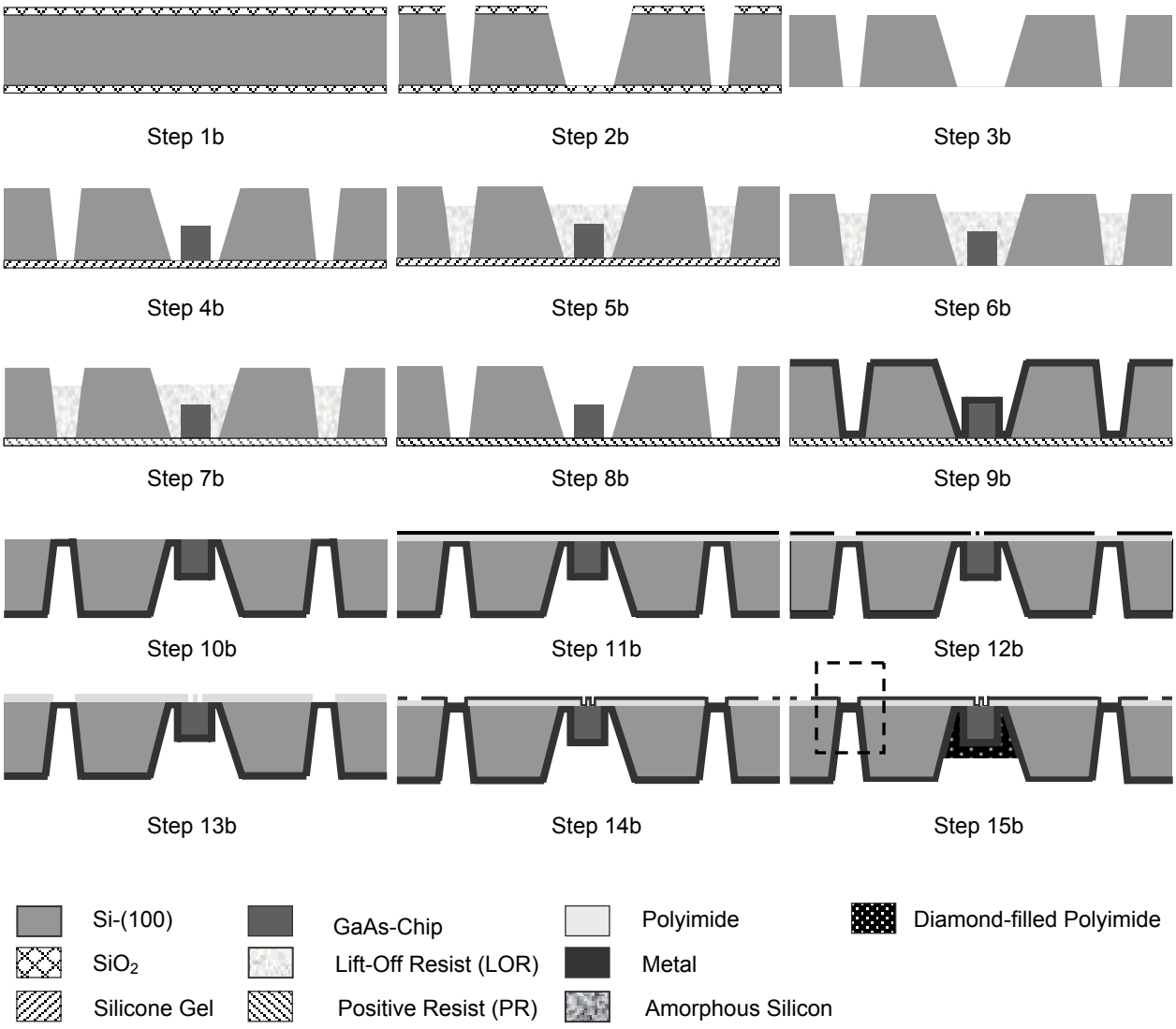


Figure 3-5: Process steps for the microstrip circuit realization in the enhanced QMIT.

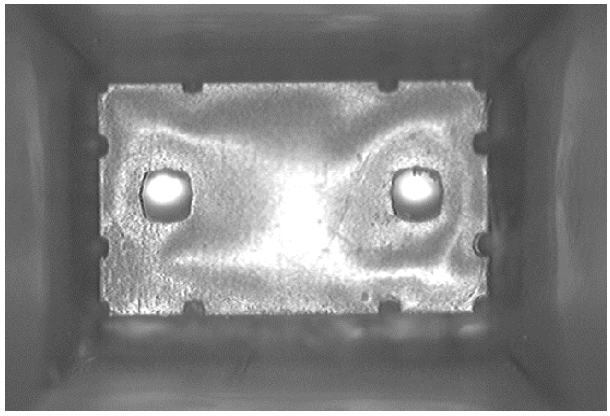


Figure 3-6: Backside view of an embedded Ka-band power AFM08P2 GaAS-MESFET from Alpha Industries in the microstrip circuit realization of the enhanced QMIT.

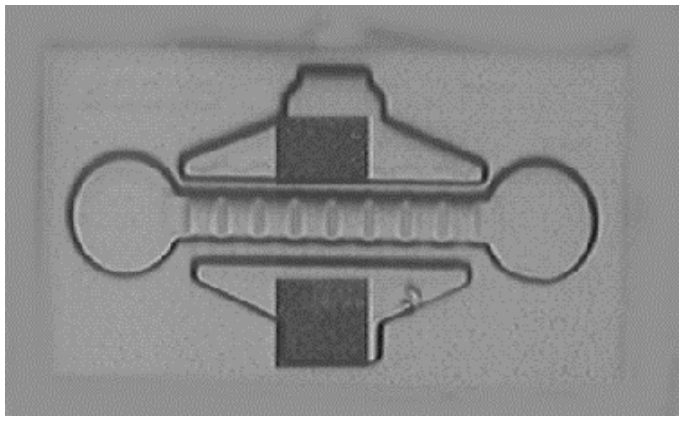


Figure 3-7: Front-side view of an embedded Ka-band power GaAs-MESFET after step 12b.

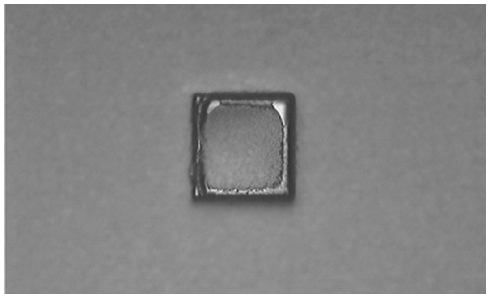


Figure 3-8: Front-side view of the wafer on a via for transition of microstrip line to coplanar waveguide. Dashed square in step15b of Fig. 3-5 represents this transition.

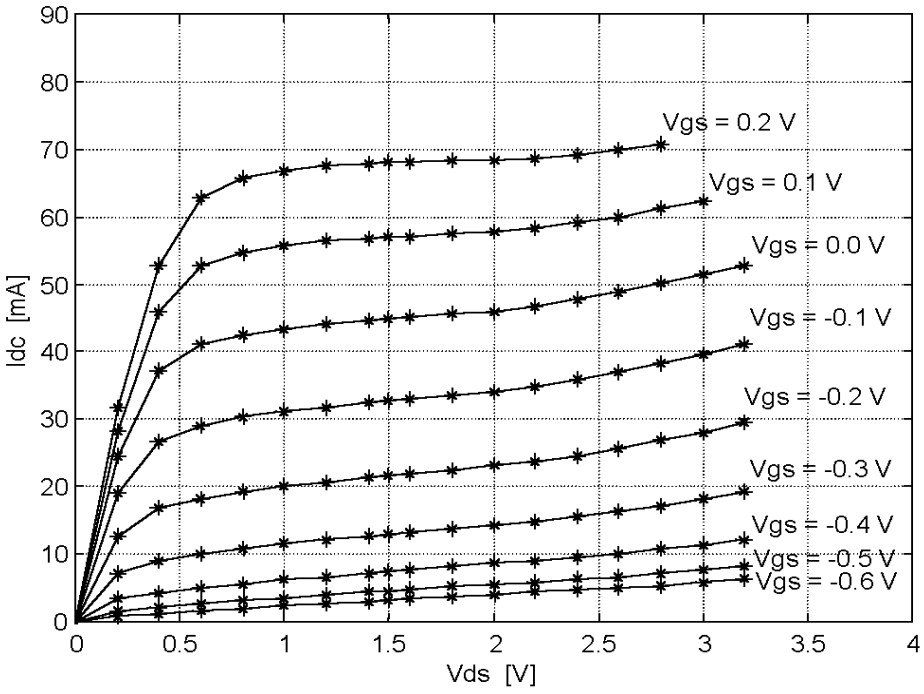


Figure 3-9: I-V curves of the Ka-band low noise p-HEMT in coplanar realization in the new generation QMIT. The transistor is fixed by an 8 mμ thick amorphous silicon.

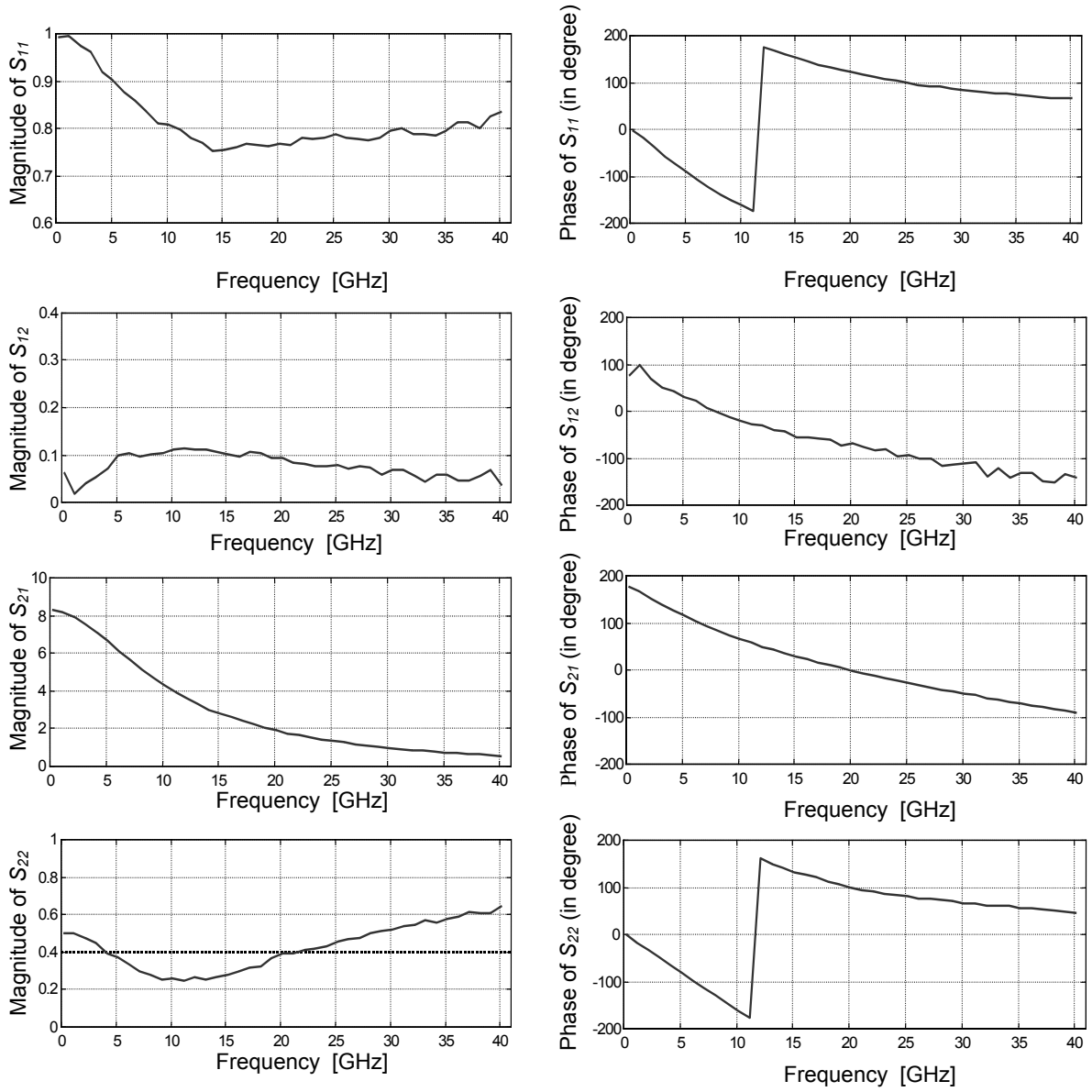


Figure 3-10: S-parameter magnitude and phase plots of the Ka-band low noise p-HEMT with coplanar realization in the new generation QMIT with bias point of V_{gs} = 0.1V and V_{ds} = 1.8 V.

3.4 Advantages of the enhanced QMIT

The earlier concept of QMIT was introduced to alleviate the problems of pure MMICs and of the conventional hybrid circuits. Although a few circuits containing low power active devices have been realized [119], the technology has suffered several shortcomings, which have been described in section 1.2.3.

- In the novel technology, active devices are fixed using low temperature PECVD amorphous silicon (for coplanar realization) or an electroplated gold layer (for microstrip realization). In this case the upper temperature limitation for the fabrication process is determined by the temperature specifications of the

embedded chip itself, which should be well below 300 °C for the GaAs-chips. This is adequate for a successful realization of passive elements in this technology.

- The better geometrical construction and smaller differences in the thermal expansion coefficients of the materials involved induce a much lower thermo-mechanical stress distribution, which results in a significant improvement of lifetime of the packaging [57].
- A thick layer of polyimide or other spin-on dielectrics gives a proper planarisation for the front-side metal deposition around the transistor and the air-bridges are no longer necessary.
- The source terminal of the transistor is directly connected to the ground plane, this minimizes the source inductance and improves microwave characteristics of the embedded transistor.
- Although a smaller dimension of passive elements is possible on a high resistivity silicon substrate than polyimide layer, by suitably adjusting the dimensions of the coplanar waveguide, passive elements and the thickness of the spin-on dielectric layer, realization of high-Q passive elements is achievable.
- By eliminating the fragile air-bridges, the new fabrication process enables the fabrication of the rest of the circuit after measuring microwave parameters of the embedded transistor. This results in very accurate microwave and millimeterwave circuit designs.
- At the end of the fabrication process, the holes are either filled with diamond-filled polyimide or a thick backside electroplated gold is used, which provides an excellent thermal resistance. Lower thermal resistance improves the lifetime of the packaging and leads to better electrical characteristics of the transistor.

3.5 Summary

A successful approach for integrating III-V semiconductor compound-based active devices in a silicon substrate has been presented. The advantages have been described and two fabrication processes for coplanar and microstrip circuit realizations in this novel technology introduced. In addition to the great improvement in lifetime and thermal resistance of the packaging in comparison to the earlier concept, integration of the power active devices and high-Q passive component fabrication is possible for the first time. In the new technology it is possible to measure the microwave parameters of the embedded transistor and then fabricate the rest of the circuit. This provides very accurate microwave and millimeter designs.

Chapter 4

Static Thermal Analysis and Management in the Earlier concept and enhanced QMIT

4.1 Introduction

The bi-directional influence of temperature on reliability and performance of packaging is well known in electronic designs. This influence is more crucial in higher frequency applications, where the designs are more sensitive to the characteristics of the devices. Thermal breakdown of active devices, carrier density, carrier mobility, band gap of semiconductors, traps and defects in semiconductors, current gain of active devices, threshold voltage of FETs, noise figure of the active devices, saturation current of pn-junctions or Schottky contacts, ohmic contacts, resistivity of the semiconductors, active device capacitances, power gain and band width of the active devices all are functions of temperature as well as electromigration, die fracture, die and substrate adhesion fatigue, failure mechanism in interconnections and failure mechanism in the package case .

Steady-state temperature, temperature cycles, temperature gradients and time dependent temperature changes all have the potential to affect the device and package performance and reliability. However, because of dominant influence and required use of reliability prediction methods, steady-state temperature has often been considered as main parameter [74]. Maximum channel temperature and thermal resistance of the GaAs-FET and thermal path of the packaging are among the most important issues for design engineers or technology developers [1]. Any improvement in the thermal resistance of the packaging readily leads to better performance and reliability.

Many system designers and reliability engineers consider temperature to be a major factor affecting the reliability of electronic equipment. Unfortunately, in an effort to improve reliability, design teams have often lowered temperature without fully understanding the impact on cooling system reliability, in costs, weight and size and the extent of any actual reliability improvement. To address the actual impact of temperature, design engineers together with thermal management and reliability engineers should utilize a physics-of-failure methodology. There are six steps to this method [74]:

- Develop a through knowledge and understanding of the environment in which the equipment will operate. Usually, the customer will specify the operating in the terms of absolute physical parameters, such as temperature ranges, or will quote the relevant chapter in some handbook or specification. It may be better to state where and how the equipment will be used.
- Develop an understanding of material properties and architectures used in design. This involves tailoring the product design to requirements by modifying materials geometry, allowable manufacturing defects, and operating stresses.
- Learn how products fail under various degrading influence. This involves assessing the potential failure mechanism and determining the role of stresses, including steady state, temperature cycling, temperature gradients and time-dependent temperature changes, on the failure mechanism.
- Examine field failure data providing information on how failures occur.
- Control manufacturing to reduce those variabilities that cause failure.
- Design the product to account for temperature-related performance degradation. As already mentioned, steady-state temperature has an influence on many electrical functional parameters, including propagation delays and noise figures.

Because of the huge area of study and necessity of knowledge about maximum channel temperature and thermal resistance of packaging (as most important parameters) for first success designs, this chapter only deals with static thermal analysis of the earlier concept and enhanced QMIT. Next two sections are dedicated to the influence of temperature on reliability and electronic properties of active devices. Section 4.4 describes finite element method briefly and the basics of heat transfer in solids are described in section 4.5. A nonlinear three-dimensional finite element temperature simulator has been used to investigate the static heat transfer analyses in the different structures of QMIT in section 4.6 and 4.7, respectively. In section 4.7, the maximum channel temperatures in the both technologies are also compared and discussed. To confirm the validity of the transistor models used in the simulation and present capability of a novel thermal nano-probe in the two-dimensional thermal imaging of microwave active devices, thermal simulation and far-field and near-field temperature measurements

on a UHF-band power GaAs-MESFET are performed and presented in section 4.8. Section 4.9 summaries the chapter.

4.2 Influence of temperature on reliability

Much of reliability theory and reliability testing is based on the assumption that the rate at which chemical and physical changes occur in devices is exponentially dependent on temperature, and is given by the Arrhenius[1] equation [74]:

$$r_r = r_{r\sim ref} e^{-E_a / k_B T} \tag{4-1}$$

where r_r is the reaction rate (moles/m^{2}s), $r_{r\sim ref}$ is the reaction rate at a reference temperature (moles/m^{2}s), E_a is the activation energy of the chemical or physical reaction (eV), k_B is Boltzmann's constant (8.617E-6 eV/K) and T is steady-state temperature (Kelvin).

Equation (4-1) has been used to assess the temperature dependence of a wide variety of reaction rate constants and diffusion coefficients often crudely, but sometimes quite accurately [128]. Arrhenius-based models have been reformulated to predict the influence of steady-state temperature on electronic device reliability. In this case, the mean time to failure (*MTTF*), which will be introduced in the next chapter, for a given steady-state temperature is represented as:

$$MTTF = MTTF_{ref} e^{E_{a\sim dev} / k_B T} \tag{4-2}$$

where $MTTF_{ref}$ is the mean time to failure at a specified reference temperature and $E_{a\sim dev}$ is the device activation energy (eV).

4.3 Influence of temperature on electronic properties of active devices

As GaAs-MESFETs and GaAs-HEMT have been utilized in the enhanced QMIT, only these devices will be discussed here. Temperature affects dc and microwave characteristics of active devices in many ways. The major physical factors are described in the following subsections.

4.3.1 Influence of temperature on material factors of GaAs

Band gap of GaAs ($E_{g\sim GaAs}$), carrier densities and dielectric constant ($\varepsilon_{r\sim GaAs}$) are functions of temperature as [1], [2], [98], [102], [105], [108], [130]:

[1] Savante Arrhenius a Nobel Prize winner in chemistry in 1889.

$$E_{g\sim GaAs} = 1.54 - \frac{5.4\times10^{-4}T^2}{T+204} \quad [\text{eV}] \tag{4-3}$$

$$n_i = 2\left(\frac{2\pi k_B T}{h}\right)^{3/2}\left(m_n^* m_p^*\right)^{3/4} e^{-E_g/2k_B T} \tag{4-4}$$

$$\varepsilon_{r\sim GaAs}(T) = \varepsilon_{r\sim GaAs0}(1 + B_\varepsilon(T-300)) \tag{4-5}$$

where h is Plank's constant, m^* is carrier effective mass, $\varepsilon_{r\sim GaAs0}$ is the dielectric constant of GaAs at 300 K and T is the temperature in Kelvin.

These factors do not have large effect on FET currents or capacitances because in GaAs, the active shallow donors are effectively totally ionized, independent of temperature. The required charge neutrality condition forces the Fermi-level to adjust such that the electron concentrations are pinned to the shallow donor concentrations, which counters the changes in electron concentrations and $E_{g\sim GaAs}$ with temperature.

4.3.2 Influence of temperature on the electron drift velocity and mobility

In order to have the electron drift velocity as a function of electric field and substrate temperature, one should solve the Boltzmann balance equation for the first three moments of carrier number, momentum, and kinetic energy. Such models are well documented in the literature, so only the main aspects will be described here [135]. Under steady-state conditions in uniform and homogeneous materials, the momentum balance equation yields an electron drift velocity of

$$v_n = -\frac{q}{m^*}\tau_m(T_e, T)F_e \tag{4-6}$$

where q is the electronic charge, F_e is the electric field strength, T_e is electron temperature and τ_m is the momentum relaxation time, which is explicitly a function of the electron and lattice temperatures. Similarly, the balance equation for kinetic energy is:

$$-qv_n F_e = \frac{3}{2}k_B\frac{T_e - T}{\tau_e(T_e, T)} \tag{4-7}$$

where τ_e is the kinetic energy relaxation time, which is also a function of the electron and lattice temperatures. Both τ_m and τ_e are determined from the sum of the rates of the operative scattering processes within the material. Once all of the scattering mechanisms have been incorporated into τ_m and τ_m, the above two equations can be solved simultaneously to produce the electron drift velocity as a function of the electric field and substrate temperature $v_n(F_e, T)$.

Fig. 4-1 illustrate the calculated velocity-field relationship for $In_{0.15}Ga_{0.85}As$ as a function of temperature in an AlGaAs/InGaAs p-HEMT [135].

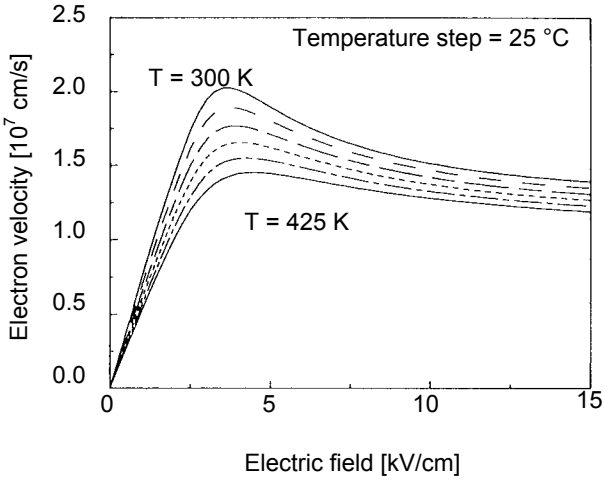


Figure 4-1: Calculated velocity-field relationship for $In_{0.15}Ga_{0.85}As$ as function of temperature for an AlGaAs/InGaAs p-HEMT [135]. As temperature increases the electron velocity decreases.

4.4.3 Influence of temperature on threshold voltage

The threshold voltage of the modulation-doped FET using AlGaAs/GaAs heterojunction is given by:

$$V_{th} = \phi_b - \Delta E_c - (\frac{qN_d^+ d^2}{2\varepsilon_{AlGaAs}}) \tag{4-8}$$

where ϕ_b is the Schottky barrier energy that decreases with increasing temperature, ΔE_c is the conduction band discontinuity, N_d^+ is the total ionized donor density in AlGaAs and d is the thickness and ε_{AlGaAs} is the dielectric constant of doped AlGaAs [115]. If we assume that the deep donors are in thermal equilibrium with the conduction band then the initial value of the threshold voltage (after the instantaneous application of a negative gate bias) is given by:

$$V_{th}(T) = \phi_b - \Delta E_c - \frac{qN_d d^2}{2\varepsilon_{AlGaAs}} - \frac{qN_{dT} d^2}{2\varepsilon_{AlGaAs}} \frac{1}{1 + g\exp(E_{FO} + E_D / k_B T)} \tag{4-9}$$

where N_d is the density of the shallow donors which are always ionized, N_{dT} is the density of deep traps, g is the degeneracy factor of the deep donor level (unity assumed here), E_{FO} is Fermi-level for electrons in AlGaAs layer at equilibrium (measured from the bottom of the conduction band) and E_D is the energy level of deep traps.

4.4.4 Influence of temperature on noise figure

The main sources of noise in a MESFET or HEMT can be identified as [90], [116]:

- Thermal noise of the parasitic resistances, mainly drain and gate resistances.
- Thermal velocity fluctuations in the channel.
- Fluctuations in the thickness of the channel.
- Scattering of electrons between the different valleys in the conduction band, (this will only occur in regions of high field strength, i.e. at the drain side of channel).

At low frequencies there is extra noise caused by traps in bulk and surface states. These traps capture and release electrons with time constants of micro to milliseconds. This result is noise with a quasi-*1/f* character in the frequency region below 1 MHz.

Considering the drain and gate noise current sources and their noise correlation and assumption that the average electron temperature is proportional to the lattice temperature, minimum noise figure is as below [22]:

$$N_{f\min} = 1 + 2\frac{T_{device}}{T_{room}}\frac{f}{f_c}\sqrt{g_m(R_s + R_g)(i_{nd} + i_{ng} - 2C_i\sqrt{i_{nd}i_{ng}}) + i_{nd}i_{ng}(1 - C_i^2)} \qquad (4\text{-}10)$$

where T_{device} and T_{room} are the device and room temperatures respectively and f the frequency. In this formula, i_{nd}, i_{ng} and C_i refer to the drain and gate noise currents and their noise correlation, respectively.

4.4 A survey of finite element method

Modeling and numerical simulation of the fabrication process and the operation of individual microdevices as well as full microsystems are becoming indispensable in the development of MEMS. Computer aided design (CAD) can significantly reduce the number of costly trial and error steps on the way to an optimized prototype [32], [103].

The enhanced QMIT structure, like most of other micomachined or micromechanical structures, is too complex to be analyzed by analytical approaches. ANSYS package [3] is used in all thermal and structural numerical analyses in this dissertation. This package provides the user with great capabilities in the nonlinear three-dimensional finite element thermal and structural simulations.

The basis of finite element analysis is the concept of dividing mechanically deformable structures into small elements (finite element discretization) for which exact or at least approximate correlations of forces and deformations can be stated. Knowing the boundary conditions, the equilibrium can then be found for the complete structure; the equilibrium is found when correlations for each element as well as boundary conditions are satisfied.

Recently, many efforts have been made to adapt commercial finite element simulators to micromachined and MEMS structures, which were developed mainly for civil and

mechanical engineering applications. The community of packaging designers has accepted those programs, but some specific concerns should be considered in micro-domain [103]:

- When scaling down a device, volume forces get smaller and surface forces larger.
- Aspect ratios for micromachined membranes and beams are unfavorable for these commercial programs.
- Material data are difficult to measure - for instance, such data are usually known for bulk material, but not for thin films that are often used.
- Mechanical properties of semiconductor crystal material are anisotropic.
- There are stresses due to technological process in multilayer systems, which cannot be easily predicted.
- Very often, coupled field effect simulation is of interest.

The biggest problem in the usage of these programs is the procedure of meshing. In finite element method, the complex mechanical structure is divided into simple elements, which are connected to each other at points called nodes. That division is called meshing. An example of a meshed structure (micromachined membrane) is given in Fig. 4-2. By increasing the dimensional aspect ratios of the micromachined structures, the mesh density will exponentially increase and in some cases the simulations are not affordable and requires some modifications in the model specifications.

When a user is interested in simulation of mechanical displacement as the result of the application of some load, the problem of modeling is reduced to the description of the geometry and description of the mesh, since the equations for mechanical behavior are already implemented in the program. However, this problem is far from trivial, since the meshing is not simple. The problem is that inappropriate meshing will usually lead to successful simulation, but with inaccurate results [100]. The meshing demands experience from the user, as well as good understanding of the underlying physics.

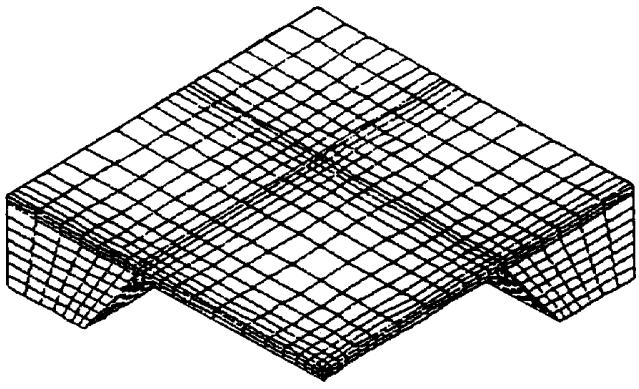


Figure 4-2: Anisotropically etched membrane modeled with three-dimensional solid elements in ANSYS [103].

For different micromachined devices some common problems can be defined for the meshing. For that reason, it was possible to produce software support for using finite element programs, developed specially for micromechanical applications such as CAEMEMS [8]. They are helping in the meshing procedure in the way that the user has already defined geometries that are of common interest in micromechanics. The user can parameterize these geometries (by defining dimensions and physical parameters), and meshing is already determined for them. A finite element analysis program is then invoked, to execute the simulation.

4.5 Basics of heat transfer analysis

The problem of heat transfer involving diffusion and convection can be described by:

$$\nabla \cdot \vec{k} \nabla T + Q = \rho c \frac{\partial T}{\partial t} + \nabla \cdot (\rho \vec{u} T) \tag{4-11}$$

in which *T(x, y, z, t)* is the temperature distribution, ρ is the density, *c* is the specific heat, *k* is the thermal conductivity, t is the time, $\vec{u}$ is velocity field and Q is the rate of heat flow [41].

In order to solve this differential equation, one needs the initial condition at time $t = t_0$ in the domain Ω and boundary condition on the surface Γ for a particular problem. The initial temperature field must be specified as:

$$T(x, y, z, 0) = T_0(x, y, z) \qquad \text{in } \Omega \tag{4-12}$$

There are two typical boundary conditions involved in. The first type specifies the values of temperature at the boundary Γ_T. These values may be constant or allowed to vary with time, i.e.

$$T = T(x, y, z, t) \qquad \text{on } \Gamma_T \tag{4 -13}$$

A boundary condition of this form is frequently referred to as a Dirichlet or essential boundary condition.

In the second type, the values of the heat outflow in the direction $\vec{n}$ normal to the boundary Γ_q are prescribed as $\bar{q}(x, y, z, t)$. Then we can write:

$$-k \frac{\partial T}{\partial |\vec{n}|} = \bar{q} \qquad \text{on } \Gamma_q \tag{4-14}$$

This type of boundary condition is often called a Neumann or natural boundary condition.

In many cases, heat convection occurs during heat exchange across fluid and solid boundaries. Therefore, convection may be considered as a kind of boundary condition to

the solid domain (such a GaAs-chip surrounded by air). According to the Newton's rule convective heat transfer is a function of the temperature difference between the solid and fluid, T_s and T_f:

$$\bar{q} = H(T_s - T_f) \tag{4-15}$$

where $\bar{q}$ and H are the heat flux and the heat transfer coefficient between the solid and the fluid. Therefore, the boundary condition equation (4-14) can be express as:

$$-k\frac{\partial T}{\partial|\vec{n}|} = H(T_s - T_f) \qquad \text{on } \Gamma_q \tag{4-16}$$

In contrast to mechanisms of conduction and convection, where energy transfer through a material medium is involved, heat may also be transferred by electromagnetic radiation that is propagated as a result of a temperature difference. It has been established that an ideal thermal radiator, namely, a blackbody, will emit energy at a rate proportional to the fourth power of the absolute temperature of the body,

$$q = \sigma_{SB} T^4 \tag{4-17}$$

where σ_{SB} is the proportionality constant and is called the Stefan-Boltzmann's constant with a value of 5.669E-8 W/m^2K^4. Equation (4-17) governs radiation emitted from a blackbody only. In fact all materials emit a fraction of the blackbody radiation, i.e.

$$q = \varepsilon_{rad}\sigma_{SB} T^4 \tag{4-18}$$

where ε_{rad} is called the emissivity. For a blackbody ε_{rad} is 1. For other surfaces, ε_{rad} is less than 1.

In practice we are usually concerned with radiation between two systems, which are at temperatures T_1 and T_2 with $T_1 > T_2$. The surface at T_2 will emit some radiation, but it will receive more radiation from T_1 and hence its temperature will rise. The net heat received by body 2 is:

$$F_{12}\varepsilon A\sigma_{SB}(T_1^4 - T_2^4) \tag{4-19}$$

where A is the receiving area of body 2, and F_{12} is a geometry dependent view factor between body 1 and body 2. Since radiation only occurs between systems, it is apparent that radiation is considered as a boundary condition in the differential equations of heat conduction. A simple radiation problem is encountered when we have a surface at temperature T_1 completely enclosed by a much larger volume maintained at T_2 (for example a Si-substrate surrounded by air). Then the net radiant exchange in this case can be written as:

$$\varepsilon_{rad1} A_1 \sigma_{SB}(T_1^4 - T_2^4) \tag{4-20}$$

where ε_{rad1} is emissivity of the enclosed surface. Therefore the boundary condition in the equation (4-14) can be rewritten as:

$$-k\frac{\partial T}{\partial|\vec{n}|}=\varepsilon_{rad1}\sigma_{SB}(T_1^4-T_2^4) \qquad \text{on } \Gamma_q \tag{4-21}$$

If we combine equations (4-14), (4-17) and (4-20) the Neumann boundary condition for the governing equations of heat transfer can be rewritten as:

$$-k\frac{\partial T}{\partial|\vec{n}|}=\overline{q}+H(T_s-T_f)+\varepsilon_{radsolid}\sigma(T_s^4-T_f^4) \qquad \text{on } \Gamma_q \tag{4-22}$$

where $\varepsilon_{radsolid}$ is the emissivity of the solid under consideration.

4.6 Static heat transfer analysis in the earlier QMIT structures

In this section, three-dimensional static thermal simulations have been used to obtain an exact temperature distribution in earlier concept of QMIT for different structures, geometries, material properties and power dissipations [59]. The effects of the most important parameters such as the distance between active device and silicon sidewalls (W_g), epoxy thermal conductivity (k_{epoxy}) and use of a heat spreader on the backside of the transistor to decrease the thermal resistance are investigated in detail.

Boundary conditions for surfaces common between air and QMIT structures are assumed to be natural convection and radiation while radiation effect has been taken into account in the natural convection with a heat transfer coefficient of H = 10 W/m^{2}K [72]. The base plate temperature is fixed at 300 K in all the simulations. Because of the symmetry only one quarter of the structures has been considered. Properties of materials involved are given in section 2.5 and different structures of the earlier concept of QMIT are described in section 1.2.2. Thermal conductivity of semiconductors used are temperature dependent leading to nonlinear simulations.

Next section presents the result of simulation for the Ka-band power GaAs-FET used in the earlier QMIT. Different structures are compared in section 4.6.2. Section 4.6.3 and 4.6.5 cover the effects of W_g and electroplated backside heat spreader, respectively. To compare the results with standard GaAs-MMICs, thermal simulation for the same transistor in two different structures of GaAs-MMICs are performed in section 4.6.6.

4.6.1 Simulation result for the power GaAs-MESFET used

A 16 fingers Ka-band power GaAs-MESFET with a maximum power dissipation of 1.4 W and a gate length of 0.25 μm is used in all simulations. The total gate periphery of the transistor is 800 μm.

To have an idea about the temperature distribution of a wire bonded transistor on a standard test-fixture with natural convection and compare it with the earlier QMIT structure and to check the transistor model, simulation for the transistor alone on a perfect heat sink has been performed. In this simulation it is assumed that the power is dissipated uniformly under the gate, which results in a heat flux of 7E9 W/m^2 in the gate region. The results from the simulation are shown in Fig. 4-3 and are in an excellent agreement with the manufacturer's data sheet specs for the transistor. The maximum temperature is 447.7 K.

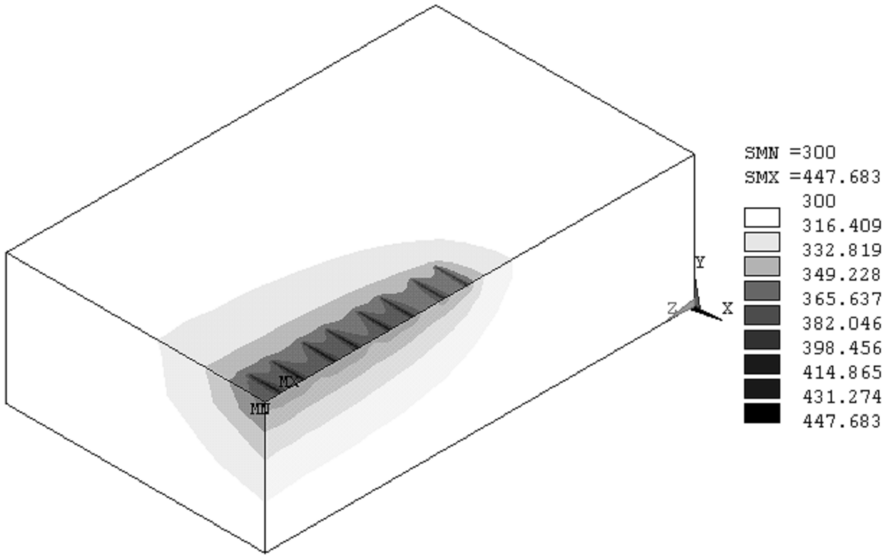


Figure 4-3: Simulation result for a quarter of Ka-band GaAs-MESFET on a perfect heat sink with a power dissipation of 1.4 W. The gray levels show the temperature distribution in Kelvin.

4.6.2 Simulation results for different structures

Results of the simulations for all the structures of earlier concept of QMIT without the backside heat spreader are presented in Figs. 4-4, 4-5 and 4-6. To compare these results, epoxy thermal conductivity and W_g are the same for all the structures (k_{epoxy} = 1.1 W/mK and W_g = 15 μm). Maximum channel temperature for the first (using full wet etching process), second (using full dry etching process) and third (using a combination of wet and dry etching processes) structures without using a heat spreader on the backside are 396.8 K, 381.4 K, 381.3 K respectively. As is shown, the maximum temperatures of all structures are much lower than that of the transistor in a standard hybrid circuit with natural convection and the third structure of the earlier concept of QMIT has the lowest maximum temperature. This structure is however not yet appropriate for high power applications since in practice realization of this structure is very difficult if not impossible and normally the base-plate temperature is higher than 300 K and may a transistor with a higher dissipation is used.

For electrothermal modeling of different structures of earlier concept of QMIT, the thermal resistance matrix for these structures is required which can be achieved from the temperature difference between each point on the surface of the transistor and the base-plate divided by the power dissipation of the transistor.

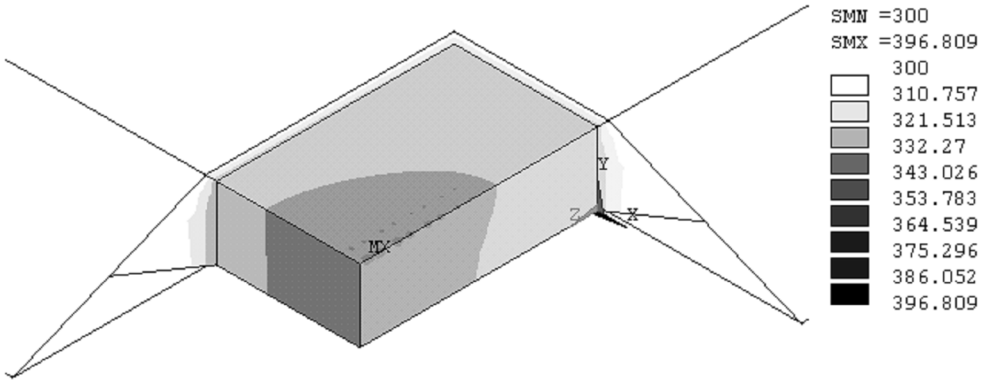


Figure 4-4: Simulation result for a quarter of the standard structure of the earlier concept of QMIT with W_g = 15 µm, k_{epoxy} = 1.1 W/mK and power dissipation of 1.4 W. Gray levels show the temperature distribution in Kelvin.

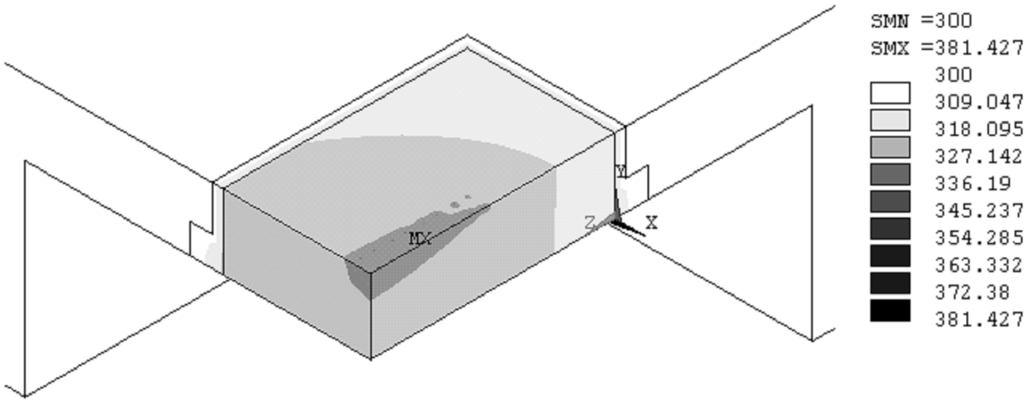


Figure 4-5: Simulation result for a quarter of the second structure of the earlier concept of QMIT with W_g = 15 µm, k_{epoxy} = 1.1 W/mK and power dissipation of 1.4 W. Gray levels show the temperature distribution in Kelvin.

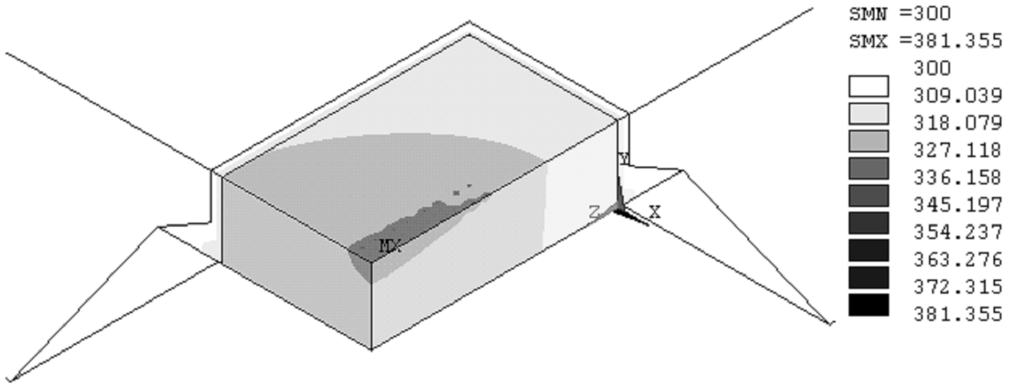


Figure 4-6: Simulation result for a quarter of the third structure of the earlier concept of QMIT with W_g = 15 µm, k_{epoxy} = 1.1 W/mK and power dissipation of 1.4 W. Gray levels show the temperature distribution in Kelvin.

4.6.4 Effect of epoxy

The distance between the active device and the substrate W_g, is limited to a maximum value of 20 µm in the technology process steps, otherwise the probability of the air-bridges breaking is high. Because of protruding defects in the scribing process of active devices by manufacturer, the minimum W_g is 5 to 10 µm but it has been shown that the standard structure with W_g = 15 µm has the minimum induced thermo-mechanical stress [3]. Fig. 4-7 shows the variations of maximum channel temperature for all the structures with W_g. As expected, the maximum temperature decreases with decreasing W_g. Fig. 4-8 illustrates the maximum channel temperature variations in all the structures as functions of k_{epoxy} for W_g = 15 µm. Again as expected, maximum channel temperatures decrease with increasing k_{epoxy}. As shown, even for the best case, k_{epoxy} = 32 W/mK, thermal resistances are 366.2 K, 364.3 K, 364.27 K for the first, second and third structures, respectively. Normally, in practice thermal conductivity of electrical nonconductive epoxy is lower than 4 W/mK. In all simulations, it is clear that the third structure is the most preferable.

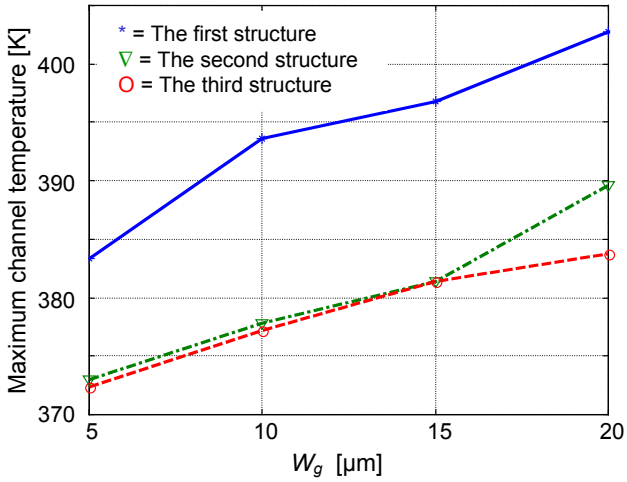


Figure 4-7: Maximum channel temperature for all structures with k_{epoxy} = 1.1 W/mK as a function of W_g.

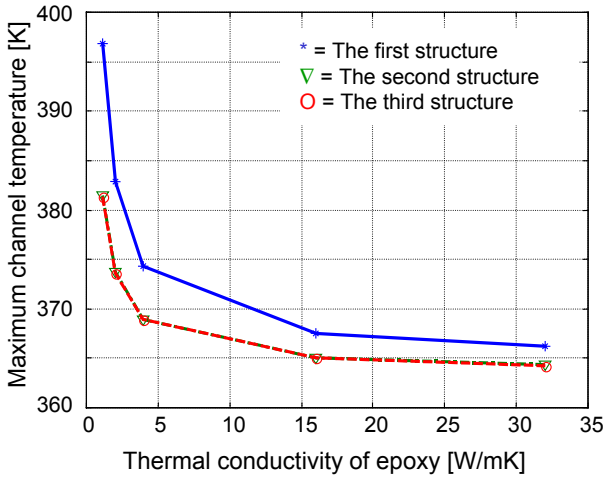


Figure 4-8: Maximum channel temperature for all structures with W_g = 15 µm as a function of k_{epoxy}.

4.6.5 Effect of heat spreader

The best thermal conductive epoxies (electrical nonconductive) have a poor thermal conductivity, so that in the earlier QMIT structure thermal resistance is high. In earlier concept of QMIT, different materials such as resins, epoxies, polyimides and metals can be used to fill the hole on the backside of the active device or to cover the backside of the active device and Si-wafer. Because of the high thermal conductivity of gold, a gold backside electroplated heat spreader could be a good solution. But as discussed in Chapter 1, thermally conductive epoxy in practice covers the backside of the transistor and is difficult to remove. As a theoretical investigation of the effect of the heat spreader thickness on the thermal resistance, simulations were performed for different thicknesses of the backside gold heat spreader. Fig. 4-9 shows the variation of the maximum channel temperature with the thickness of the heat spreader on the third structure for W_g = 15 μm and k_{epoxy} = 1.1 W/mK.

To investigate the effect of k_{epoxy} on the total thermal resistance of the third structure with the backside heat spreader, simulation for this structure for a heat spreader thickness of 400 μm and k_{epoxy} = 20 W/mK was performed. The maximum channel temperature obtained was 359.74 K, which is very near to 359.8 K for k_{epoxy} = 1.1 W/mK in the Fig. 4-9. From this result one can conclude that with a 100 μm thick backside heat spreader, most of the total thermal resistance is related to the thermal resistance inside of active device and a thicker heat spreader of higher thermal conductivity of epoxy has no significant effect. Fig. 4-10 shows the simulation results for the optimum structure of the earlier concept of QMIT.

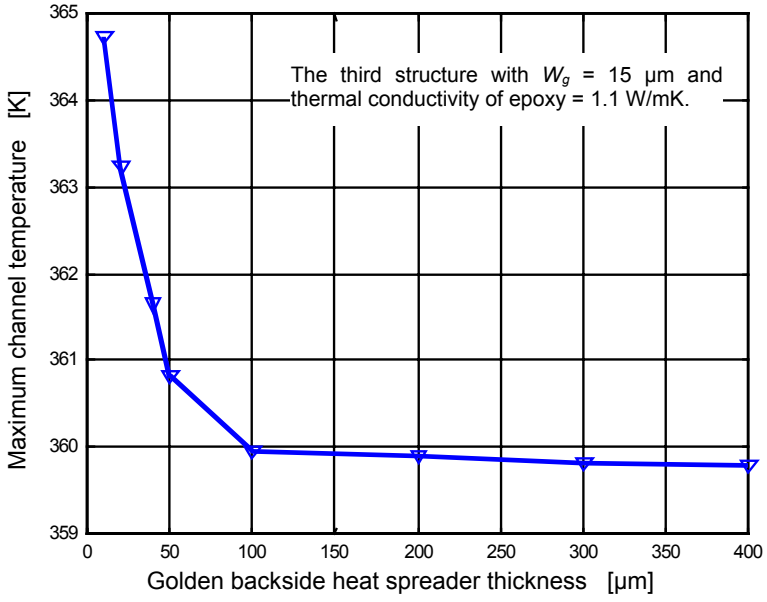


Figure 4-9: Maximum channel temperature in the third structure of the earlier concept of QMIT as a function of backside heat spreader thickness.

4.6.6 Comparison of the optimum structure with standard GaAs-MMICs

To compare the thermal characteristics of the earlier concept of QMIT and standard GaAs-MMICs, the simulation for the same active device and the same substrate thickness in a GaAs-MMIC has been performed. Fig. 4-11 illustrates the result of the simulation. In this situation maximum channel temperature is 361.98 K, which is higher than that of the third structure in Fig. 4-10.

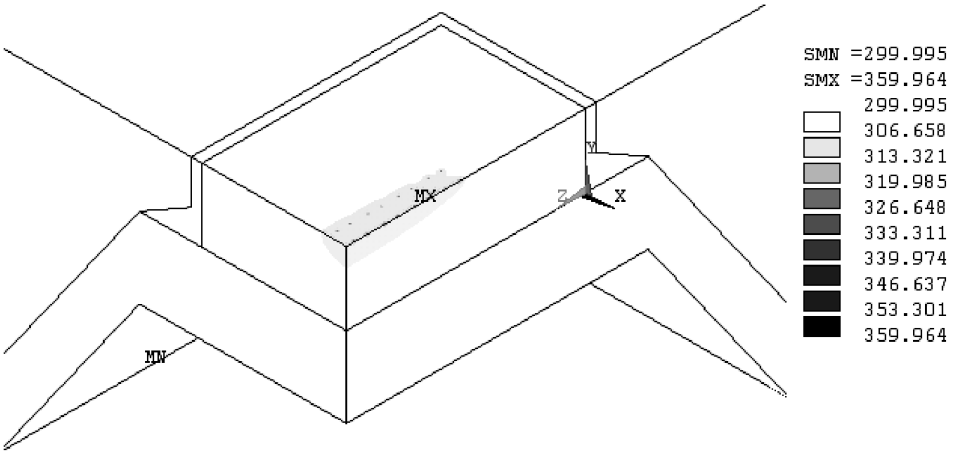


Figure 4-10: Temperature distribution in the third structure of the earlier concept of QMIT with W_g = 15 µm, k_{epoxy} = 1.1 W/mK and a 100 µm golden backside heat spreader in Kelvin.

In standard GaAs-MMICs, the substrate is normally thinned up to 100 µm using mechanical or chemical processes to achieve a lower thermal resistance. Fig. 4-12 shows the result of simulation for the same transistor in a thinned GaAs-MMIC. It is shown that the earlier QMIT structure with a thick Si-substrate and a gold backside heat spreader has approximately the same thermal resistance of a standard thinned GaAs-MMIC structure.

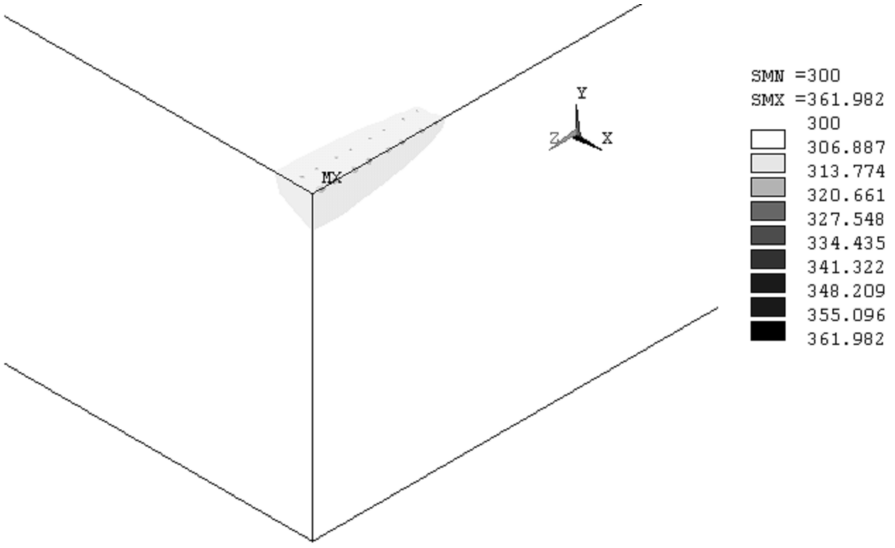


Figure 4-11: Simulation result for the same transistor used in the earlier concept of QMIT in a GaAs-substrate with thickness of 375 µm in Kelvin.

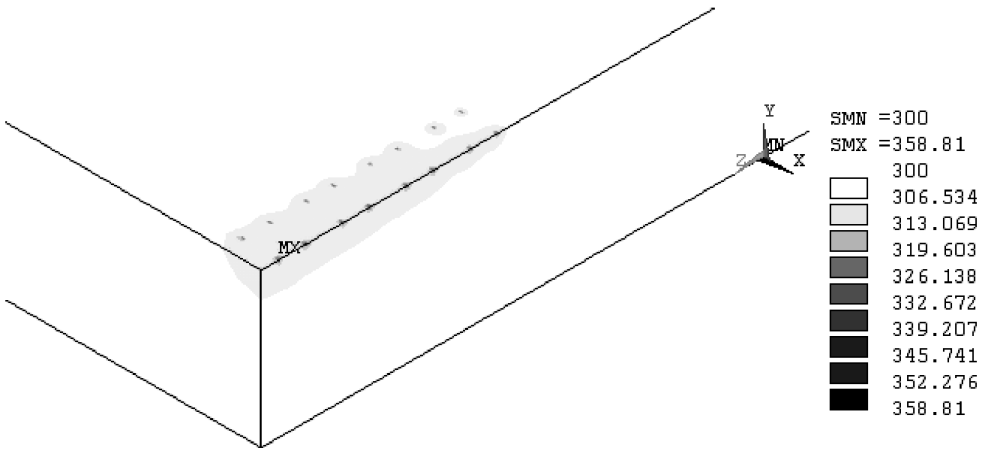


Figure 4-12: Simulation result for the same transistor used in the earlier concept of QMIT in a thinned GaAs-substrate with thickness of 100 μm in Kelvin.

4.7 Static heat transfer analysis in the enhanced QMIT structure

In this part, static heat transfer properties of the enhanced QMIT structure have been investigated [57]. To compare the thermal properties of the structure regardless of the transistor gate layout, a thermal resistance concept is defined. In all the simulation the same transistor in subsection 4.6.1 is implemented.

Fig. 4-13 shows the temperature distribution in the enhanced QMIT structure with 15 μm gap between GaAs-chip and silicon side-walls (W_g) and a 10 μm thick electroplated gold layer. In comparison to the results for the transistor on a perfect heat sink (Fig. 4-3), a significant decrease in the maximum temperature is depicted. As is shown, a thin layer of gold is adequate for low and medium power applications.

Fig. 4-14 illustrates the maximum temperatures for the enhanced QMIT with W_g of 15 μm as a function of electroplated gold layer thickness. The curves imply that most of the thermal resistance results from the layout of the gate on the transistor. For a better investigation of the thermal properties of the structure ignoring this effect, a uniform 1 W power dissipation has been applied to the whole surface of the transistor. The resulting maximum temperature difference from the base-plate temperature indicates the thermal resistance of the structure. Fig. 4-15 shows the thermal resistance of the new generation technology as electroplated gold layer thickness. The structure with a 200 μm thick electroplated gold layer in the backside of the transistor gives a good thermal resistance of 11.2 K/W which mostly relate to the thermal resistance of the active device itself.

As was mentioned in Chapter 3, there are two circuit realization methods in the new structure of QMIT, coplanar and microstrip circuit realizations. Although with a good

geometrical design of the coplanar waveguide and polyimide spin on layer, a backside metal can be used without significant effect on the electrical characteristics of the packaging, diamond-filled ploymide can be used to fill the hole in the backside of the transistor. If it is assumed that the diamond-filled polyimide mixture has a thermal conductivity of 1000 W/mK, the structure gives an excellent thermal resistance of less than 8.5 K/W.

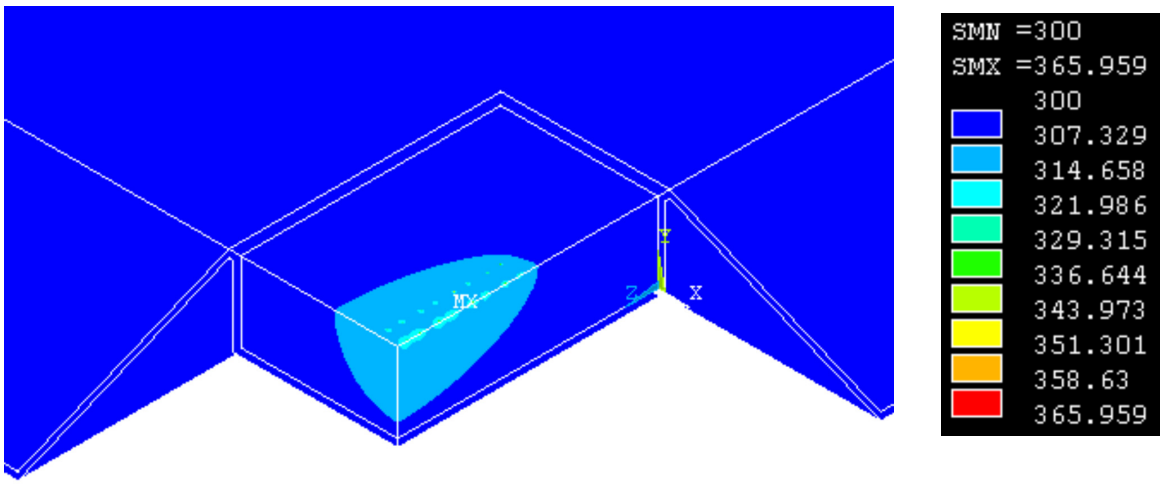


Figure 4-13: Temperature variations for the Ka-band power GaAs-MESFET in the enhanced QMIT in Kelvin.

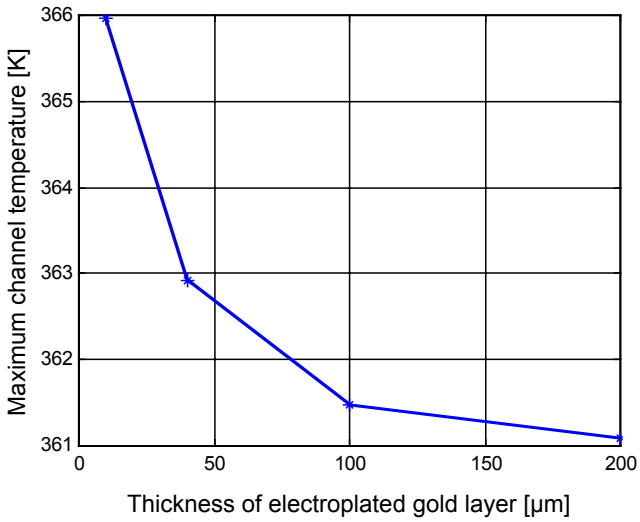


Figure 4-14: Maximum temperature in the enhanced QMIT structure as a function of the electroplated gold layer thickness. W_g = 20 µm.

4.7.1 Comparison of the hottest points in the earlier and enhanced QMIT

Figs. 4-7 and 4-8 show the simulation results for practically possible structures of the earlier concept of QMIT. Although the effect of a gold electroplated heat spreader has been described in subsection 4.6.5 and calculations for the per-assumed optimum model

have been performed, as mentioned, it is practically almost impossible to realize. Actually these simulations confirmed the requirement of a practical fabrication process such as the enhanced QMIT [61].

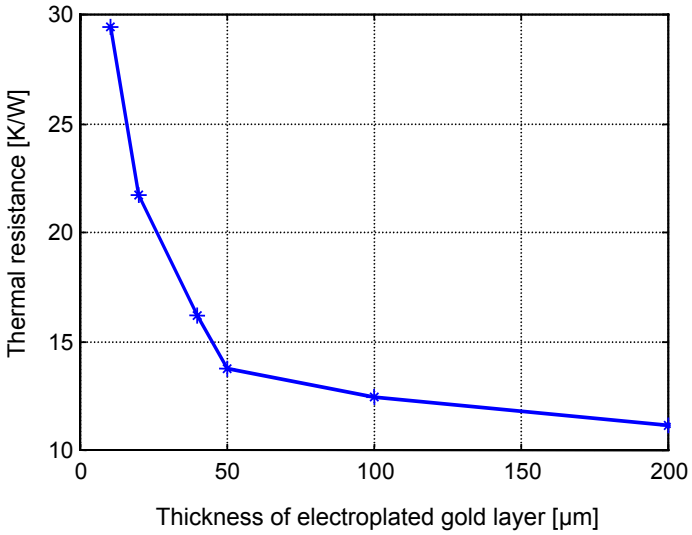


Figure 4-15: Thermal resistance of the enhanced QMIT structure as a function of electroplated gold layer thickness. W_g = 20 µm.

From Figs. 4-7 and 4-14 superiority of the enhanced QMIT in comparison to the earlier concept can clearly be understood. The worst-case maximum temperature of the enhanced QMIT (for 10 µm thick electroplated gold layer) is more than 40 K lower than that of the standard structure of the earlier concept of QMIT with the same W_g of 20 µm. It should be mentioned that most of thermal resistance in the enhanced QMIT is related to the geometrical dimensions of the gate of the transistor and the poor thermal conductivity of GaAs. Fig. 4-15 shows that extremely low thermal resistances for the enhanced QMIT are achievable. These low thermal resistances not only increase the reliability and lifetime of the embedded active device, but also can improve its electrical performance such as noise figure, power gain and maximum power rating.

4.8 Thermal imaging of microwave power GaAs-FET with scanning thermal nano-probe

It is well known that the temperature distribution measurement on electronic active devices is not only useful for investigation of reliability and lifetime of the device and its packaging, but also for device modeling and characterization which is crucial in microwave and millimeterwave design. For example, the power GaAs-MESFET is one of the common components in microwave integrated circuits. The volumetric heat generation rate inside such a small semiconductor device can be expected to be very high since the device operating power cannot be lower than a certain level. The resulting

increase in the device local temperature can significantly affect the device electrical characteristics and reliability.

In addition to thermal imaging using scanning probe microscopy (SPM), there are three other common methods used to measure temperature on GaAs devices, and none is perfect. These methods are infrared microscope, liquid crystal, and electrical diode drop [128].

Among the three methods, the infrared microscope method is the most expensive and sophisticated. Commercial instruments with computerized control and graphic displays are available. The microscope focuses infrared emission from the surface of the die onto an infrared sensor, and the temperature is determined. In this method knowledge of emissivity of the surface is required unless the device is perfectly black. Computerized commercial instruments are able to determine emissivity in a separate procedure in which the infrared radiance is recorded at several temperatures while the overall device is heated, but unpowered so that its temperature is uniform and known. The instrument in subsequent measurements of the die then uses this calibration with power applied to it.

These commercial instruments can produce pixel-by-pixel map of temperature over the surface of the powered die. Accuracy of temperature determination can be ±1 °C. The major limitation of the infrared measurement is spatial resolution. Infrared wavelength limits resolution to about 15 μm. The lateral dimension of the heat sources in GaAs devices, such as channel of FETs, can be on the order of 1 μm or even less. In other words infrared instrument records an average temperature over the area of its minimum resolution, which will be less than the true peak temperature.

The second method is the use of liquid crystals to achieve temperature on GaAs devices. Liquid crystals are substances in which crystalline orientation changes from random to aligned at a well-defined temperature, called the transition temperature. The resulting optical properties (transmission or reflectance of polarized light) change dramatically at this temperature. Different liquid crystals have different transition temperatures.

To measure the temperature on the device, a liquid crystal substance with a known transition temperature is deposited on the device, normally applied by hand with a brush, and left to dry. Then the device is slowly powered up or heated until the phase transition occur, this can easily be seen in an optical microscope using polarized light. The advantage of this method is resolution, which is as good as the best optical microscopes. This method is well suited to find the hottest spots on the device. A limitation of the method is the restriction to specific transition temperatures of available liquid crystal materials. However, liquid crystal materials with a wide range of transition temperatures are commercially available, encompassing the range between 30 and 250 °C.

The third method used to determine temperature is electrical and based on the fact that the forward voltage characteristic of any diode is temperature-dependent. Normally, to determine temperature, the diode is biased with a constant current (forced bias) and the voltage across the diode is measured.

The diode used for temperature sensing should first be characterized over the temperature range of interest. In the GaAs-FETs, one can use the Schottky gate diode as the temperature sensing diode. To measure temperature on the GaAs-FET, the FET can be run under operating dc bias and perform the diode measurement in a time brief enough to prevent significant, additional heating by the diode measurement or cooling from cessation of FET operation. Nevertheless, the method is somewhat awkward because of initial characterization process and problems with reproducibility. None of these three is ideal and therefore are sometimes used in combination.

In this section, the application of a new thermal nano-probe based on the changes of electrical resistivity of a nanometer-sized filament with temperature is presented for the thermal imaging of microwave power active devices. The filament is integrated into a piezoresistive type cantilever for an atomic force microscopy (AFM). The novel thermal probe has a spatial resolution better than 80 nm and a thermal resolution of the order of 10^{-3} K [93]. The measurement has been successfully performed on a 30 finger GaAs-MESFET with a maximum power dissipation of 2.5 W. The microwave transistor has been implemented in a circuit in such a way to prevent the undesired microwave oscillations. In this case the power dissipation is equal to the dc power input. The near-field measurement has been compared with a far-field measurement and nonlinear three-dimensional finite element simulation. A good agreement between simulations and measurements is achieved [49].

4.8.1 Experimental and calculated results

The transistor is implemented in a standard microwave test-fixture on an aluminum heat sink. Using two resistive loads at the drain and source of a UHF-band power GaAs-MESFET, the undesired oscillations have been prevented. Fig. 4-16 illustrates the top view of the GaAs-transistor. The black square represents the measurement window for the near-field measurements.

Fig. 4-17 predicts the result of the near-field measurement using the thermal nano-probe on the surface of the transistor for V_{ds} = 7 V and I_d = 283 mA.

To determine the position of the measurement on the transistor for every measurement, a two-dimensional surface profile mapping has been performed on the same measurement window. Figs. 4-18 and 4-19 illustrate the topographic image and cross-section view of the 15th gate region in the measurement window, respectively.

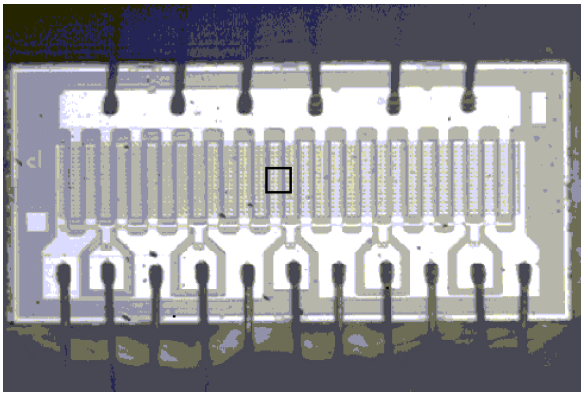


Figure 4-16: Top view of the UHF-band power KGF1305T GaAs-MESFET from OKI.

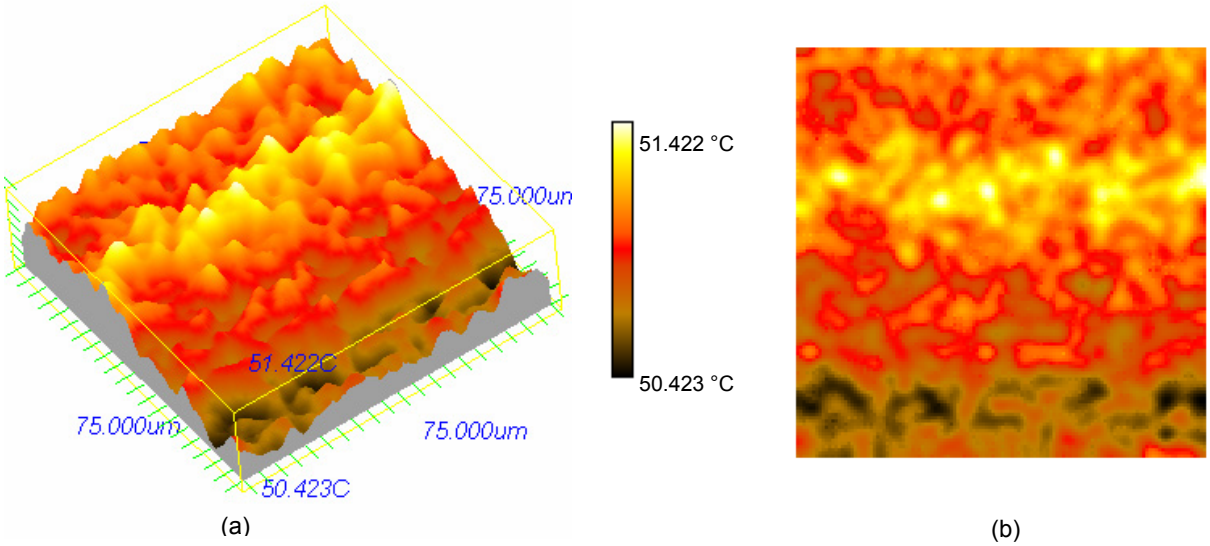


Figure 4-17: Thermal image (near-field measurement) of the 30 fingers UHF-band power GaAS-MESFET for bias point of I_{ds} = 289 mA and V_{ds} = 7 V using the novel thermal nano-probe implemented in an AFM cantilever. The corresponding measurement window is shown in Fig. 4-16. (a) Three dimensional view of the thermal imaging. (b) Top view of the thermal imaging.

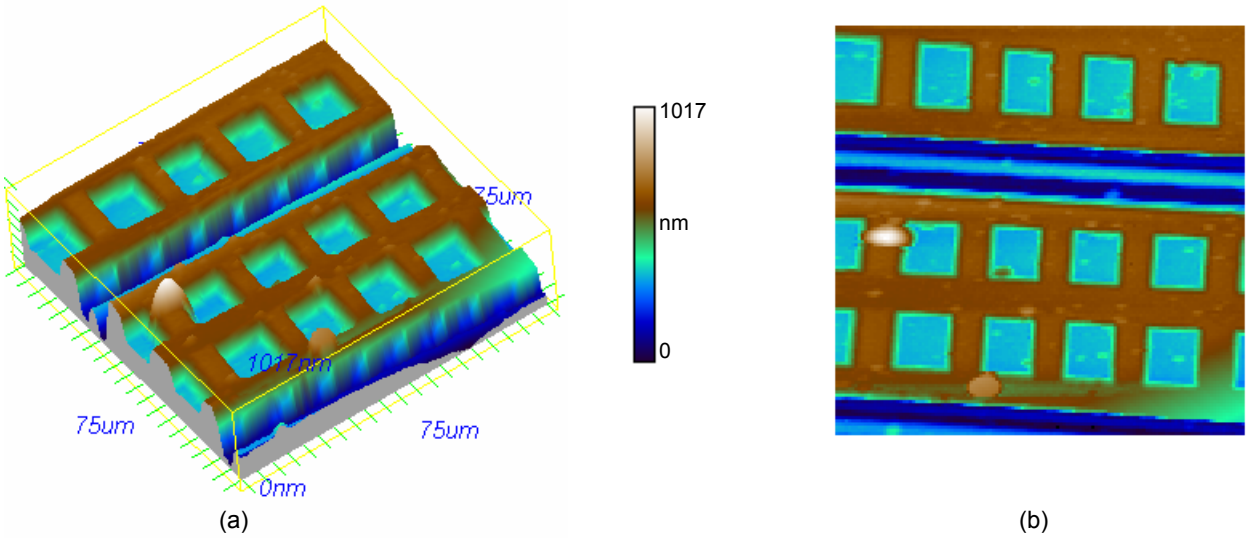


Figure 4-18: (a) Corresponding topographic image of the thermal imaging in Fig. 4-17 (a). (b) Corresponding topographic image of the thermal imaging in Fig. 4-17 (b).

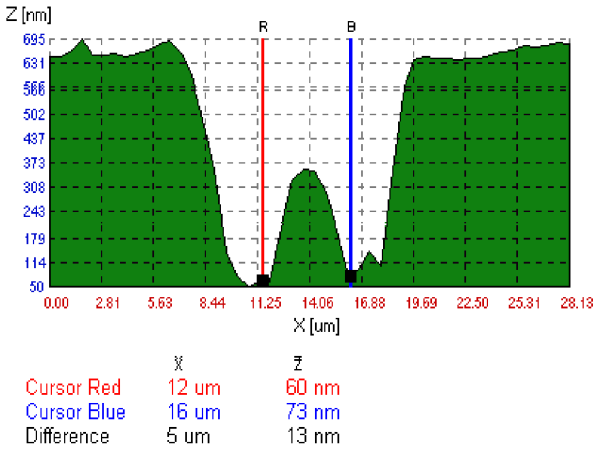


Figure 4-19: Cross-section view of the 15th gate region in Fig. 4-18(a).

Cross-section of the drain, gate and source of the mid-point of the transistor is shown in Fig. 4-19. The distance between the drain and gate in the left-hand side is larger than that of source-gate in the right-hand side. Fig. 4-17 shows the maximum temperature is on the 15th gate a little intended to the drain-side. Because maximum power dissipation is under the gate a little intended to the drain, the temperature on the drain and source is lower that of gate area near to the drain. The 15th gate is placed very near to the middle of the transistor and the peak of temperature on that area (at the top) is higher than the peak on the 14th gate (at the down), which is farther from the middle.

Fig. 4-20 illustrates far-field temperature measurement on the thirty finger UHF-band power GaAs-MESFET for I_{ds} = 283 mA and V_{ds} = 7 V. Because spatial resolution in the infrared camera measurement is limited to about 15 μm, hot regions around the gate fingers are not detected. On the other hand for an infrared temperature measurement knowledge of emmisivity of the surface is required and that is why there is a small difference between the far-field and near-field measurements.

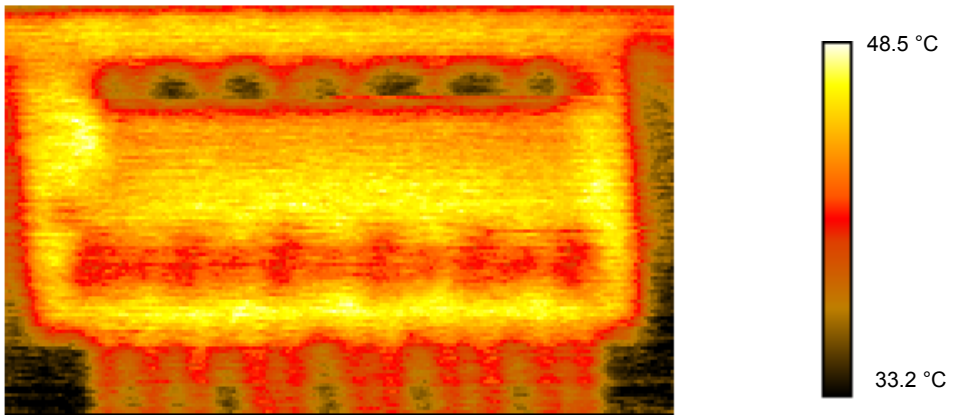


Figure 4-20: Infrared thermal imaging (far-field measurement) of the 30 fingers UHF-band power GaAS-MESFET for bias point of I_{ds} = 283 mA and V_{ds} = 7 V.

A three-dimensional nonlinear finite element temperature simulator has been used to calculate the temperature variations in the GaAs-transistor. In this simulation, a simple model similar to the model used in [124] is implemented. Percentages of the dissipated power at the gate region in this model are shown in Fig. 4-21. Heat sources are assumed to be uniform heat fluxes on the areas shown in Fig. 4-21. Because of symmetry the simulation is performed for a quarter of the power GaAs-MESFET.

Fig. 4-22 depicts the simulation result for a power dissipation of 2.03 W (V_{ds} = 7 V and I_{ds} = 290 mA). For the simulation the base-plate temperature of 300 K was assumed. The temperature of aluminum plate under the transistor during the measurement was 22.5 °C. If we assume the temperature on the button of transistor is 1 °C warmer, the predicted peak of temperature for 15th gate (maximum channel temperature) will be 51.5 °C, which is in excellent agreement with the near-field measurement shown in Fig. 4-17. The simulation result in Fig. 4-22 shows that the simple model used can predict the maximum temperature very well. But because the metallization and passivating silicon-nitride on the transistor and power dissipation in the metallization have been ignored in the model, the calculated temperature distribution between the gate fingers is different from those of the far-field and near-field measurements.

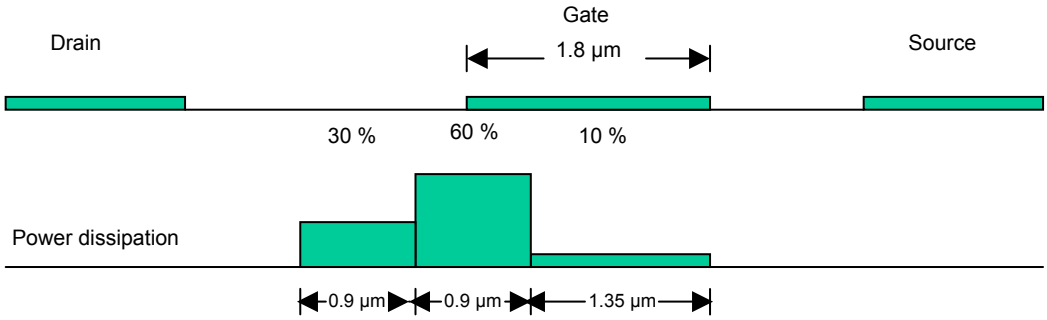


Figure 4-21: Power dissipation percentages around the gate region.

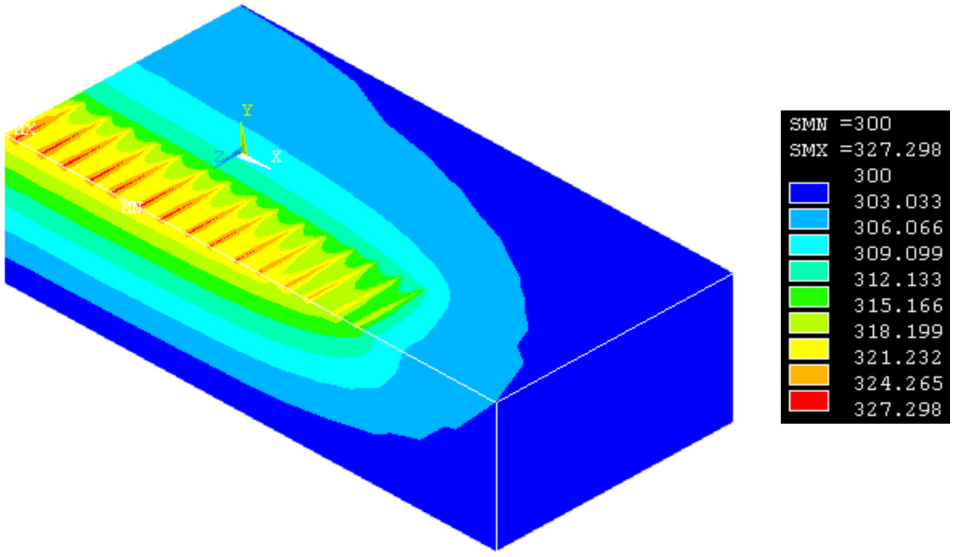


Figure 4-22: Simulation result for the UHF-band power GaAs-MESFET on a perfect heat sink with a power dissipation of 2.03 W.

4.8 Summary

Static thermal analyses for the earlier concept and enhanced QMIT structures have been carried out in detail. Brief surveys of the temperature influences on the reliability of the packaging and the electronic properties of semiconductor devices have been given. The effects of several parameters such as the properties of materials involved and different geometries in all the possible structures have been discussed in detail. Simulation results confirm an excellent thermal resistance for the enhanced QMIT structure and highlight its superiority to the earlier concept of QMIT structures. This leads to longer lifetime, higher reliability and better performance of the packaging.

The first successful application of a thermal nano-probe for two-dimensional thermal imaging on microwave GaAs-FETs has been presented and compared with far-field measurements and calculated results. A remarkable agreement among the calculated results and the far and near-field measurements and calculated results was demonstrated.

Chapter 5

Thermo-mechanical Stress Analysis and Measurement in the Earlier Concept and Enhanced QMIT Structures

5.1 Introduction

It is well known that thermo-mechanical stress not only affects the reliability and lifetime of the packaging but also the device characteristics, which is crucial in microwave and millimeterwave design. Therefore, every reliability and lifetime study of an electronic packaging or reliable design and modeling of electronic devices in the packaging requires knowledge of the maximum and the variation of the induced stress in the structure.

QMIT structures are constructed from different materials with different mechanical properties. This requires a state of the art investigation to bring these material together in such a way that the maximum induced thermo-mechanical stress is well down. Since the QMIT structures are too complex to solve by analytical methods a nonlinear three-dimensional finite element structural simulator has been used for the thermo-mechanical stress calculations. To compare the calculated results with measurements, the surface profile of the silicon-wafer near to the embedded active device at different temperature conditions has been measured and compared with calculations. During the measurements, the temperature was accurately adjusted using a closed-loop system consisting of a Pt-100 temperature sensor, Peltier-element and an automatic digital current supply. An excellent agreement between calculated and measurements results under different temperatures, was found. In comparison with the earlier concept of QMIT, the results confirm a great decrease of maximum induced thermo-mechanical stress in the enhanced QMIT structure.

This chapter is dedicated to analysis and measurement of the thermo-mechanical stress in the earlier concept and enhanced QMIT structures. In the next section, the effect of mechanical stress on reliability and lifetime of the packaging is discussed. Section 5.3 describes the influence of the stress (or strain) on electronic properties of semiconductors. Sections 5.4 and 5.5 cover the thermo-mechanical stress simulations and measurements in the earlier concept and enhanced QMIT structures, respectively. The maximum induced thermo-mechanical stress in the earlier and the new concepts of QMIT have been compared in section 5.6. The chapter will be closed with a brief summary.

5.2 Effect of mechanical stress on packaging reliability and lifetime

5.2.1 Reliability overview

Reliability is understood as the probability that an item will perform its required task for a set amount of time. Reliability is ultimately a measure of the rate at which things fail and can be used to make intelligent predictions about the performance of a system. If the assumption is made that a system is operating at time $t = 0$, and a time t_f is defined as the time to failure, then it is possible to define the complementary failure and reliability rates as [63], [109]:

$$F(t) \equiv P\{ t_f \leq t\} \tag{5-1a}$$

$$R(t_f) \equiv P\{ t_f > t\} = 1 - F(t) \tag{5-1b}$$

where

$P\{a\}$ = The probability that the event *'a'* will occur

$F(t)$ = The probability that a system fails in $[0,t]$

$R(t)$ = The probability that a system survives until time t

From probability theory, it is known that $F(t)$ and $R(t)$ are non-negative and that $F(0) = 0$ and $F(\infty) = 1$, since all parts will eventually fail. A good measure of reliability in the interval $(t, t+\Delta t]$ is the probability that a system does not fail in the interval $(t, t+\Delta t]$, given that it has not failed by time t, which is written as:

$$P\{t_f \notin (t, t+\Delta t] \mid t_f > t\} \tag{5-2}$$

this quantity is known as the conditional reliability of a system of age t, represented by the expression $R(\Delta t \mid t)$ and is related to $R(t)$ by:

$$R(\Delta t \mid t) = \frac{R(t + \Delta t)}{R(t)} \tag{5-3}$$

It should be apparent that $R(\Delta t \mid t) = R(\Delta t)$, since $R(0) \equiv 1$, as defined earlier.

5.2.1.1 Reliability measure

The main challenge of reliability analysis is to quantify a system's reliability. This can be done in a number of ways by utilizing some important probability principles. When data from a reliability test is first collected, it is plotted as failure versus time. This plot is usually smoothened by fitting the reliability data to established reliability models such as Weibull, normal, and lognormal distributions. After this is done, the probability density function (PDF), is determined [109].

5.2.1.1(A) Probability Density Function

The measure of the probability of failure around a point in time, *t*, is represented by the probability density function of f_p:

$$f_p(t) \equiv \frac{dF(t)}{dt} = \lim_{\Delta t \to 0} \frac{F(t+\Delta t) - F(t)}{\Delta t} \tag{5-4}$$

$f_p(t)$ is, for a small Δt, approximately equal to the probability of failure in the time interval $[t, t+\Delta t]$. Once $f_p(t)$ is found by whatever approximation is made for the failure function, one can determine the failure rate, which is the same as the reliability rate.

5.2.1.1(B) Failure Rate

The instantaneous failure rate is defined as:

$$\lambda(t) \equiv \lim_{\Delta t \to 0} \frac{P\{t < t_f \le t + \Delta t \mid t_f > t\}}{\Delta t} \tag{5-5a}$$

which can be rewritten as:

$$\lambda(t) \equiv \lim_{\Delta t \to 0} \frac{P\{t < t_f \le t + \Delta t\}}{\Delta t P\{t_f > t\}} \Rightarrow \tag{5-5b}$$

$$\lambda(t) \equiv \frac{1}{R(t)} \lim_{\Delta t \to 0} \frac{F(t+\Delta t) - F(t)}{\Delta t} = \frac{f_p(t)}{R(t)} \tag{5-5c}$$

since $\lambda(t) = f_p(t)/R(t)$, it is also possible to define $\lambda(t)$ by:

$$\lambda(t) = -\frac{1}{R(t)} \frac{dR(t)}{dt} = -\frac{d}{dt}(\ln R(t)) \tag{5-6}$$

thus, given that $R(0) = 1$, it is possible to determine $R(t)$ as a function of λ as:

$$R(t) = e^{-\int_0^t \lambda(x)dx} \tag{5-7}$$

So, if λ is constant for a period of time, the reliability function is:

$$R(t) = e^{-\lambda t} \tag{5-8}$$

which is the exponential model of reliability. However for most systems, the failure rate is not constant with time. In fact, the change of λ with time becomes one of the most important reliability measures. A decreasing λ indicates improvement with time, while an increasing λ indicates wear-out and a reduction in reliability over time.

5.2.1.1(C) The Bathtub curve

By looking at a plot of failure rate over time, it is possible to derive substantive information about reliability. From experience in the semiconductor industry, it has been shown that most devices, including MEMS, have a failure rate $\lambda(t)$ shown in Fig. 5-1 [50]. This model is known as the Bathtub curve and was initially developed to model the failure rates of mechanical equipment, but has since been adopted by the semiconductor industry.

The bathtub curve can be reduced to three regions of reliability. The failure rate of a successful part is initially high and falls off as latent defects cause devices to fail until a time, t_{infant}, at which point the failure rate levels off. A decreasing failure rate will typically justify initial testing and burn-in. The purpose of the burn-in procedure is to operate the devices for some time during which most of the devices that are subject to infant mortality failure actually fail. The failure rate remains constant for a period of time specified as the useful life, t_{useful}. Failures that occur during this period of time may be considered random and, for high-reliability operations, λ should be exceedingly small. Finally, after $t_{operation}$, devices begin to exceed their lifetime and wear-out causes the curve to rapidly increase. From ths data it is evident that t_{useful} can be defined as:

$$t_{useful} = t_{operation} - t_{infant} \tag{5-9}$$

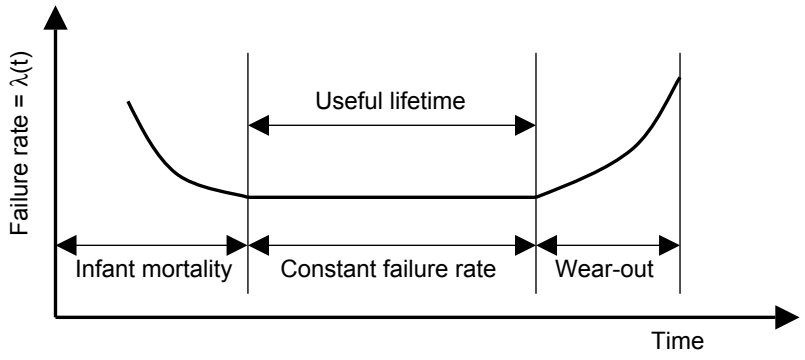


Figure 5-1: The Bathtub curve.

As indicated by the bathtub curve, manufacturers aim for the failure rate to remain fairly constant over t_{useful}, which justifies using the exponential reliability model for each part to be used in the system reliability models. The time scale is often plotted logarithmically, although the values of t_{useful} and t_{infant} are rarely well defined. Consequently, every manufacturer has his own specific test and burn-in procedure to maximize the reliability of each product.

5.2.1.1(D) Predicting time to failure

Sometimes it is desirable to discuss the average time to failure instead of the probability of failure. This value is known as the mean time to failure (MTTF) and is defined as:

$$MTTF \equiv \int_0^\infty tf(t)dt \tag{5-10a}$$

and can be written as:

$$MTTF = \int_0^\infty R(t)dt \tag{5-10b}$$

Once a device is operational a more useful value is the mean residual life, or MRL. This quantity is derivable as:

$$MRL(t) = \frac{1}{R(t)} \int_0^\infty R(T)dT \tag{5-11}$$

Noted that $MRL(0) = MTTF$.

5.2.1.1(E) Failure rate units

Since, for most systems, $\lambda(t)$ is a small quantity, special units are used to describe reliability. The failure rate is given as the number of units failing per unit time. In normal operation, this number when expressed as the number of devices failing per unit time, is a fraction of a percent. To make this function more useful, the values are scaled to a more meaningful time frame. Thus $\lambda(t)$ is expressed as tenths of a percent of devices failing per 10^6 hours or as the total number of devices failing in 10^9 hours. This latter quantity is known as the failure in time, or FIT, and is the common unit of reliability defined as:

$$1 \text{ FIT} = \frac{1 \text{ failure}}{10^9 \text{ device hour}} \tag{5-12}$$

A FIT is an approximate rate measure over the useful life of a part. Assuming a constant failure rate and a given the bathtub curve model, the FIT rate = $\lambda/10^9$, where λ is the constant failure rate shown in Fig. 5-1.

5.2.1.2 Failure

The time dependence of reliability, R, and Failure, F, are complimentary, so that the both rates are equal to the failure rate, λ. In order to accurately study packaging reliability, the nature of failures must be quantified.

Failure may be separated into two distinct categories [109]:

(1) Degradation failure, which consist of device operation departing far enough from normal conditions that the component can no longer be trusted for reliable operation

(2) Catastrophic failures, which are, as the name implies, the complete end of device operation.

Failures occur when the stresses on a device exceed its strength. In order for a device to be classified as highly reliable, it must meet some basic criteria. The most significant of these is that a device cannot exhibit a dominant failure mechanism. This ensures that there is no inherent design flaw that prohibits long-term reliable device operation. In order to make this assessment, the failure mechanisms with a device must be understood [128].

A critical part of understanding the reliability of any system comes from understanding the possible ways in which the system may fail. There are many different modes and mechanisms of failure in the RF/microwave packaging but this subsection is dedicated to describe how mechanical stress affects the reliability.

5.2.2 Mechanical fracture

Mechanical fracture is defined as the breaking of a uniform material into two separate sections. This will usually lead to the catastrophic failure of a package or a device, although there are some structures that will have more moderate performance degradations. No matter what the actual outcome, any fracturing is a serious reliability concern. There are three types of fractures: ductile, brittle, and intercrystalline fracture.

Ductile fracture, as the name implies occurs in ductile materials. It is characterized by almost uninterrupted plastic deformation of a material. It is usually signified by the necking, or extreme thinning, of a material at one specific point. Brittle fracture occurs along crystal planes and develops rapidly with little deformation.

Intercrystalline fracture is a brittle fracture that occurs along grain boundaries in polycrystalline materials, often beginning at a point where impurities or precipitates accumulate. For MEMS and for micromachined structures such as QMIT, the latter two types of fracture are more common. To understand the actual causes of fracture and the methods for predicting it, several terms must be defined [109].

5.2.2.1 Definitions

Mechanical failure in a crystal lattice occurs when an applied stress exceeds the failure stress of the structure. Stresses are separated into the two categories of normal and shear stress. Normal stress is defined as stress perpendicular to a plane in a material, while shear stress occurs parallel to a plane, as shown in Fig. 5-2. In solid materials, stress is linearly related to a concept called strain, which is the fractional elongation of a material. The proportionality constant between stress and strain is, for small normal loads, called the modulus of elasticity, or Young's modulus. The actual deformation of a cubic volume will depend upon all the stresses applied to it:

$$\begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \tau_{xy} \\ \tau_{xz} \\ \tau_{yz} \end{bmatrix} = \begin{bmatrix} \hat{E}_{11} & \hat{E}_{12} & \hat{E}_{13} & \hat{E}_{14} & \hat{E}_{15} & \hat{E}_{16} \\ \hat{E}_{21} & \hat{E}_{22} & \hat{E}_{23} & \hat{E}_{24} & \hat{E}_{25} & \hat{E}_{26} \\ \hat{E}_{31} & \hat{E}_{32} & \hat{E}_{33} & \hat{E}_{34} & \hat{E}_{35} & \hat{E}_{36} \\ \hat{E}_{41} & \hat{E}_{42} & \hat{E}_{43} & \hat{E}_{44} & \hat{E}_{45} & \hat{E}_{46} \\ \hat{E}_{51} & \hat{E}_{52} & \hat{E}_{53} & \hat{E}_{54} & \hat{E}_{55} & \hat{E}_{56} \\ \hat{E}_{61} & \hat{E}_{62} & \hat{E}_{63} & \hat{E}_{64} & \hat{E}_{65} & \hat{E}_{66} \end{bmatrix} \begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{xy} \\ \varepsilon_{xz} \\ \varepsilon_{yz} \end{bmatrix} \tag{5-13a}$$

where σ is normal stress, τ is shear stress, ε is strain and $\hat{E}$ is Elastic Modulus.

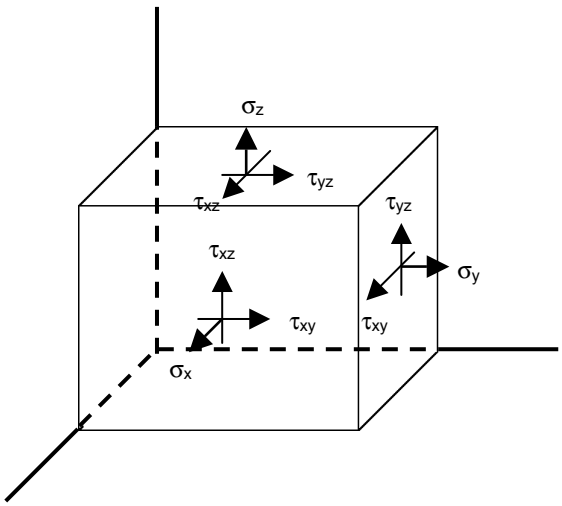


Figure 5-2: Generalized stress states on a three-dimensional unit cube.

One important aspect of this tensor is that $\hat{E}_{ij} = \hat{E}_{ji}$, so that there are actually only 21 independent constants. Further simplifying this effect is the internal symmetry of most crystals. In cubic crystals, such as Si and GaAs, the tensor reduces to:

$$\begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \tau_{xy} \\ \tau_{xz} \\ \tau_{yz} \end{bmatrix} = \begin{bmatrix} \hat{E}_{11} & \hat{E}_{12} & \hat{E}_{12} & 0 & 0 & 0 \\ \hat{E}_{12} & \hat{E}_{11} & \hat{E}_{12} & 0 & 0 & 0 \\ \hat{E}_{12} & \hat{E}_{12} & \hat{E}_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \hat{E}_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \hat{E}_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \hat{E}_{44} \end{bmatrix} \begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{xy} \\ \varepsilon_{xz} \\ \varepsilon_{yz} \end{bmatrix} \tag{5-13b}$$

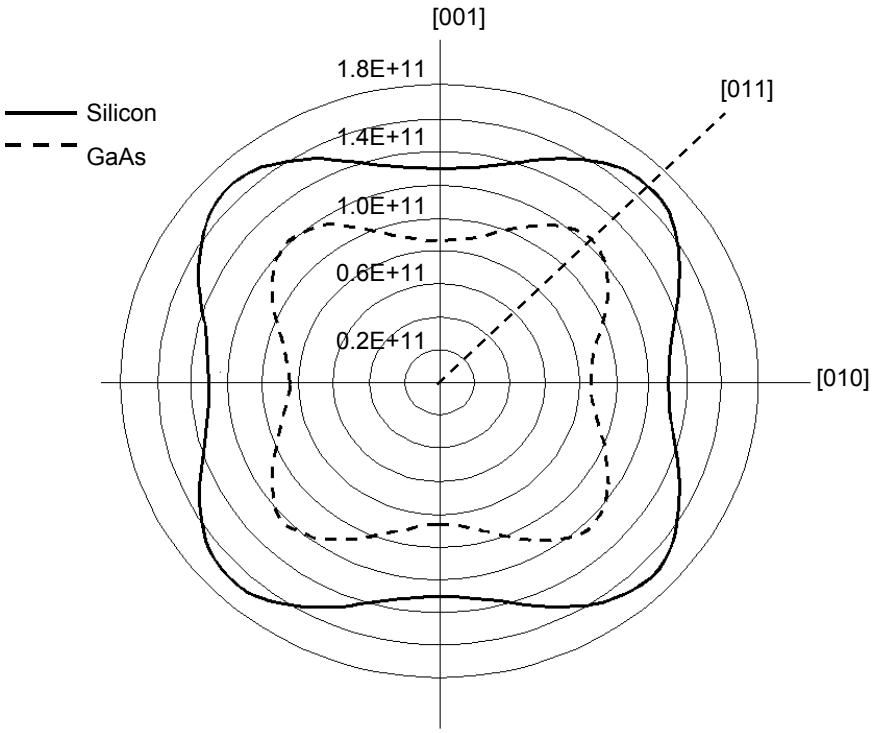


Figure 5-3: Young's modulus as a function of crystalline orientation for Si and GaAs along the <100> axis.

One of the difficulties in using equation 5-13b is that, in an anisotropic crystal, the elastic modulus will vary with crystalline orientation. To account for this variation with the crystal orientation a plane modulus is defined:

$$\hat{E}_{[hkl]} = \frac{\sigma_{[hkl]}}{\varepsilon_{[hkl]}} \tag{5-14}$$

The modulus of a crystalline plane is related to the elastic constants in equations (5-13), through:

$$\hat{E}^{-1}(\theta,\phi,\psi) = C_{11} - 2(C_{11} - C_{12} - 0.5C_{44})(l_1^2 l_2^2 + l_2^2 l_3^2 + l_1^2 l_3^2)) \tag{5-15}$$

where

$$C_{11} = \frac{\hat{E}_{11} + \hat{E}_{12}}{(\hat{E}_{11} + 2\hat{E}_{12})(\hat{E}_{11} - \hat{E}_{12})}$$

$$C_{12} = \frac{-\hat{E}_{12}}{(\hat{E}_{11} + 2\hat{E}_{12})(\hat{E}_{11} - \hat{E}_{12})}$$

$$C_{44} = \frac{1}{\hat{E}_{44}}$$

θ, ϕ, ψ = Euler's angles formed between the <100> axis and an arbitrary <hkl> axis

l_1, l_2, l_3 = the direction cosines defined by the following matrix

$$\begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} = \begin{bmatrix} \cos(\theta)\cos(\phi)\cos(\psi) - \sin(\phi)\sin(\psi) & \cos(\theta)\sin(\phi)\cos(\phi) - \sin(\phi)\sin(\psi) & -\sin(\theta)\cos(\psi) \\ -\cos(\theta)\cos(\phi)\cos(\psi) - \sin(\phi)\sin(\psi) & -\cos(\theta)\sin(\phi)\cos(\psi) - \sin(\phi)\sin(\psi) & \sin(\theta)\sin(\psi) \\ \cos(\theta)\cos(\phi) & \cos(\theta)\cos(\phi) & \cos(\theta) \end{bmatrix}$$

The modulus of Si and GaAs as a function of crystalline orientation is shown in Fig. 5-3 [109].

In common nomenclature the constants, C_{11}, C_{12}, and C_{44} are called compliance coefficients. This equation reveals that the {100} planes of Si have an elastic modulus of 130 GPa, while the {110} planes have a modulus of 165 GPa. For the {111} planes, with a θ and ϕ angle of 45° and a ψ angle of 0°, the value of $\hat{E}_{\{111\}}$ is 187 GPa, which is the stiffest plane in silicon. As a result, wear effects will be most severe in the [100] direction because it has the lowest stiffness of any crystal planes in silicon. It must also be noted that, $\hat{E}_{11}$, $\hat{E}_{12}$, and $\hat{E}_{44}$ are usually defined relative to the <110> planes, while C_{11}, C_{12}, and C_{44} are generally defined relative to the <100> planes.

Poisson's ratio is also orientation dependent, with the basis vector given along with the value of the number. Poisson's ratio is normally defined in terms of the elastic compliance coefficients as ν = -C_{12}/C_{11}. If a longitudinal stress is considered in a direction that is displaced from the {100} planes by angles θ, ϕ, and ψ it has been proven that [109]

$$\nu = -\frac{C_{12} + (C_{11} - C_{12} - 0.5C_{44})(l_1^2 m_1^2 + l_2^2 m_2^2 + l_3^2 m_3^2)}{C_{11} - 2(C_{11} - C_{12} - 0.5C_{44})(l_1^2 l_1^2 + l_2^2 l_3^2 + l_1^2 l_3^2)} \tag{5-16}$$

5.2.2.2 Stress induced failure

Once the definitions of stress and strain are understood, it is possible to understand how stress leads to failure. In Fig. 5-5, the process of crystal lattice failure is illustrated through a graph of stress versus strain. As can be seen, the application of stress causes a linear increase in strain until fracture. This is a function of the brittle properties of these

materials; brittle materials deform elastically until fracture occurs. To understand the fracture tolerances of any mechanical structure one needs to determine the maximum stresses.

The maximum stress in a device usually occurs near stress risers, or concentrators. Stress concentration occurs when there is a sudden change in the cross section of a material. At these points, stress is usually non-uniformly distributed and somewhat difficult to resolve analytically.

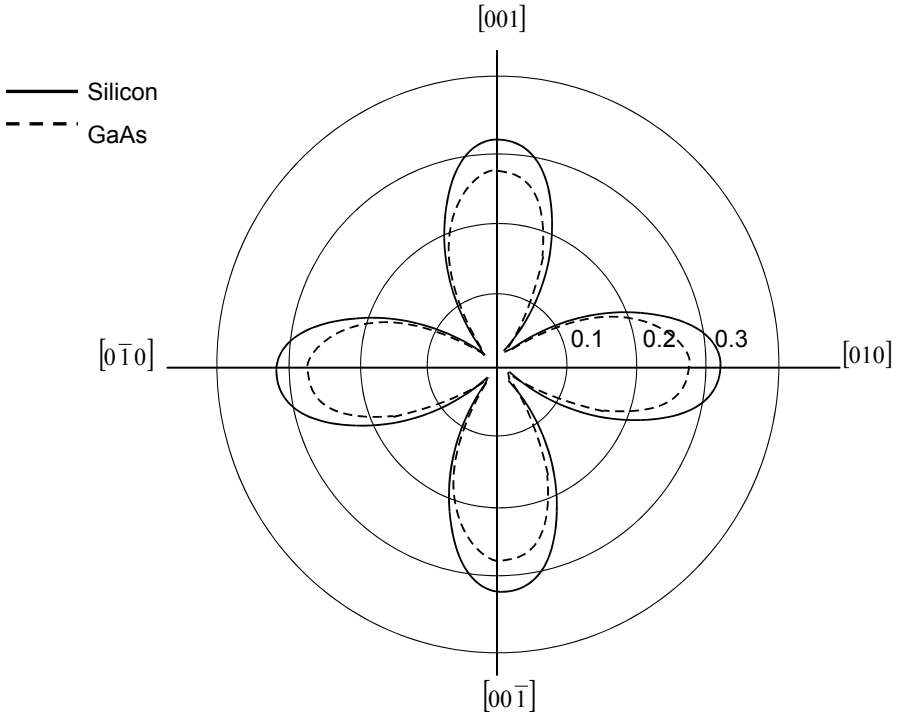


Figure 5-4: Poisson's ratio as a function of angle in the (100) plane with *l* and *m* varying in the (100) plane [109].

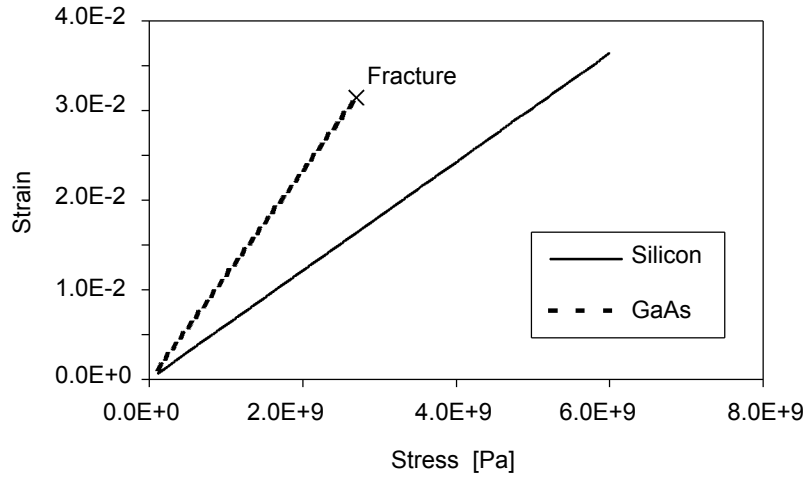


Figure 5-5: Stress versus strain relationships for bulk Si and GaAs. This chart has been idealized. In reality there is a small curvature to the stress strain curve of any material [109].

Many of the mechanical failures in crystalline solids occur as the result of defects in crystal structures. These defects are the result of imperfect techniques in crystal growth and are critically important to the study of the properties of crystals.

There are several kinds of defects. Point defects such as vacancies, interstitial atoms and point (atoms) replacements and dislocations such as edge dislocation, screw dislocation and precipitates. From the reliability standpoint, this means that using high quality wafers with smaller numbers of point defects and dislocations device reliability and lifetime will ultimately increase [20].

5.2.2.3 Fracture strength

The reason for studying defects is that, for brittle materials, the fracture strength is a function of the largest crystal defect. For a defect of length l_c, the fracture strength can be determined by [109]:

$$\sigma_F = \frac{K_{lc}}{Y_g \sqrt{l_c}} \tag{5-17}$$

where

K_{lc} = fracture toughness

σ_F = fracture strength

Y_g = dimensionless parameter that depends on the geometry of the flaw

It is sometimes useful to approximate the defect as being penny shaped with a radius, l_r, in which case the fracture strength is [17]:

$$\sigma_F = \frac{1.6K_{lc}}{\sqrt{\pi l_r}} \tag{5-18}$$

5.2.3 Fatigue

Fatigue is failure mechanisms caused by the cyclic loading of a structure below the fracture stress of a material. This loading leads to the formation of surface microcracks that cause the slow weakening of the material over time and create localized plastic deformations.

Fatigue also causes a gradual change in the properties of a material. After repeated cycling, which is often on the order of billions of cycles, Young's modulus will gradually shift. Electrical resistance of many structures will also increase over time. The combined effect of these changes can lead to degradation failure [63], [86].

5.3 Stress (strain) effects on electronic properties of semiconductors

5.3.1 Stress effects on the energy band-gaps

The compressive and tensile forces result in the modification of the electronic properties of semiconductors, such as the band structure shown in Fig. 5-6. Compressive forces, for example, cause the in-plane atoms to get closer. Thus, both the conduction and valence band extremes move away from one another and the band-gap increases. In the case of tensile forces, the in-plane atoms move away, and the opposite situation occurs, i.e., the width of the band-gap decreases. Analysis shows that the valence band can undergo profound changes. This is due to the presence of heavy-hole (large effective hole mass) and light-hole bands in most compound semiconductors, which are degenerated at the zone center, as shown in Fig. 5-6. Under uniaxial tensile strain ($\varepsilon_{xx} > 0$), the light-hole band moves up faster than the heavy-hole band. In the uniaxial compressive strain case ($\varepsilon_{xx} < 0$), the light-hole band moves downwards away from the heavy-hole band. In both cases, the degeneracy in the zone center is removed. The conduction band, and therefore the electron properties, does not change appreciably except that the conduction band moves up with compressive strain and moves down with tensile strain. Such stain effects on the energy levels can be mathematically described which are out of the scope of this dissertation [83].

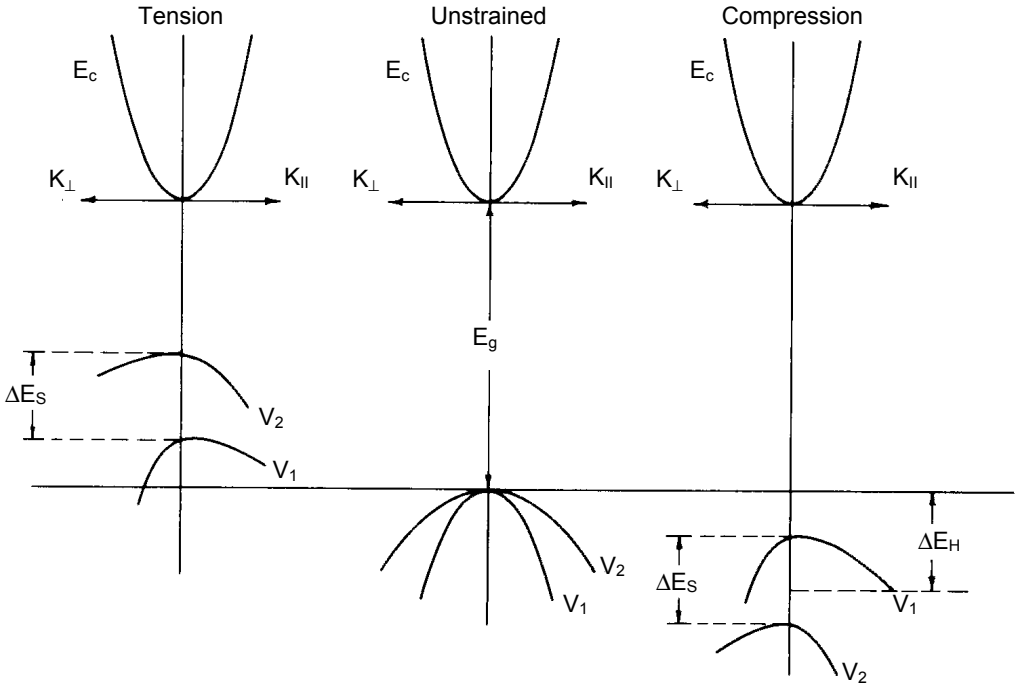


Figure 5-6: The compressive ($\varepsilon_{xx} < 0$) and tensile ($\varepsilon_{xx} > 0$) strain result in the modification of energy band structure in a semiconductor. E_c, V_1 and V_2 are conduction band, light-hole band and heavy-hole band energies, respectively. E_g is band-gap and ΔE_H and ΔE_S are the hydrostatic and shear strain components, respectively [83].

5.3.2 Stress effects on the carrier densities

Since GaAs-base devices have been used in the QMIT, the carrier densities under mechanical stress are extracted for GaAs material.

If strain is present in a semiconductor, the electron concentration in the Γ band will be given by:

$$n_e(\varepsilon) = \int_{-\infty}^{+\infty} \rho_c(E - E_c^{\Gamma}(\varepsilon)) f_c(E) dE \tag{5-19a}$$

where ρ_c is the strain-dependent conduction band density of states given by:

$$\rho_c(E - E_c^{\Gamma}(\varepsilon)) = \frac{(2m_n)^{3/2}}{2\pi^2\hbar}(E - E_c^{\Gamma}(\varepsilon))^{1/2} \tag{5-19b}$$

and $f_c(E)$ is the probability of electron occupancy at a given energy E (Fermi-Dirac distribution function) and is given by:

$$f_c(E) = 1/\{1 + \exp[(E - E_F(\varepsilon))/k_bT]\}$$

Using dimensionless notation:

$$u = (E - E_c^{\Gamma}(\varepsilon))/k_bT \text{ and } \ddot{u} = (E_F(\varepsilon) - E_c^{\Gamma}(\varepsilon))/k_bT$$

equation (4-19) can be rewritten as:

$$n_e(\varepsilon) = \frac{1}{2\pi^2}\left(\frac{2m_nk_bT}{\hbar^2}\right)^{3/2} \int_0^{\infty} \frac{u^{1/2}du}{1 + \exp(u - \ddot{u})} \tag{5-20}$$

For the non-degenerate (low-doping) case the Maxwell-Boltzmann distribution is used to replace the Fermi-Dirac distribution function in (4-20); the electron concentration is given by:

$$n_e(\varepsilon) = N_c \exp\left(-\frac{E_c^{\Gamma} - E_F}{k_bT}\right) \tag{5-21a}$$

where

$$N_c = \left(\frac{2\pi m_nk_bT}{h^2}\right)^{3/2} M_{\Gamma} \tag{5-21b}$$

is the effective density of states in the conduction band and M_Γ = 1 is the number of equivalent minima in the Γ band.

When all the Γ (direct) and X (indirect) conduction bands are considered in GaAs, the integral may be easily evaluated for $(u-\ddot{u}) >> 1$ (Boltzmann distribution). In this way the electron density is:

$$
\begin{aligned}
n(\varepsilon) &= 4\pi\left(\frac{2m_n^{\Gamma}k_bT}{h^2}\right)^{3/2} M_{\Gamma}\exp(\ddot{u})\int_0^{\infty} u^{1/2}\exp(-u)du \\
&+ 4\pi\left(\frac{2m_n^{\mathrm{L}}k_bT}{h^2}\right)^{3/2} M_{\mathrm{L}}\exp(\ddot{u})\exp\left(\frac{-\Delta E_{\Gamma\mathrm{L}}}{k_bT}\right)\int_0^{\infty} u^{1/2}\exp(-u)du \\
&+ 4\pi\left(\frac{2m_n^{\mathrm{X}}k_bT}{h^2}\right)^{3/2} M_{\mathrm{X}}\exp(\ddot{u})\exp\left(\frac{-\Delta E_{\Gamma\mathrm{X}}}{k_bT}\right)\int_0^{\infty} u^{1/2}\exp(-u)du
\end{aligned}
\tag{5-22}
$$

where ΔE is the displacement of the L and X bands from the E_c^{Γ}, i.e., $\Delta E_{\Gamma\mathrm{L}} = E_c^{\mathrm{L}} - E_c^{\Gamma}$ and $\Delta E_{\Gamma\mathrm{X}} = E_c^{\mathrm{X}} - E_c^{\Gamma}$, and $M_{\Gamma} = 1$, $M_{\mathrm{L}} = 4$ and $M_{\mathrm{X}} = 3$ are the numbers of the equivalent minima in the Γ, L and X bands, respectively.

Similar expressions for the hole concentration can be calculated in the same way [83]. It should be mentioned that the above equations are useful for electron concentration in three-dimensional cases and must be modified for lower dimensional cases.

5.3.3 Stress effects on the carrier mobility

Carrier mobility of semiconductors is influenced by mechanical stress. The accepted explanation for this phenomenon is the many-valley model [77], [112]. Anisotropic conditions exist when the mobility in one crystal direction is different from the mobility in the other crystal lattice directions. This results when the semiconductor is in a stressed state.

The stress tensor distorts the conduction energy bands of the unstressed semiconductor in different magnitudes depending on direction. The energy levels and curvatures of the band energies corresponding to the perpendicular directions are influenced differently by the applied strain. The effective masses of the carriers are proportional to the energy bands' curvatures in reciprocal momentum-space. Since the carrier mobility is a function of the carrier effective masses, the strain influence on the energy band level curvatures results in directionally dependent influences on the carrier mobility and therefore the resistivity of the semiconductor. The energy band shifts are also influenced on dopant concentration and temperature. Therefore the energy band's sensitivity to stress will also be dependent on these influences.

Mechanical stress also influences the generation/recombination process in the semiconductors. Rindner [97] attributed the effect of uniaxial compressive stresses to increased dislocation densities that decreased the carrier lifetimes and therefore increased the generation/recombination current component in a pn-junction. This effect becomes the greater influence under higher magnitudes of stress due to the dislocation generation to relax the applied stress.

5.4 Thermo-mechanical stress in the earlier concept of QMIT

In this section, a three dimensional finite element thermo-mechanical stress simulator, an scanning probe microscopy (SPM) measurement and a nanometer surface profiler of DEKTAK accompanied by a Peltier-element, have been used to determine the thermo-mechanical stress distribution in the standard structure of earlier concept of QMIT. In this method, by measuring and mapping the surface profile of Si-wafer around the embedded devices using SPM and DEKTAK, the induced thermo-mechanical stress is determined. Effects of different parameters such as baking temperature, power dissipation of the embedded GaAs-FET, geometry and elastic properties of thermal conductive epoxy have been described in details. For faster performance of simulations, a new model for standard structure of earlier concept of QMIT with a minimum number of nodes has been introduced [55], [56].

5.4.1 Principle of the applied approach

In this approach, it is assumed that at the beginning of the baking process, the glue is fluid and expanded. The glue is baked in this state. Due to different thermal expansion coefficients of Si, GaAs and glue, mechanical stress builds up when the structure is removed from the oven (at room temperature). Normally the baking process of the epoxy is done at different temperatures. Because the Young's modulus of the epoxy at temperatures higher than the glass temperature is much smaller than that at lower temperature, it is assumed that at these temperatures, the stress is very low and most of the stress is induced by the temperature difference between the glass temperature and operating temperature. In this method, the induced stress is determined by measuring and mapping the surface profile of Si-wafer around the embedded devices, using DEKTAK and SPM. To measure the one-dimensional surface profile of the Si-wafer around the embedded active device, a simple nanometer surface profiler of DEKTAK has been used successfully. DEKTAK has a big range of measurement (>6mm) and this makes it possible to perform the auto-leveling of the measurements according to the unstressed places far from the active device and have absolute amount of the displacement which can be compared with the simulation. At the places near the corner of the active device the structure is not symmetrical and a two-dimensional mapping of the surface such as SPM measurement is needed. The range of measurement with SPM is limited (≈ 100 μm) and auto-leveling with this small range is rather difficult because there are no unstressed points in the measuring window and numerical discussion is not possible.

To perform the measurements, different test structures have been fabricated up to the baking stage of epoxy. In order to measure the displacement as a function of temperature,

a Peltier-element has been used and the exact temperature is read using a flat Pt-100 temperature sensor on the Si-wafer surface.

5.4.2 Modeling of the standard structure of earlier concept of QMIT

In the earlier concept of QMIT, decreasing the temperature causes the Si-wafer to contract and thus the hole dimensions decrease. Similarly, the dimensions of GaAs-based p-HEMT and epoxy also decrease but the thermal expansion coefficient of epoxy is much bigger than that of Si and this induces the stress. The hole dimensions change as a function of temperature difference multiplied by the expansion coefficient of Si. To have a model with minimum dimensions, which requires a minimum number of nodes, a novel model for standard structure of the earlier QMIT has been introduced. Fig. 5-7 illustrates the cross section of the model. In this model boundaries of *A* and *B* at two sides are fixed, the length of H_{eq} is equal to H_{in} and thermal expansion coefficient of Si is negative in the X and Z direction. W_g is the distance between GaAs-chip and the edge of Si-wafer.

Physical properties of the materials involved are discussed in chapter 3. In all simulations and measurements the active device used has the dimensions of 400 µm × 620 µm × 100 µm. The thickness of the Si-substrate used is 375 µm.

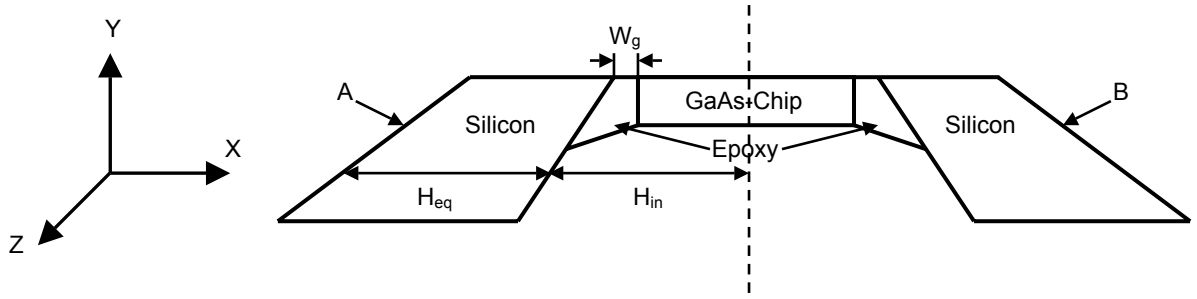


Figure 5-7: Model of standard structure of the earlier concept of QMIT.

5.4.3 Thermo-mechanical stress analysis in the standard structure

In this section the simulation results are described and the effects of different W_g, different temperature differences (DTs) and elastic property of epoxy are investigated in details.

5.4.3.1 Calculated thermo-mechanical stress in the standard structure

Fig. 5-8 illustrates the simulated "von Mises" stress at a room temperature of 25.5 °C (DT = -74.5 °C) and a W_g of 10 µm. As shown, the maximum stress is near the corners of the active device. The corresponding Y component of displacement for this simulation is shown in Fig. 5-9. To be able to compare the simulations with measurements the component of the displacement in the Y direction is presented. The cross sections normal to X and Z directions for the displacement simulation are illustrated in Figs. 5-10 and 5-

11, respectively. Fig. 5-12 shows the cross section passing through the transistor corner and outer corner of Si-substrate for the displacement simulation.

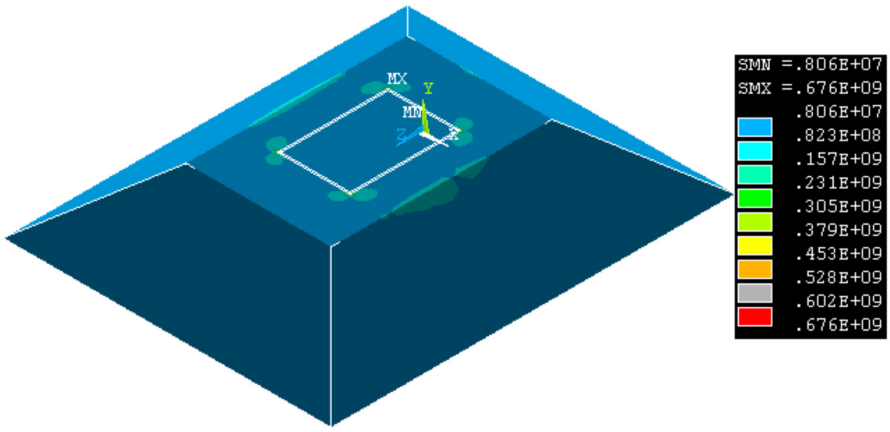


Figure 5-8: Calculated "von Mises" thermo-mechanical stress in standard structure of the earlier concept of QMIT for W_g = 10 µm and DT = -74.5 °C [Pa].

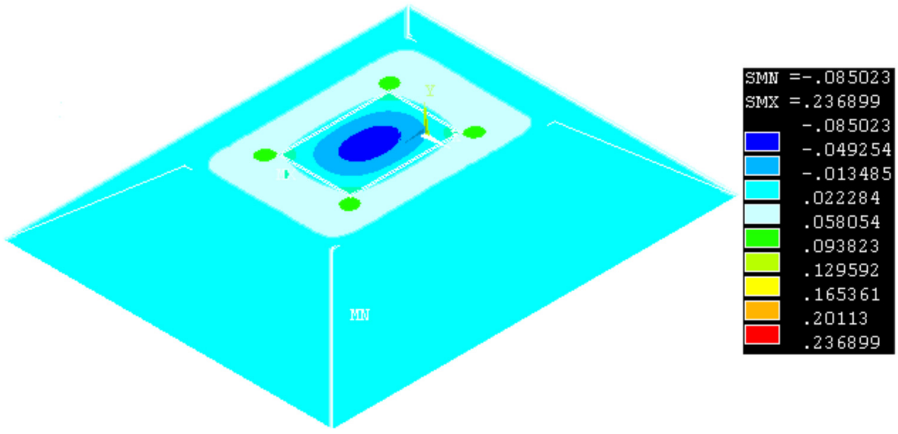


Figure 5-9: Calculated Y component of displacement in standard structure of the earlier concept of QMIT for W_g = 10 µm and DT = -74.5 °C [µm].

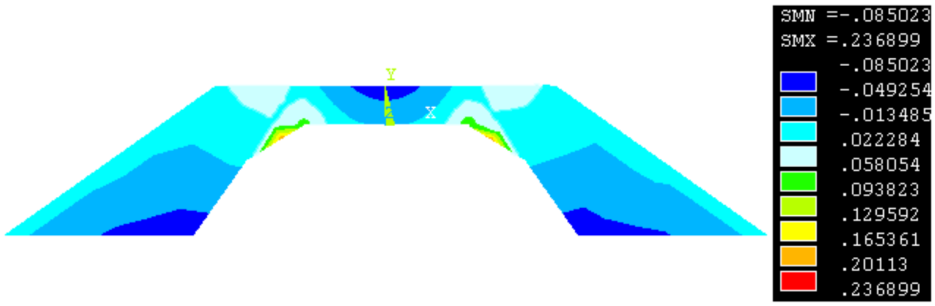


Figure 5-10: Cross-section of the displacement simulation normal to Z-axis [µm].

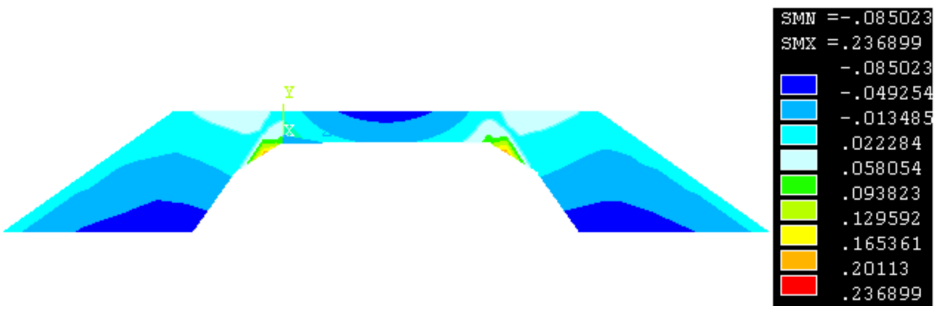


Figure 5-11: Calculated displacement distribution in the plane normal to X-axis [µm].

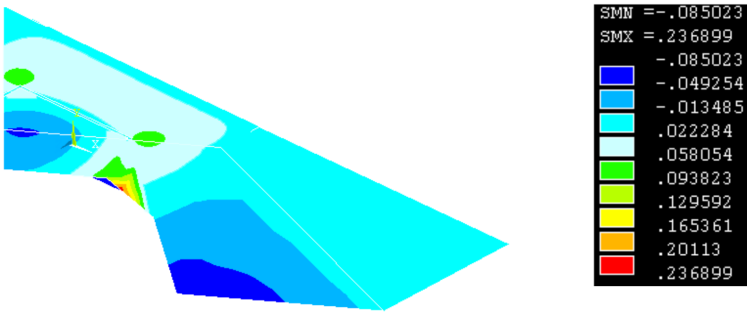


Figure 5-12: Calculated displacement distribution in the plane passing through the transistor corner and outer corner of Si-substrate [µm].

5.4.3.2 Effect of elastic properties of the epoxy

The calculated maximum "von Mises" thermo-mechanical stress for the standard structure of the earlier concept of QMIT as a function of Young's modulus of epoxy is represented in Fig. 5-13. In these simulations, W_g is 20 µm and DT is -74.5 °C. As shown, the lower Young's modulus of the epoxy is, the lower is the thermo-mechanical stress and the mechanical strength. On the other hand, some other parameters such as thermal conductivity, thermal expansion coefficient and permeability near to those of silicon and GaAs should be considered and use a trade-off among them.

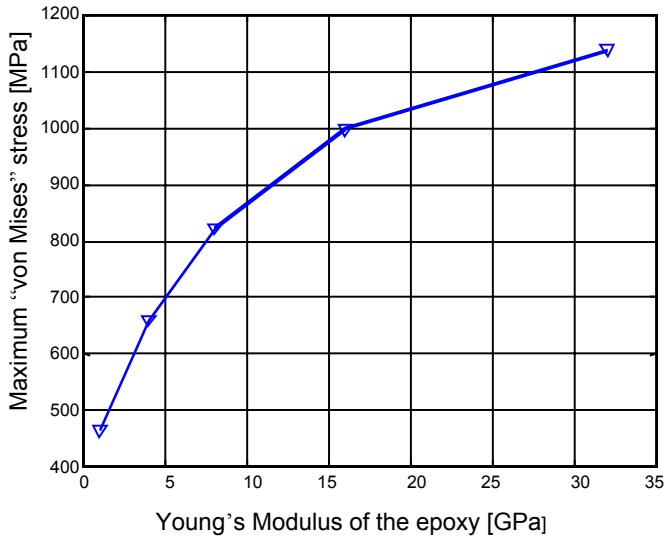


Figure 5-13: Maximum "von Mises" stress as a function of the epoxy Young's modulus. W_g = 20 µm and DT = -74.5 °C.

5.4.3.3 Effect of different geometry of the epoxy

Fig. 5-14 shows the calculated maximum "von Mises" thermo-mechanical stress as a function of W_g. In the fabrication process, the minimum of W_g is about 10 µm and is determined by the defects in the scribing process of the active device, which is done by the manufacturer, but the maximum of W_g is determined by the thermo-mechanical stress and the corresponding displacement result from the DT in the succeeding fabrication

steps. A big amount of displacement breaks the air bridges in the succeeding steps. From Fig. 5-14 the optimum W_g is 15 µm.

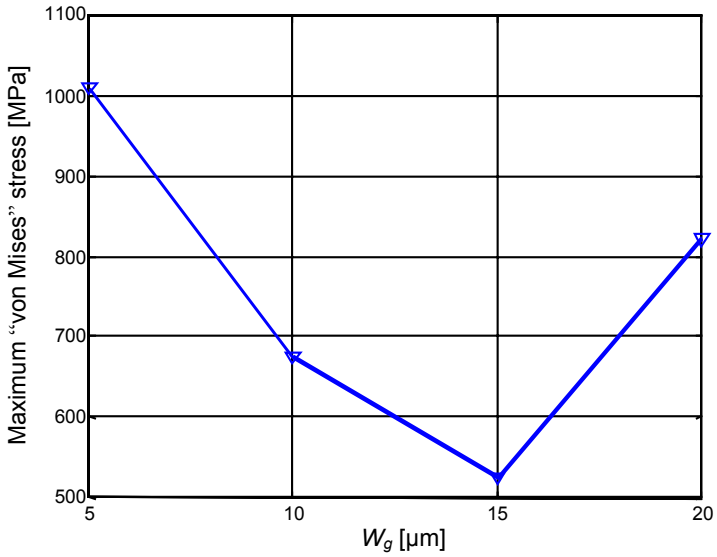


Figure 5-14: Maximum "von Mises" stress as a function of W_g.

5.4.3.4 Effect of baking temperature of the epoxy and power dissipation of the active device

According to the manufacturer's data sheet [18], baking temperature of the epoxy may vary from 50 °C for 12 hours to 120 °C for 20 min. For baking temperatures below T_g, the DT is equal to the difference between the room temperature and the baking temperature. For baking temperatures higher than T_g, DT is equal to the difference between T_g and the room temperature.

Using the thermal resistance of the earlier QMIT structure, the power dissipation in active device can be easily related to DT. The thermal resistance for different structure of the earlier concept of QMIT has been simulated and optimized in chapter 3. The results can be used to have the stress distribution as a function of power dissipation of active device.

Fig. 5-15 depicts the calculated height differences of the maximum displacements from unstressed points on the surface of the Si-wafer in the A-A direction for DT values of -74.5 °C, -54.5 °C, -34.5 °C and -14.5 °C, and a W_g of 10 µm.

5.4.4 The measured displacement distributions in the standard structure

Fig. 5-16 shows the microtest-fixture from the top. All the measurements with DEKTAK are performed along the direction A-A within a 4 mm measurement range. The square shows the measurement window for SPM. The measurement window dimensions for

SPM are 100 µm × 100 µm. The DEKTAK measurement for W_g = 10 µm and DT = -74.5 °C is shown in Figs. 5-17 and 5-18.

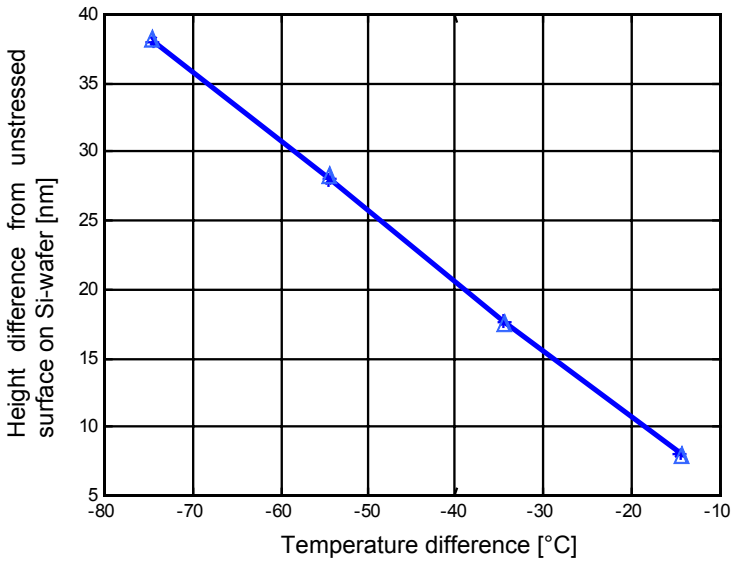


Figure 5-15: Calculated maximum height difference from the unstressed surface on Si-wafer in A-A direction for W_g = 10 µm.

The measurement in Fig. 5-18 corresponds to that in Fig. 5-17 but with a larger scale and just at one side of the embedded transistor.

Mapping results of the silicon surface near to the corner of transistor for W_g = 20 µm with DT = -74.5 °C (T = 25.5 °C) and DT = 0 °C (T= 100 °C) are shown in Figs. 5-19 and 5-20, respectively. The cross section along the direction C-C and D-D for these figures are represented in Figs. 5-21, 5-22, 5-23 and 5-24. In this measurement, because of the limited range of measurements, the auto-leveling is not properly done but from the pictures it is clear that at DT = -74.5 °C, there is a big curvature on the surface of the Si-wafer. But the surface at DT = 0 °C is almost flat and the maximum displacements very near to the corners of embedded chip have been detected and measured. These maximum displacements are predicted by the simulation and shown in Fig. 5-9.

The measurement results for DT values of -74.5 °C, -54.5 °C, -34.5 °C and -14.5 °C with DEKTAK are shown in Fig. 5-25. During the measurements, the temperature around the GaAs-chip was accurately adjusted using a closed-loop system consisting of a Pt-100 temperature sensor, a Peltier-element and an automatic digital current supply. The fabricated microtest-fixture was fixed on the Peltier-element by a thermal conductive paste. The flat Pt-100 temperature sensor was placed on the top of Si-wafer very near to the embedded GaAs-based p-HEMT. The temperature very near to the active device was measured and the desired reference temperature was obtained by adjusting the input current of the Peltier-element within an accuracy of less than 0.1 °C.

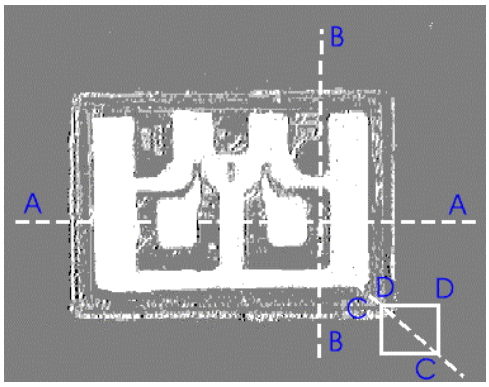


Figure 5-16: Top-view of the microtest-fixture.

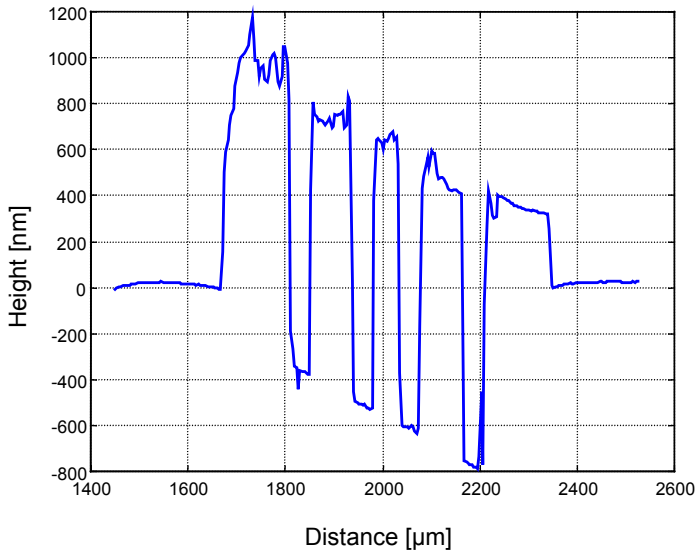


Figure 5-17: Surface profile of the microtest-fixture along the A-A line using DEKTAK.

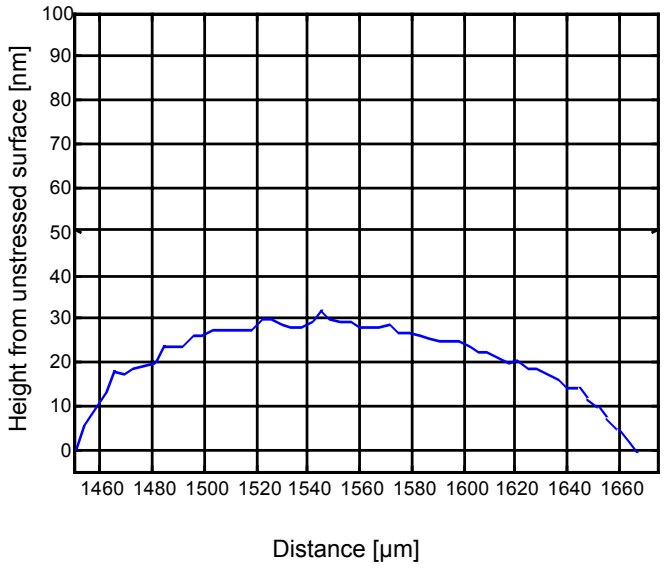


Figure 5-18: The left part of Fig. 5-17. W_g = 10 µm and DT = -74.5 °C.

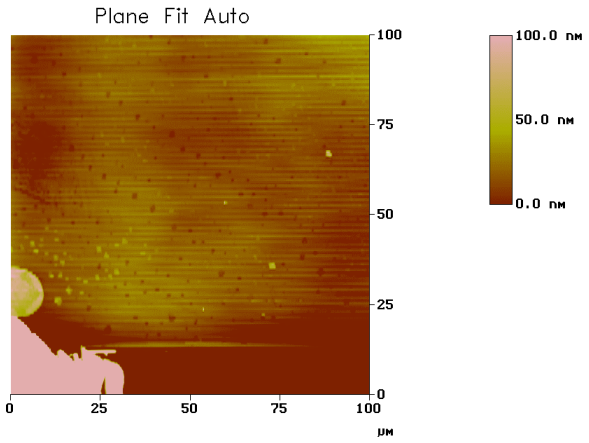


Figure 5-19: Surface mapping of the microtest-fixture with SPM. W_g = 20 µm and DT = 0 °C.

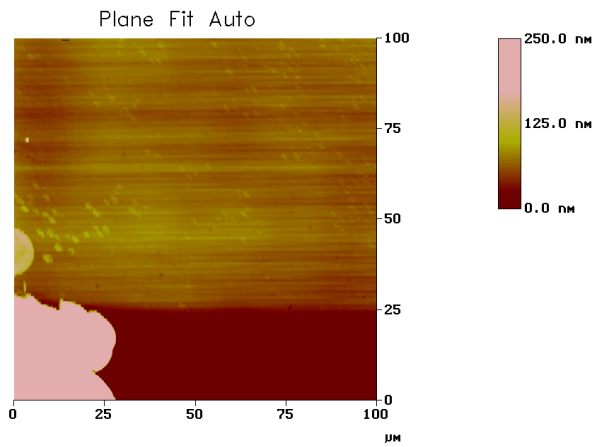


Figure 5-20: Surface mapping of the microtest-fixture with SPM. W_g = 20 µm and DT = -74.5 °C.

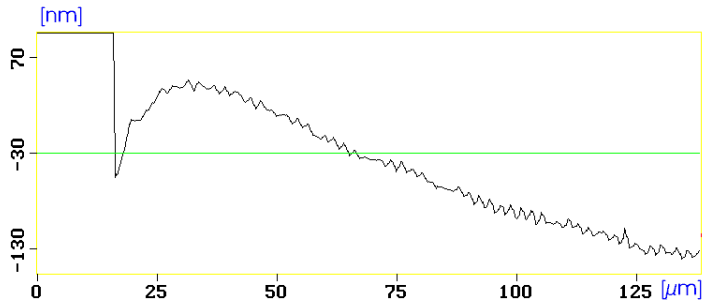


Figure 5-21: Cross-section of Fig. 5-19 along the C-C line.

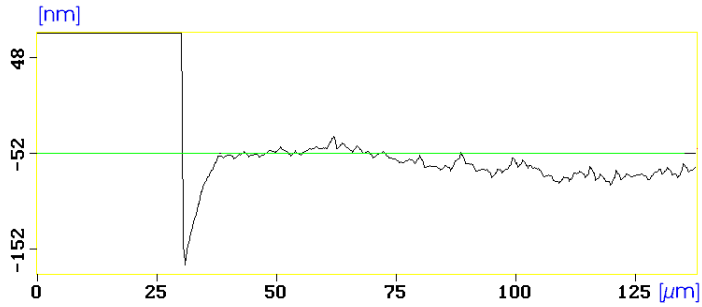


Figure 5-22: Cross-section of Fig. 5-20 along the C-C line.

Figure 5-23: cross-section of Fig. 5-19 along the D-D line.

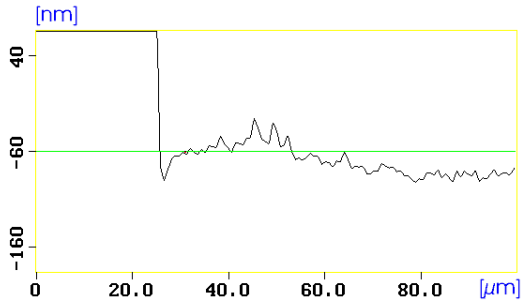


Figure 5-24: Cross-section of Fig. 5-20 along the D-D line.

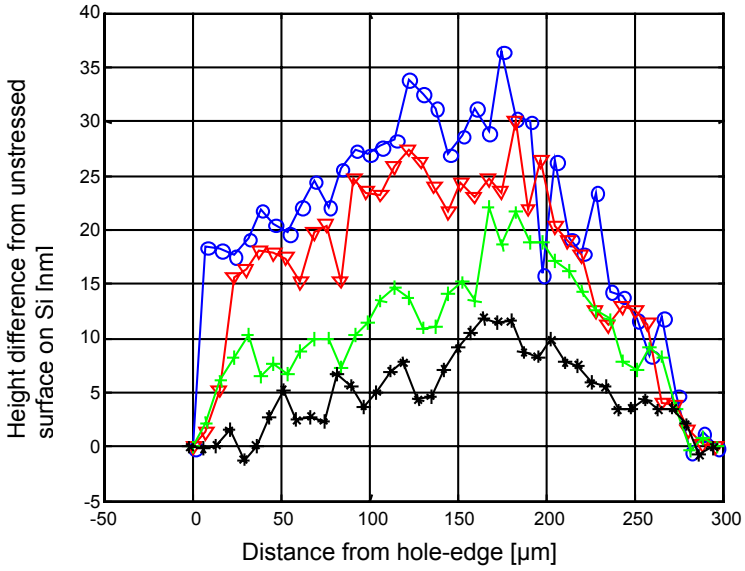


Figure 5-25: Measured surface profile on the Si-wafer along A-A direction in Fig. 5-16. DT for o, ∇, + and * are -74.5 °C, -54.5 °C, -34.5 °C and -14.5 °C, respectively.

5.4.5 Comparison of the calculated and measured induced displacement

The calculated and measured height differences of the maximum displacements from the unstressed points on the surface of the Si-substrate in the A-A direction for DT values of -74.5 °C, -54.5 °C, -34.5 °C and -14.5 °C and W_g of 10 µm have been compared in the Fig. 5-26. The results show an excellent agreement.

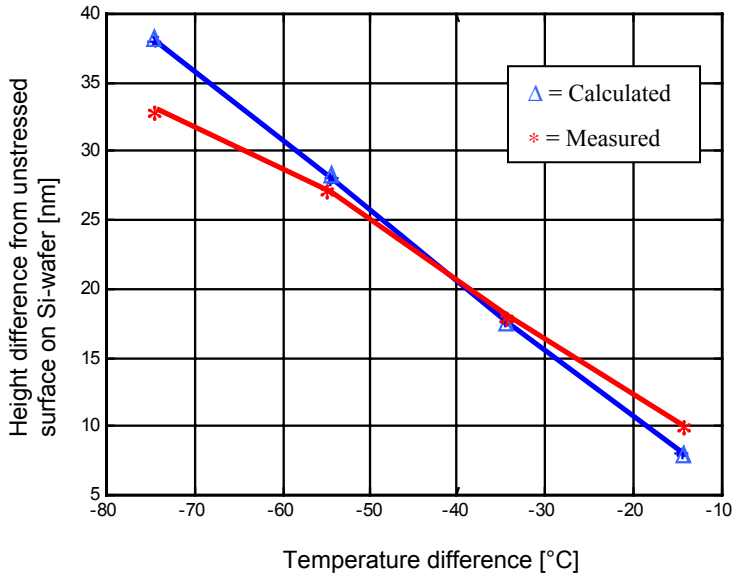


Figure 5-26: Measured and calculated maximum height difference from the unstressed surface on Si-wafer in A-A direction. W_g = 10 µm.

5.5 Thermo-mechanical stress in the enhanced QMIT

In this section thermo-mechanical stress analysis for the enhanced QMIT has been performed using a nonlinear three-dimensional finite element simulator. To confirm the simulation results, a white-light interferometery measurement along with a Peltier-element and a Pt-100 temperature sensor have been used.

Simulation and measurement results have an excellent agreement and demonstrate a great decrease of thermo-mechanical stress in the new generation QMIT in comparison to the earlier concept, which extremely improves lifetime of the packaging [57].

5.5.1 Thermo-mechanical stress analysis

Fig. 5-27 shows the cross-section view of the fabricated microtest-fixture in the coplanar circuit realization of the enhanced QMIT (Fig. 2-4). For all the thermo-mechanical stress simulations and measurements, a low noise Ka-band GaAs-based p-HEMT with a gate length of 0.25 µm, a height of 100 µm, a length of 620 µm and a width of 400 µm have been used. Because of the symmetry only one quarter of the structure is used for simulations. In the thermo-mechanical stress simulations, the displacement on some surfaces has been set to zero to fulfill the symmetry in the model and fixation of the model. Properties of the materials involved are described in chapter 3.

Fig. 5-28 illustrates the thermo-mechanical stress simulation results for the enhanced QMIT structure with 10 µm PECVD amorphous silicon deposited on the backside of the transistor and W_g of 20 µm. The assumed deposition temperature of amorphous silicon is 60 °C. A higher deposition temperature improves the quality of the silicon and has a minor increase in the thermo-mechanical stress. The 8 µm thick polyimide layer is gently baked up to 250 °C. The maximum "von Mises" stress is 63.7 MPa, which is eight times smaller than that of the earlier concept of QMIT [55]. This greatly improves lifetime of the packaging. Maximum "von Mises" thermo-mechanical stress curve with a W_g of 5, 15 and 20 µm for the same conditions in Fig. 5-28, is shown in Fig. 5-29. As opposed to the earlier QMIT, the maximum thermo-mechanical stress decreases by increasing the W_g.

White-light interferometery surface mapping is used to perform the displacement measurements. The spin on polyimide is transparent. The displacement measurements are done before the spinning of the polyimide layer on the microtest-fixture. To be able to compare the simulations with measurements, the displacements are calculated before the deposition of the polyimide layer. Because the Y-axis is normal to the surface of the silicon wafer, the Y component of the displacement distribution has been considered. The calculated distributions of induced displacement for W_g = 20 µm and a 30 µm thick electroplated gold layer on the transistor backside are shown in Figs. 5-30 and 5-31.

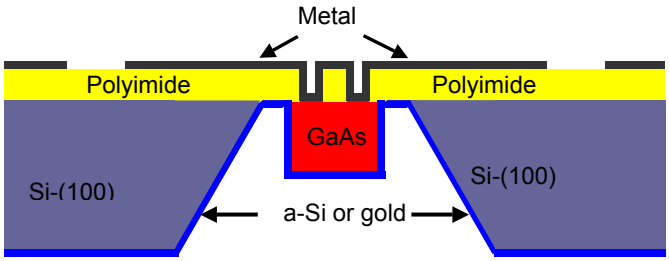


Figure 5-27: Cross-section view of the fabricated microtest-fixture in the coplanar circuit realization of the enhanced QMIT.

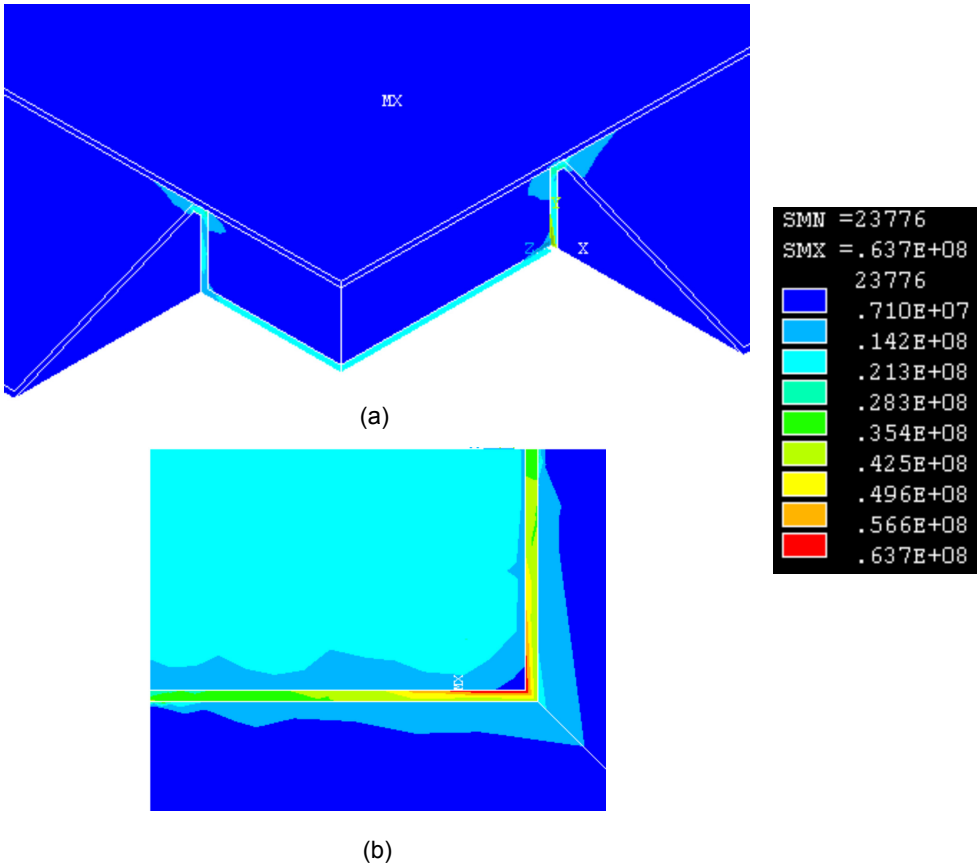


Figure 5-28: (a) Thermo-mechanical stress distribution ("von Mises") in the enhanced QMIT with a deposited 10 µm thick PECVD a-Si layer at 60 °C and W_g = 20 µm [Pa]. (b) Backside view of the simulation in the part (a).

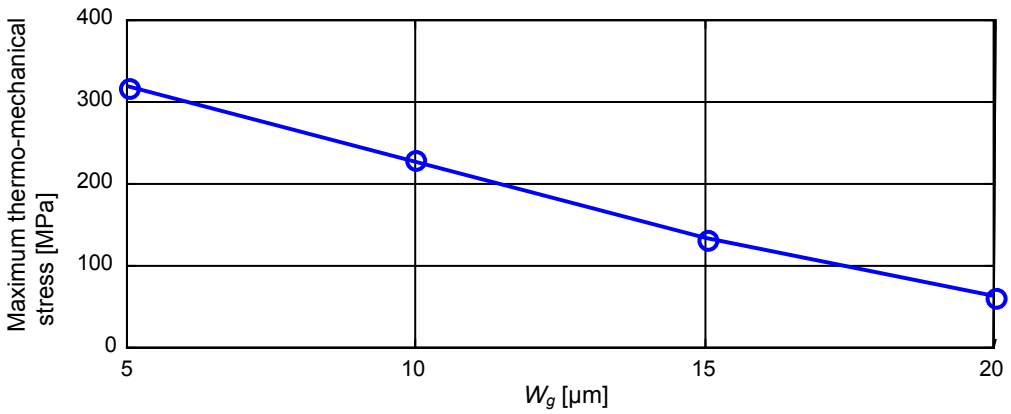


Figure 5-29: Maximum " von Mises" thermo-mechanical stress in the enhanced QMIT against W_g.

The simulation in Fig. 5-30 was performed at 22 °C (DT = -43 °C) while that shown in Fig. 5-31 was performed at 80 °C. The black square in Fig. 5-30 indicates the measurement window, which has a dimension of 0.36 mm × 0.27 mm.

5.5.2 The measured displacement distributions

To measure the displacement resulting from the thermo-mechanical stress distribution in the enhanced QMIT structure, a white-light interferometery measurement has been used. In this method, two-dimensional mapping of the surface of the silicon wafer at the corner of the transistor has been measured for temperatures between 22 °C and 80 °C. For the accurate adjustment of the temperature on the microtest-fixture, as described in the last section, a Peltier-element and a Pt-100 temperature sensor have been used in a closed-loop feedback system with a digitally controlled current source.

A similar displacement measurement method using SPM and nano-meter surface profiler of DEKTAK is described in the last section [1]. The SPM measurements are very time-consuming with a limited range of measurement (100 μm × 100 μm) and the DEKTAK measurements are mechanically destructive. The white-light interferometery measurements are fast, accurate and non-destructive and can be done in a wider range of measurement.

Figs. 5-32, 5-33 and 5-34 show the two-dimensional mapping for the measurement temperatures of 22, 60 and 80 °C. For the temperatures below electroplating temperature, there is a convex curvature while for the upper temperatures, there is a concave curvature. Top view, cross section along the diagonal and cross section along one side of the measurement window in Fig. 5-32 are illustrated in Fig. 5-35.

5.5.3 Comparison of the calculated and measured induced displacement

A pretty agreement in both variations and distributions of the induced displacement is observed. Fig. 5-30 depicts the corresponding calculated results for the measurement in Fig. 5-35. They exhibit a perfect similarity.

To prepare a sound comparison, the difference displacements of the point on the corner of the measurement square near to the transistor corner, and the point on the middle of the measurement square as a function of temperature have been calculated and measured for W_g = 20 μm and a 30 μm thick plated gold layer on the backside of the GaAs-chip. Fig. 5-36 depicts the results. The comparison reveals that the temperature dependent 3DFE structural simulator used has successfully predicted mechanical behavior of the enhanced QMIT structure under different temperatures.

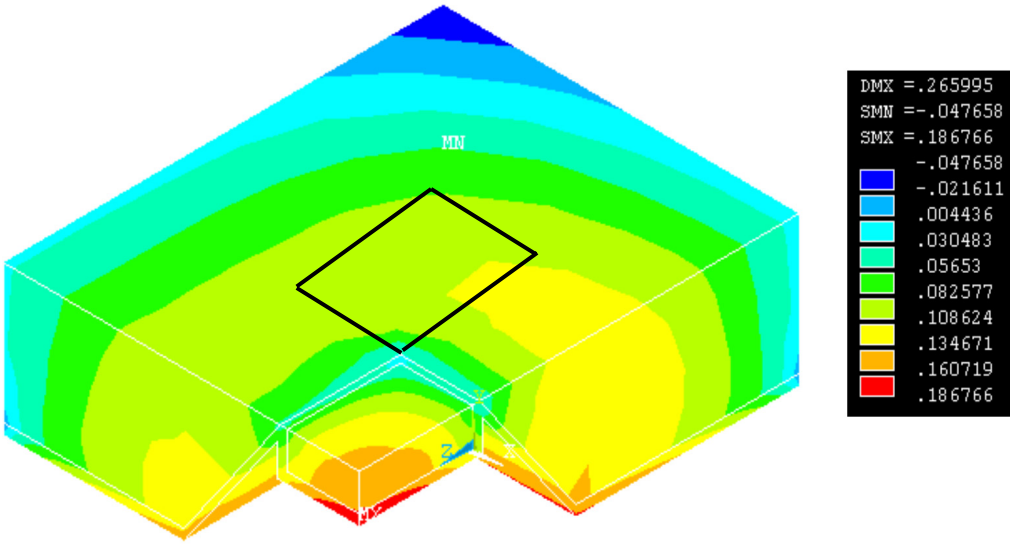


Figure 5-30: Calculated Y component of the displacement for W_g = 20 µm and a 30 µm thick electroplated gold layer on the backside of the transistor 22 °C [µm].

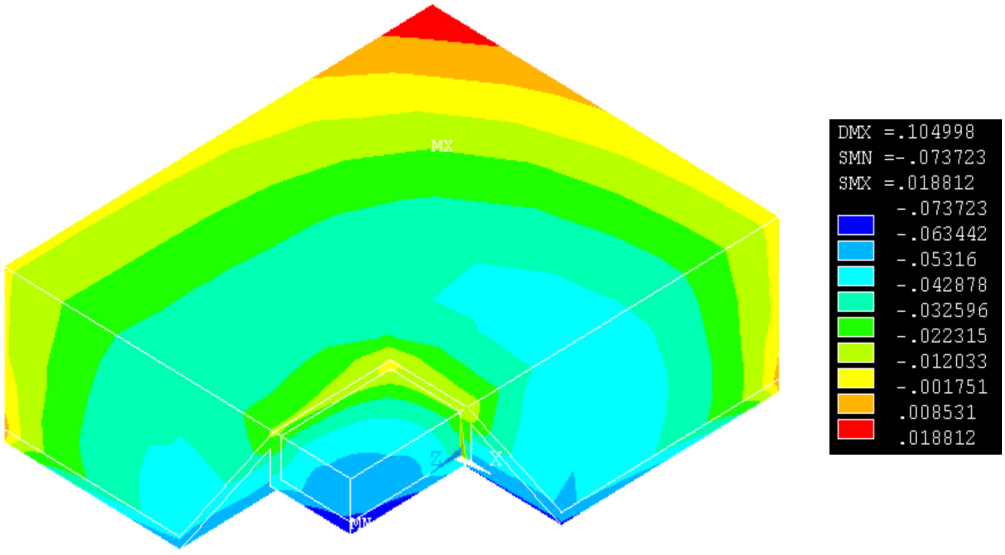


Figure 5-31: Calculated Y component of the displacement for W_g = 20 µm and a 30 µm thick electroplated gold layer on the backside of the transistor at 80 °C [µm].

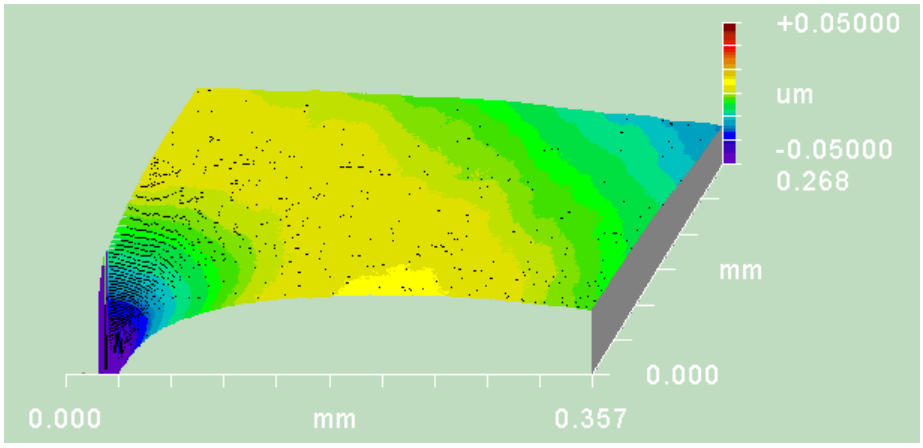


Figure 5-32: White-light interferometery mapping of the silicon surface at the corner of the transistor at a room temperature of 22 °C.

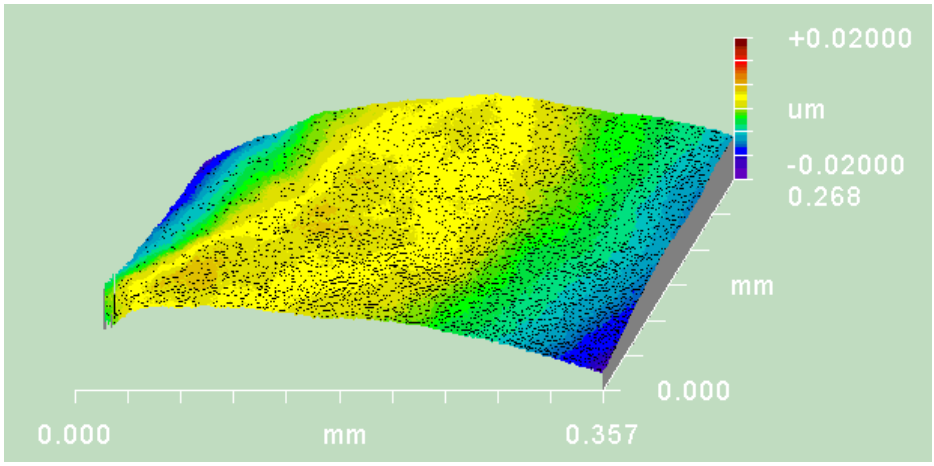


Figure 5-33: White-light interferometery mapping of the Si-surface at the corner of the transistor at a temperature of 60 °C.

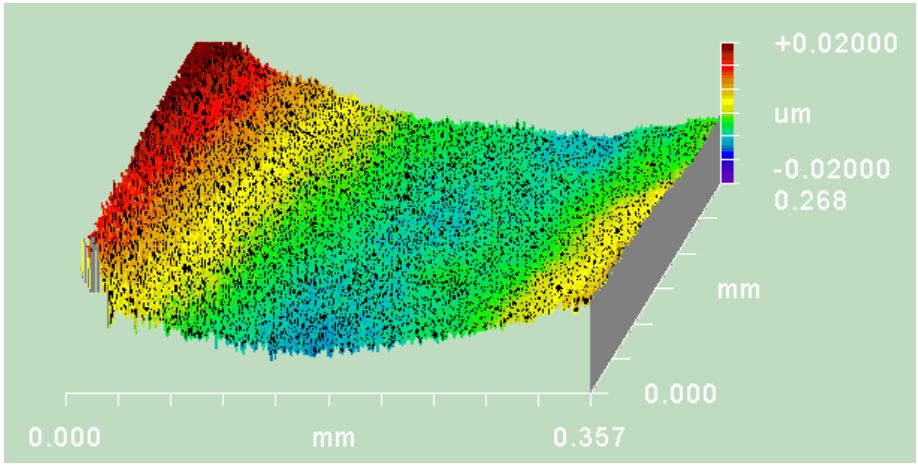


Figure 5-34: White-light interferometery mapping of the silicon surface at the corner of the transistor at a temperature of 80 °C.

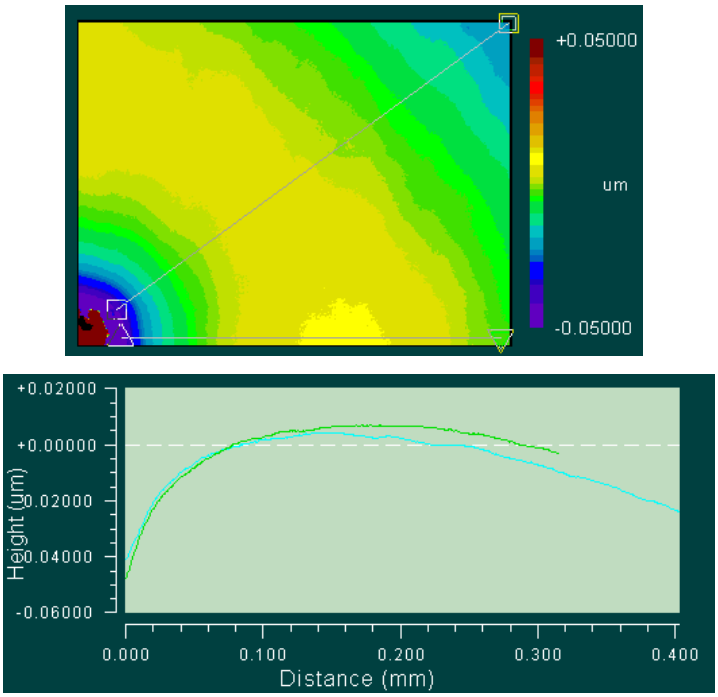


Figure 5-35: Top view and cross-sections along the diagonal and down side of the measurement in Fig. 5-32. The line along the diagonal is signed by squares in the top view and is longer in the cross-sections.

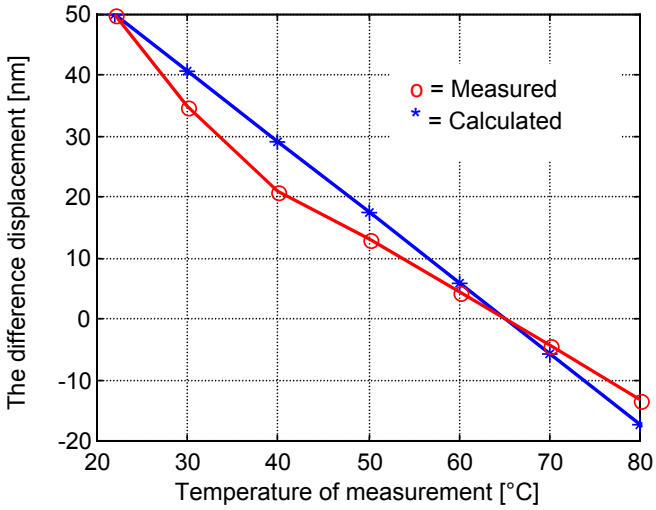


Figure 5-36: The difference displacement of the point on the corner of the measurement square near to the transistor corner and the point on the middle of the measurement square versus the temperature of measurement. W_g is equal to 20 µm and a 30 µm thick gold layer is plated.

5.6 Comparison of maximum thermo-mechanical stress in the earlier concept and enhanced QMIT structures

In comparison to silicon and GaAs, the thermally conductive epoxy used in the earlier QMIT structure has a large thermal expansion coefficient of 30E-6 K^{-1} [18]. This induces a very high stress into the structure. On the other hand, the GaAs-chips are fixed by a deposited amorphous silicon layer or an electroplated gold layer. In both cases, the thermal expansion coefficients are far nearer to those of crystal silicon and GaAs.

Maximum "von Mises" thermo-mechanical stress curve as a function of W_g for earlier concept and enhanced QMIT structures have been plotted in Fig. 5-14 and Fig. 5-29, respectively. The maximum "von Mises" stress for the enhanced QMIT structure with W_g of 20 µm is 63.7 MPa, which is more than eight times lower than that of the earlier QMIT structure with an optimum W_g of 15 µm.

The fracture strengths of silicon and GaAs are strongly dependent on surface characteristics of the wafer, dicing history, diced edge surface finish, etc. [118]. Micromechanical cantilever beam structures in ordinary GaAs semi-insulating and silicon wafers have been fracture tested in [38] and [19]. The average fracture strength for the GaAs and silicon beams were 2.7 and 6 GPa, respectively. In another report, 135 bulk silicon microcantilever beams loaded from the front-side exhibit the minimum and maximum fracture strengths of 0.7 to 5.0 Gpa with a standard deviation of 0.8 GPa [129]. Although, the thermo-mechanical stresses in the earlier concept of QMIT can be lower than these reports, it is well known that a higher thermo-mechanical stress results in a higher fracture probability and a shorter lifetime [74], [109], [112].

5.7 Summary

Reliability and lifetime of a packaging have been defined and the main effects of the mechanical stress on failure mechanism and electronic properties of semiconductors have been discussed.

A method for the determination of the thermo-mechanical stress distribution in the earlier QMIT structure has been represented. A nonlinear three-dimensional finite elements simulator, an SPM, a nanometer surface profiler of DEKTAK and a Peltier-element have been used to calculate and measure the stress distribution in the standard structure of the earlier concept of QMIT. Effects of different parameters such as W_g, elastic property of epoxy, baking temperature of epoxy and power dissipation of active device have been investigated. A new model for the earlier QMIT structure has been introduced which uses a minimum volume, which leads to minimum number of nodes and hence a maximum speed of calculations. The model agrees very well with.

Three-dimensional finite elements thermo-mechanical stress simulations for the enhanced QMIT have been performed. To measure the resulting displacements, a white-light interferometery measurement along with a Peltier-element and a Pt-temperature sensor has been used. The measured displacements have been compared with the corresponding calculations. In comparison with the earlier concept of QMIT, great improvement in maximum thermo-mechanical stress has been observed for the new generation. This results in a much better reliability and lifetime of the packaging.

Chapter 6

A Reliable Neural Model for p-HEMT from a Smaller Number of Measurement Data in the Enhanced QMIT

6.1 Introduction

In this chapter a systematic approach is presented to achieve a reliable neural model for microwave active devices with different numbers of training data. The method is implemented for a small-signal bias dependent modeling of p-HEMT in two different environments: on a standard test-fixture and in the enhanced QMIT, with different numbers of training data. The errors for different numbers of training data have been compared to each other and show that, by using this method, a reliable model is achievable even though the number of training data is considerably small. The method aims at constructing a model, which can satisfy the criteria of minimum training error, maximum smoothness (to avoid the problem of over-fitting), and simplest network structure [48].

In the next section, different aspects of RF and microwave designs and role of artificial neural networks (ANN) are briefly described. Multilayer perceptrons (MLP) type neural network (NN) is covered in section 6.3. Principle of the approach, method for training and evaluation of the neural model, model developments and results for a GaAs-based p-HEMT on a standard test-fixture and in the enhanced QMIT environment are given in sections 6.4, 6.5, 6.6 and 6.7, respectively. The last section is dedicated to the summary.

6.2 RF and microwave designs and position of the neural modeling

The sequence of various steps in a typical RF and microwave design, like any other design, is shown in Fig. 6-1 [133]. One starts with problem identification. This phase deals with determining the need for a product. A product is identified, resources allocated, and end-users are targeted. The next step is drawing up the product design specifications (PDS), which describes the requirements and performance specifications of the product. This is followed by a concept generation stage, where preliminary design decisions are made. Normally several alternatives will be considered. Decisions made at this stage determine the general configurations of the product and thus have enormous implications for the remainder of the design process. At each of these design stages, there is usually a need for feedback to earlier stages and reworking of the previous steps. The analysis and evaluation of the conceptual design lead to concept refinement, for example, by placing values on numerical attributes. The performance of the conceptual design is tested for its response to external inputs and its consistency with the design specifications. These steps lead to an initial design. The step from initial design to final detailed design involves modeling, computer-aided analysis, and optimization. Computer aided design (CAD) tools currently available to us for RF and microwave design primarily address this step only. The design process outlined above can be considered to consist of two segments. Initial steps starting from the product identification to the initial design may be termed *design-in-the large*. The second segment that leads from an initial design to the detailed design has been called *design-in-the-small*. It is for this second segment that the most current RF and microwave CAD tools have been developed [133].

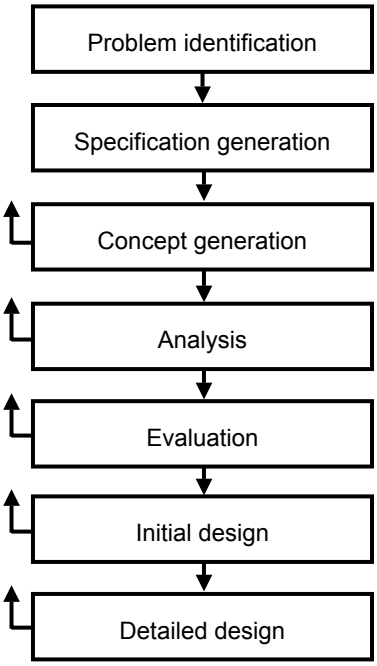


Figure 6-1: Sequence of stages in a typical design process.

6.2.1 Modeling of RF and microwave circuits and devices

As already discussed three important segments of CAD are:

- Modeling
- Analysis
- Optimization

An accurate and reliable modeling of RF, microwave and millimeterwave circuit components is one of the basic prerequisites of successful CAD. The degree of accuracy to which the performance of microwave integrated circuits can be predicted depends on the accuracy of characterization and modeling of components.

Electromagnetic (EM) modeling of RF and microwave passive components and circuits is frequently used. EM simulators offer excellent accuracy if critical areas are meshed with a sufficiently small grid. A major disadvantage is their heavy demand on computer resources [110]. There are several methods of EM modeling such as: finite-difference time-domain (FDTD) [132], finite-element method (FEM) [106] and method of momentum (MoM) [28]. Many commercial EM simulators are available in the market but we can single out the high frequency structure simulator (HFSS) from Ansoft and HP (Agilent) as the flagship FEM solver and MoM product *em* from Sonnet Software as the benchmark planar solver. They emerged in the late 1980s.

Active device modeling is one of the most important areas of microwave CAD. Over the past 50 years, there has been progressive improvement in both the active devices and their associated models. Most traditional microwave and RF design techniques for active circuits are based on equivalent-circuit models or parametric characterization (black-box models), requiring extensive dc and RF characterization, although there is an increasing trend toward using physical models as part of the designer's library of tools [110].

6.2.1.1 Equivalent-circuit models

Early models of diodes and transistors consisted of a few ideal circuit elements to represent the dc, transient, and high frequency performance of these active devices. As the frequency of operation increased, so did the complexity of the models and parasitic (extrinsic) elements were added to improve accuracy. Considerable effort has been devoted to the modeling of microwave transistors, although there still remains today interest in modeling the nonlinear behavior of microwave and millimeterwave devices especially Schottky, p-i-n and resonant tunneling diodes. Equivalent-circuit models are particularly attractive for established device designs and well characterized fabrication processes [69], [71], [99], [110], [126].

6.2.1.2 Physical models

Early physical models were developed principally to provide insight into the intrinsic physical operation of devices and as an aid in the design and optimization of these semiconductor devices. Over the past 30 years, there has been an increasing application of physical models in microwave CAD and, in particular, in the study of large-signal nonlinear operation.

There are two principal types of physical models that are applied to device design and characterization. The most straightforward of these is based on a derivative of equivalent-circuit models, where the circuit element values are quantitatively related to the device geometry, material structure, and physical processes. The second approach is more fundamental in nature and is based on the rigorous solution of the carrier transport equations over a representative geometrical domain of the device. These models use numerical solution schemes to solve the carrier transport equations in semiconductors often accounting for hot electrons, quantum mechanics (HEMTs), EM, and thermal interaction. In particular, a key advantage is that physical models allow the performance of the device to be closely related to the fabrication process, material properties, and device geometry. This allows performance, yield, and parameter spreads to be evaluated prior to fabrication, resulting in a significant reduction in the design cycle (and cost). Furthermore, since physical models can be embedded in circuit simulations, the impact of device-circuit interaction can be fully evaluated. A further advantage of physical models is that they are generally intrinsically capable of large-signal simulation [110].

6.2.2 Role of neural modeling

As mentioned in subsection 6.2.1, the most frequently used approaches in today's circuit design are based on lumped equivalent circuits. A large variety of such equivalent circuit models have been developed in the past, because no single equivalent model can represent all kind of transistor behavior. The specific equivalent circuit structure in a model optimized for one type of device becomes a limitation of the model for other devices. As the technology changes rapidly, new semiconductor devices are constantly evolving, and development of models to represent the new transistor behaviors is a continuous activity. Often a time-consuming trial-and-error process is used for formulating new equivalent circuit topology and for creating formulas for nonlinear elements. Although considerable number of electrothermal quasi-2-dimensional (Q2D) physical models have been developed, but physical models, considering temperature effects, require a three-dimensional domain to achieve accurate results and this increases the computational time and cost. Developing new equivalent circuit or physical models requires human experience and judgment [110].

Significant advances have been made in the exploitation of ANNs as an unconventional alternative to modeling and design tasks in RF and microwave CAD [14], [133]. ANN computation is very fast and ANNs can learn and generalize from data, allowing model development even when component formulas are unavailable. State of the art developments include knowledge-based ANN modeling and neural space mapping optimization. Initiatives in integration of ANN capabilities into circuit optimization, statistical design, and EM and global modeling are being made [110].

NNs are commonly used for different aspects of microwave CAD. An MLP type NN was used for bias-dependent small-signal modeling of p-HEMT in different environments. The commonly used MLP model belongs to the type of black-box models structurally embedding no problem-dependent information or knowledge. Therefore, it derives the entire information about the microwave behavior from the training data. Consequently, a large amount of training data is needed to ensure model accuracy and generalization [30], [107], [117], [127]. In microwave and millimeterwave applications, training data is obtained by simulation of original EM or device-physics problems, or by measurements. Generating a large amount of training data could be very expensive, because simulation or measurement may have to be performed at many points in the model input parameter space. For example, a combination of geometrical, process and bias parameters need a large number of training data.

6.3 Fundamental of multilayer perceptrons type neural networks

An artificial neural network (ANN) is a massively interconnected dynamic system of simple adaptive units interacting with the objects of the real world in a manner similar to a biological nervous system. The network has no pre-programmed instructions to follow; it responds to inputs through parallel recognition and association by modifying the strength (weights) of connections. Thus, ANN may be deemed as non-programmed adaptive computation systems capable of developing associations among objects in response to the environment [30].

An ANN consists of two primary types of elements, the processing units (artificial neurons) and interconnections (artificial synapses). Typically, a network consists of a set of sensory units (source nodes) that constitute the input layer, one or more hidden layers of computation nodes, and an output layer of computation nodes called MLP. The input signal propagates through the network in a forward direction, on a layer-by-layer basis. MLP have been applied successfully to solve some difficult and diverse problems by training them in a supervised manner with a highly popular algorithm known as the error back propagation (EBP) algorithm [30]. Although the four layer perceptrons in some cases are preferred, it has been previously shown a three-layer perceptrons NN with an

EBP algorithm can encode any arbitrary complex input-output relationship [117]. The structure of a three-layer perceptrons type NN is presented in Fig. 6-2. The circles represent neurons and the lines between them correspond to connection weights w_i. In each neuron the inputs S_i are multiplied by the connection weights w_i, and products are added to yield the neural potential p, which is given by:

$$p = \sum_{i=1}^{N_i} w_i S_i \tag{6-1}$$

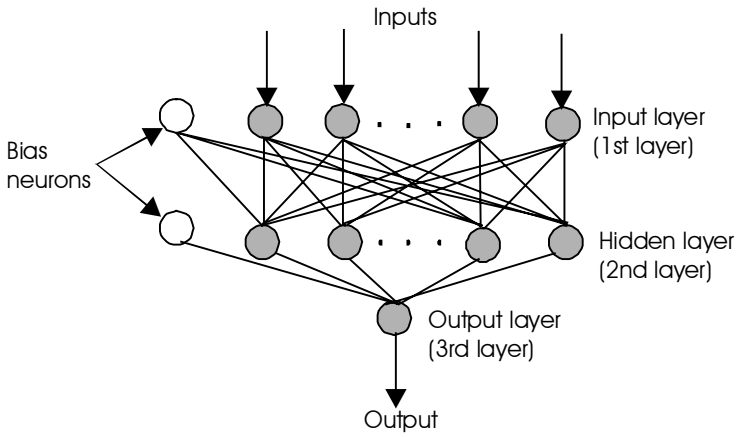


Figure 6-2: Structure of an multilayer perceptrons (MLP) type neural network (NN).

where N_i is the number of neuron inputs. The output of the neuron (the state S) is defined as:

$$S = f_s(p) = f_s(\sum_{i=1}^{N_i} w_i S_i) \tag{6-2}$$

where f_s is the sigmoid function :

$$f_s(p) = \frac{1}{1 + \exp(-p)} \tag{6-3}$$

This function limits the neuron output between 0 and 1 and has the useful property $df_s(p)/dp = f_s(p)[1 - f_s(p)]$. The states of the hidden neurons S_i^H and the output neurons S_m^O are calculated using equation (6-2) as follow:

$$S_i^H = f_s(\sum_{i=1}^{N_i} w_{ji}^I S_j^I + \hat{w}_i^I) \quad j = 1, ..., N_h \tag{6-4}$$

$$S_m^O = f_s(\sum_{i=1}^{N_h} w_{im}^H S_i^H + \hat{w}_m^H) \quad m = 1, ..., N_o \tag{6-5}$$

where $\hat{w}_i^I$ and $\hat{w}_m^H$ are offset or bias weights, N_h is the number of hidden neurons and N_o is the number of output neurons. In this particular application the neural network has a single output ($N_o = 1$), and therefore (6-4) and (6-5) result in:

$$S^O = f_s(\sum_{i=1}^{N_h} w_i^H f_s(\sum_{j=1}^{N_i} w_{ji}^I S_j^O + \hat{w}_i^I) + \hat{w}^H) \tag{6-6}$$

$$S^O = g_{NN}(S_1^I, ...S_N^I) \tag{6-7}$$

For simplicity S_m^O is replaced by S^O, the weights from the hidden to the output layer w_{im}^H, $\hat{w}_m^H$ by w_i^H, $\hat{w}^H$ respectively, and the function g_{NN} is equivalent to the NN function (6-6). The optimum number N_h of the hidden layer neurons is determined experimentally.

For the adjustment of w_i^H and w_{ji}^I, EBP training algorithm is applied which minimizes the mean square error (MSE) between the NN calculated data and the measured data set.

The training data set consists of a discrete set of measured input/output data $y^{(r)} = g_s(x^{(r)})$ *(r = 1, ...,N)* which describes the behavior of the experimental system g_s. *N* is the number of available measurements.

To update the weights, a given input training data $x^{(r)}$ is presented to the inputs of the neural network:

$$S_j^I = x_j^{(r)} \qquad j = i, ..., N_i$$

The neural network output S^O is evaluated by:

$$S^O = g_{NN}(x^{(r)})$$

and the mean square error (MSE) between output training data $y^{(r)}$ and S^O is:

$$EF = \frac{1}{2}[y^{(r)} - g_{NN}(x^{(r)})]^2 \tag{6-8}$$

The gradient updating rule (EBP algorithm) is used to obtain the new values of the weights by the iterative procedure:

$$w(n+1) = w(n) + \eta \frac{\partial EF}{\partial w} \tag{6-9}$$

where η is the learning rate coefficient, *n* is the iteration index and *w* represents the weights w_i^H and w_{ij}^I. The updating terms for hidden to output weights are given by:

$$\frac{\partial EF}{\partial w_i^H} = S^O(1 - S^O)[y^{(r)} - S^O]S_i^H \tag{6-10}$$

$$\frac{\partial EF}{\partial w_{ij}^I} = S_j^H(1 - S_j^H)S^O(1 - S^O)[y^{(r)} - S^O]w_j^H(q)S_i^I \tag{6-11}$$

The same procedure is repeated for all data pairs *r* until the error function *EF* becomes sufficiently small and therefore $g_s \approx g_{NN}$. The speed of this training procedure depends on the non-linearity of the approximated function *g* and the initialization of the weights.

6.4 Principle of the approach

As mentioned in section 6.2, NNs have been used recently as fast and flexible tools for microwave modeling, simulation, and optimization. Since they are fast, accurate, flexible, and can be constructed from microwave data under different conditions, they are an excellent solution for RF and microwave design considering packaging effects [47], [48].

Despite the outstanding advantages of NNs, as the number of model input parameters increase, the amount of training data, size of NN, and training time would all increase. Increased nonlinearity in a model also requires increased training data, larger neural network size, and longer training time [127]. In this way, decreasing the number of the training data is of utmost importance.

On the other hand, design of experiment (DOE) can be used to obtain maximum information with minimal measured data and produce an experimental plan that is in some sense mathematically and statistically optimal. Watson and Gupta used DOE to decrease the number of electromagnetic simulations in electromagnetically trained artificial neural networks (EM-ANN) models for microstrip vias and interconnects in multilayer circuits [123].

A very important issue is, when ample training data are available for model development involving ANN, considerable freedom exists in the selection of model topology. However, when only limited data are available, the size of a network and the number of connections have to be carefully selected, and the NN should be appropriately trained; otherwise, it will not generalize well even when interpolating [65]. In this dissertation, to have a reliable neural model from a limited number of training data, DOE method is used to prepare the proper input training data to the NN and then the neural model is constructed with respect to minimum training error, maximum smoothness, and simplest network structure. The method is implemented for constructing a small-signal bias-dependent neural model for a p-HEMT from a limited number of training data.

Devadhaktuni, Xi, and Zhang have already introduced a neural network HBT modeling [14]. They implemented a multilayer perceptrons (MLP) type NN with 3 layers to model the HBT directly from its S-parameter data under different bias conditions. A similar model to [14] has been used in this dissertation and the only differences are in inputs and training algorithm. The MLP type NN in this work takes three inputs (frequency, drain-source voltage, and gate-source voltage) and gives 8 outputs (magnitudes and phases of S_{11}, S_{12}, S_{21}, and S_{22}). The most commonly used training algorithm of EBP, considering a smoothing term for adjusting the weights, has been used. Predictions of the neural model are tested by a new set of measured data. The results with different number of training data using this method have been compared with those of a neural model trained with a large number of training data.

6.5 Method for training and evaluation of the neural model

Huang and et al. [42] proposed a criterion, tempered modified prediction squared error (MPSE), which can be used to train and evaluate a neural model. The criterion for a single output is:

$$MPSE = TSE + \alpha^2 \sigma_0^2 \frac{k_n}{N} \tag{6-12}$$

where

$$TSE = \frac{1}{N} \sum_{i=1}^{N} (y_i - \hat{y}_i)^2 \tag{6-13}$$

is the total training squared error, α is the penalty factor in the range of 0 to 1, k_n is the number of coefficients in a network, y_i is the ith measurement which is the ith target of the output node (i = 1, 2, ..., N), $\hat{y}_i$ is the ith output of output node and the error variance of σ_0^2 is:

$$\sigma_0^2 = \frac{\sum_{i=1}^{N} (y_i - \bar{y})^2}{N} \tag{6-14}$$

where $\bar{y}$ is the mean value of all the experimental data.

Because, according to Kolmogorov's theorem [36], any continuous vector mapping of a vector variable on any compact (closed and bounded) set can be implemented exactly with a three-layered ANN, a three-layered neural model has been used. With the full connections between each pair of adjacent layers, the total number of weights in a three-layered NN, k_n, is expressed as:

$$k_n = (N_i \times N_o) N_h \tag{6-15}$$

where N_i is the number of input neurons, N_o is the number of output neurons and N_h is the number of hidden neurons. Thus for a multi output neurons the MPSE is:

$$MPSE = \frac{1}{N} \sum_{j=1}^{N_o} \sum_{i=1}^{N} (y_{i,j} - \hat{y}_{i,j})^2 + \alpha^4 \frac{(N_i + N_o) N_h}{N^2} \sum_{j=1}^{N_o} \sum_{i=1}^{N} (y_{i,j} - \frac{\sum_{i=1}^{N} y_{i,j}}{N}) \tag{6-16}$$

where $y_{i,j}$ is the jth measured output of the ith experiment and $\hat{y}_{i,j}$ is the jth estimated output of the ith experiment. By increasing the number of hidden neurons, TSE decreases exponentially but the second part of (6-16) increases linearly. Because the MPSE is the sum of the both parts, it decreases initially, but eventually the MPSE starts to increase due to the rise in the second part. The location of minimum MPSE is a function of α. In this work, α was selected between 0.4 and 0.6, so that the value of $MPSE_{min}$ decreased

neither rapidly nor very slowly, and over-fitting is avoided while the network was reasonably complicated.

To add another smoothing factor, the modified delta-learning rule proposed by Sejnowski and Rosenberg [36] has been used to provide exponential smoothing in weight adjustment. The change of weights between adjacent layers is expressed as:

$$\Delta w_{pq,l}(n+1) = (1-\beta_l)\delta_{q,l}O_{p,l} + \beta_l \Delta w_{pq,l}(n) \tag{6-17}$$

and the adjustment of the weights is done in the following manner:

$$w_{pq,l}(n+1) = w_{pq,l}(n) + \eta_l \Delta w_{pq,l}(n+1) \tag{6-18}$$

where $w_{pq,l}(n)$ is the weight from neuron p in layer l to neuron q in layer (l+1) at step n (before adjustment); $w_{pq,1}(n+1)$ is the weight from neuron p in layer l to neuron q in layer (l+1) at step (n+1) (after adjustment); $\delta_{q,l}$ is the error term of neuron q between target and actual outputs of layer l; $O_{p,l}$ is the actual output of neuron p in layer l; β_l is the smoothing factor in layer l; η_l is the learning rate in layer l.

The range of β_l is from 0 to 1. If β_l is 0, then smoothing is minimum; the entire weight adjustment comes from the newly calculated change. If β_l is 1, the new adjustment is ignored and pervious one is repeated.

An interactive approach has been used to train and evaluate a neural model as follow:

1. Select the number of training data.
2. Determine the minimum and maximum numbers of hidden layer neurons to be considered. N_t is the total number of NNs to be tested.
3. Construct the neural networks with the minimum number of neurons in the hidden layer up to maximum number of neurons in the hidden layer. Input nodes are V_{ds}, V_{gs}, frequency and a bias neuron (4 nodes). The outputs are magnitudes and phases of S-parameters (8 nodes).
4. Train the NNs considering (6-17) and (6-18).
5. Calculate the TSE, $\alpha^4 \hat{\sigma}_0^2 k$ /N, and MPSE for different networks.
6. Plot MPSE as a function of hidden neurons for different α, with discrete intervals of 0.1 ranging from 0 to 1. Plot TSE and $\alpha^4 \hat{\sigma}_0^2 k$ /N as a function of hidden layer neurons.
7. Select a neural model using two figures obtained in step 6 or use the default α between 0.3 and 0.7.

6.6 Model development and results for the GaAs-based p-HEMT on a standard test-fixture

To verify the method, crossed D-optimal design has been used to design the bias dependent S-parameters measurement. The levels for V_{ds} are 0 (0.1) 1 V and 1.5 (0.5) 5 V and for V_{gs} are -0.1 (-0.1) -0.6 V, -0.8 V, -1 V, -1.5 and -2 V. Frequency range is from 300 MHz to 40 GHz (41 measurement points). To simplify the measurement, D-optimal is only applied on V_{ds} and V_{gs}, which gives 68 experiments, and considering the frequency, the total number of measurements is 2788.

Since the networks with less than 6 hidden neurons are not able to fit to the measured data, the minimum number of hidden layer's neurons (N_h) is assumed to be 6. Fig. 6-3 shows the TSE and penalty terms ($\alpha^4 \hat{\sigma}_0^2 k/N$) while Fig. 6-4 shows MPSE as functions of N_h, and α. In this verification example, an α of 0.4 is selected which locates the MPSE_{min} at 14 neurons in the hidden layer.

Figs. 6-5 and 6-6 illustrate predictions of S-parameters by the neural model and the measured S-parameters for the bias point of V_{ds} = 0.9 V and V_{gs} = - 0.6 V which is not used as a training data (the transistor at this bias point is not in the active working region so the magnitude of S_{21} is smaller than one).

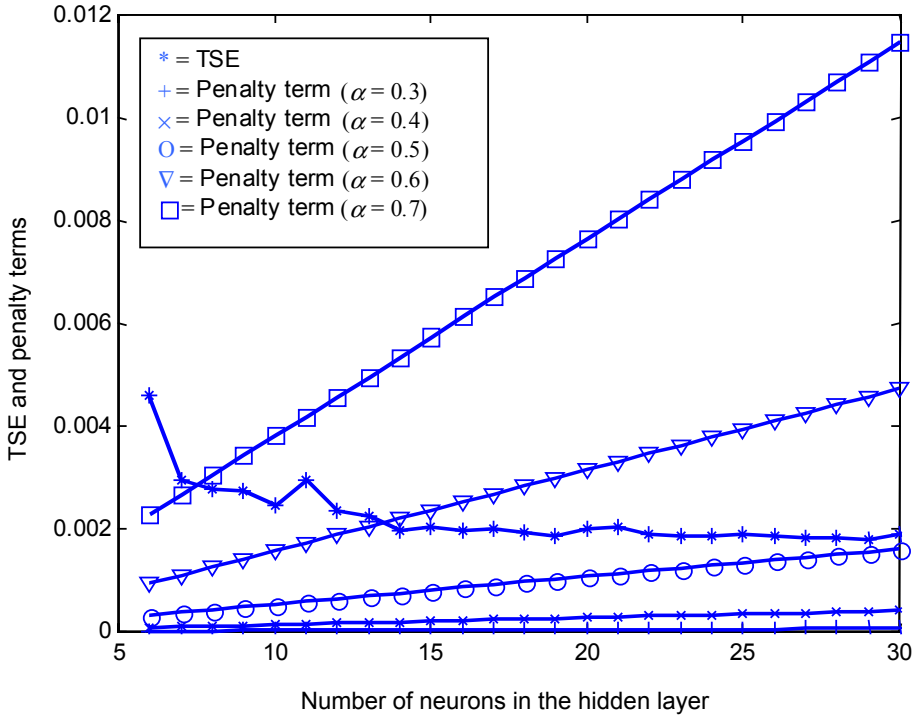


Figure 6-3: Training square error (TSE) and penalty terms against number of neurons in the hidden layer.

To compare the results, the average errors for this model and a model trained with the same method but with 24 neurons in the hidden layer are 1.46% and 1.29% for the used

training data (2788 measurement points) and 2.55% and 2.48% for all the available measured data (8200 measurement points), respectively. It means the average error related to the predictions of new data for the neural model with 14 neurons in the hidden layer is smaller.

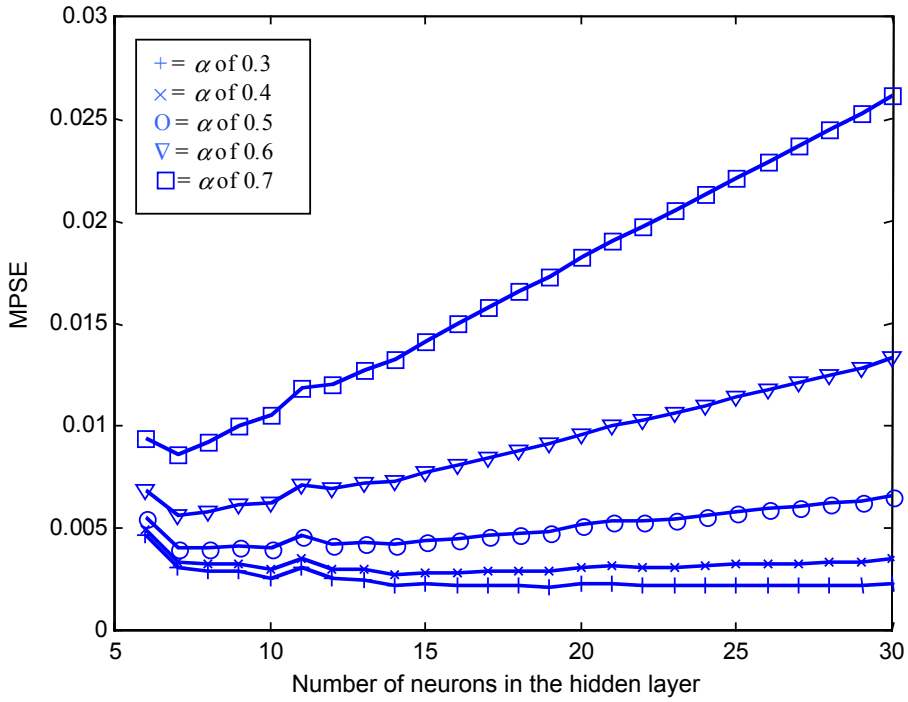


Figure 6-4: MPSE as a function of number of neurons in the hidden layer (N_h) and penalty factor (α). In this verification example α of 0.4 is selected which locates the $MPSE_{min}$ at 14 neurons in the hidden layer.

To compare this model to the standard MLP with training algorithm of EBP, all the measurements data (8200 measurements) have been used to train a neural network with 24 neurons in the hidden layer. The average error for the standard MLP network is 1.63% but as the Fig. 6-7 shows, the predictions by this neural network are not smooth and are affected by the noise.

6.7 Model development and results for the GaAs-based p-HEMT in the enhanced QMIT environment

The same approach in section 6.6 was applied for the low noise Ka-band GaAs-based p-HEMT in the enhanced QMIT environment. Crossed D-optimal design was used to design the bias dependent S-parameters measurement. The levels for V_{ds} are 0 (0.2) 3.2 V and 1.5 V and for V_{gs} are -0.2 (-0.1) -1.3 V. Frequency range is from 300 MHz to 40 GHz (41 measurement points). To simplify the measurement, D-optimal is only applied on V_{ds} and V_{gs}, which gives 68 experiments, and considering the frequency, the total number of measurements is 2788.

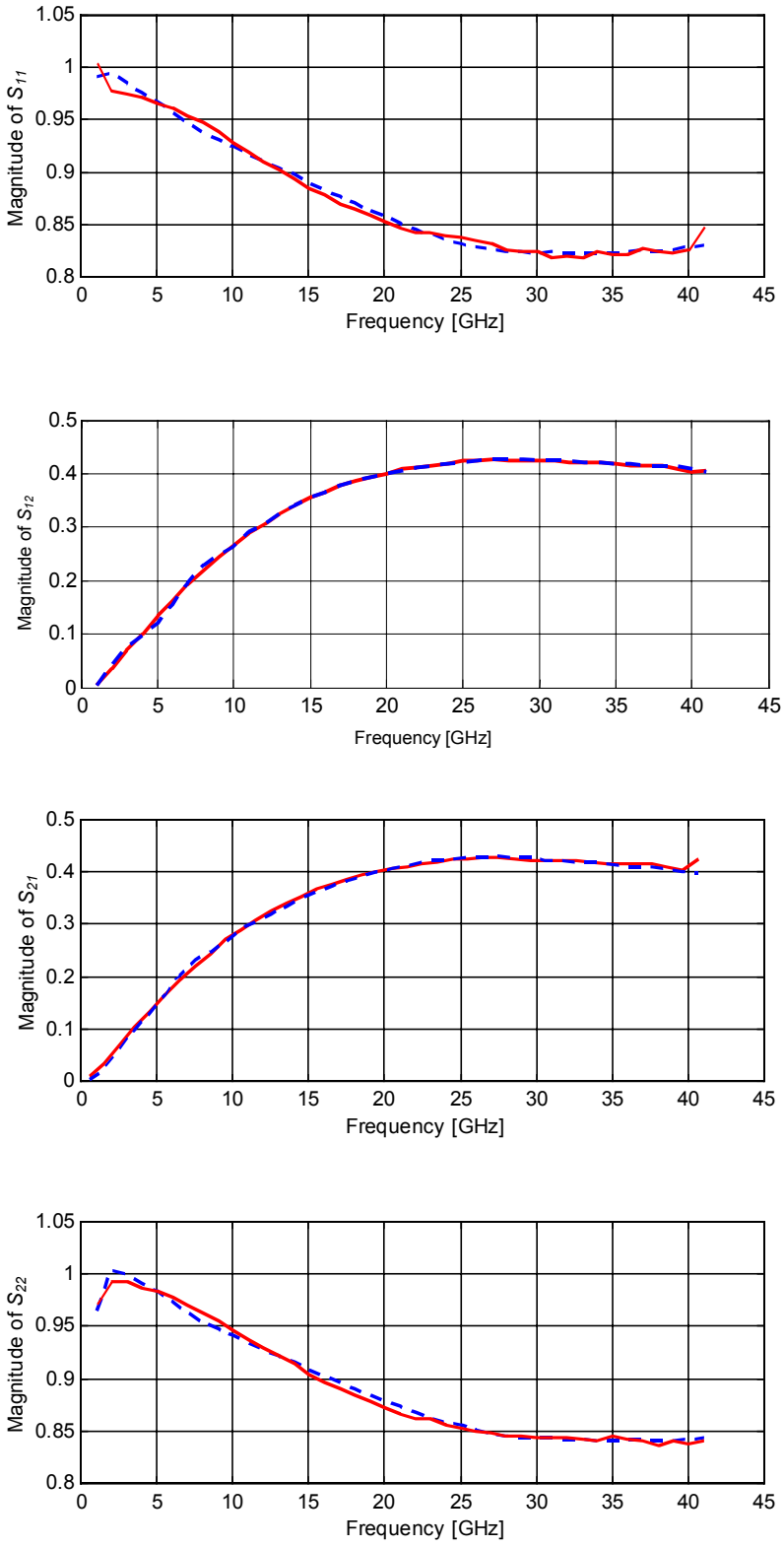


Figure 6-5: Predictions of the magnitudes of S-parameters by the neural model compared with the measurements for the low noise Ka-band GaAs-based p-HEMT on a standard test-fixture under the bias point of V_{ds} = 0.9 V and V_{gs} = - 0.6 V. Dashed-line represents the neural model results while solid-line represent measurement results. The device at this bias point is in the passive mode.

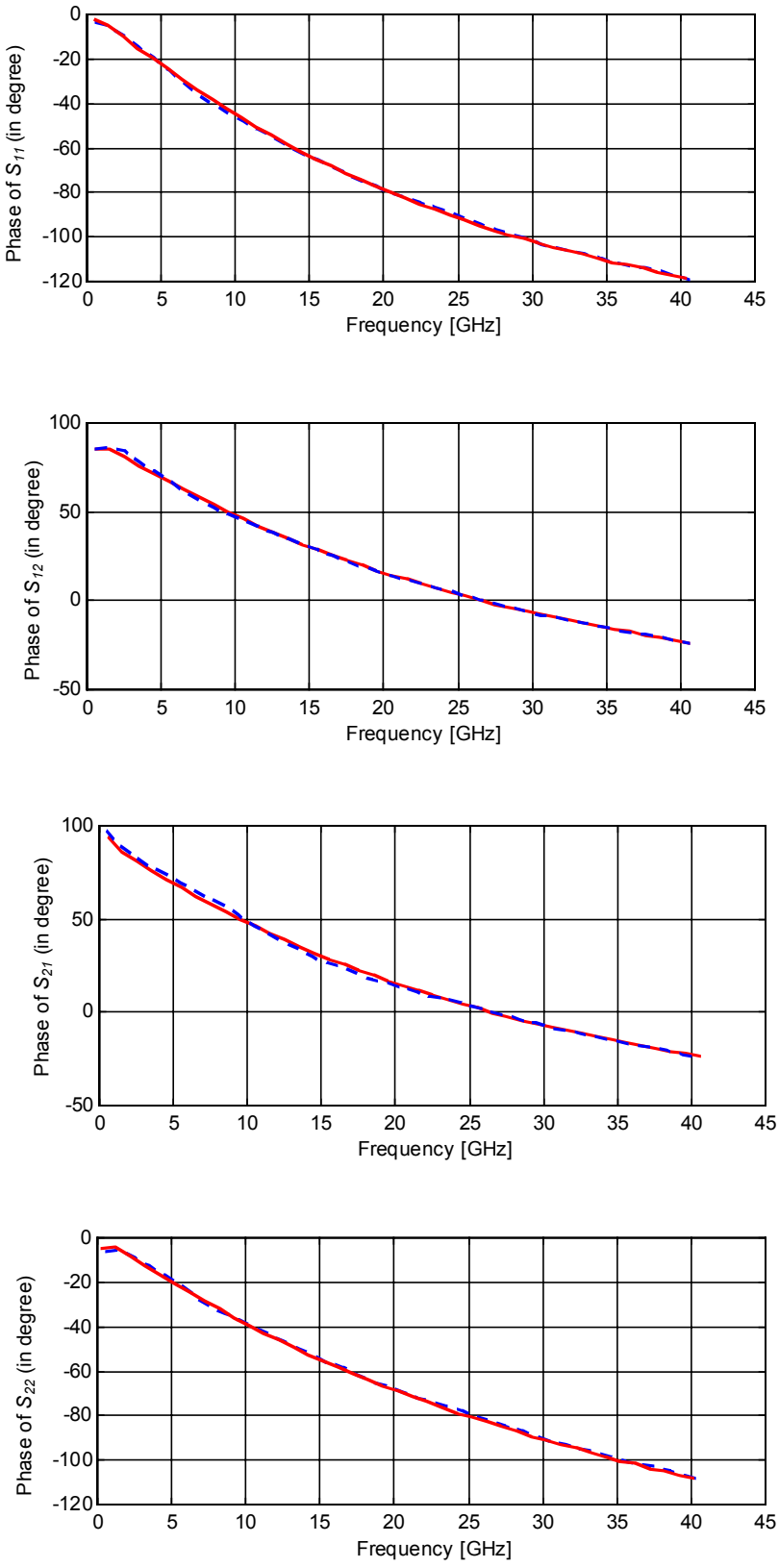


Figure 6-6: Prediction of the phase of S-parameters by the neural model compared with the measurements for the low noise Ka-band GaAs-based p-HEMT under the bias point of V_{ds} = 0.9 V and V_{gs} = - 0.6. Dashed-line represent the neural model results while solid-line represents measurement results. The device at this bias point is in the passive mode.

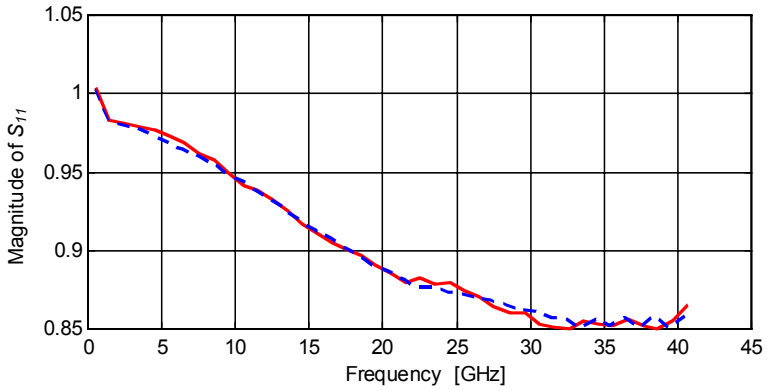


Figure 6-7: Prediction of the magnitude of S_{11} by a standard MLP type neural network with 24 neurons compared with measurement for the same test-fixture and bias point used in Figs. 6-5 and 6-6. Dashed-line represents the neural model results and solid-line represents measurement results.

Since the networks with less than 8 hidden neurons were not able to fit to the measured data, the minimum number of hidden layer's neurons (N_h) was assumed to be 8. In this verification example, an α of 0.5 is selected which locates the $MPSE_{min}$ at 16 neurons in the hidden layer.

Fig. 6-8 shows S-parameter's magnitudes predicted by the neural model and measured S-parameters magnitudes for the bias point of V_{ds} = 1.8 V and V_{gs} = -0.4 V. The average errors for this model are 1.96% for the used training data (2788 measurement points) and 3.23% for all the available measured data (8364 measurement points), respectively.

6.8 Summary

A short survey of RF/microwave/millimeterwave design is presented and the position of neural modeling in RF and microwave CAD is determined. Fundamental of MLP type NNs is described. A systematic method has been introduced to construct a reliable neural model for microwave active devices. The method aims at constructing a model considering the criteria of minimum training error, maximum smoothness and simplest NN structure. The model is implemented for low noise Ka-band GaAs-based p-HEMT of AF02N3 from Alpha Industries in two environments: on a standard test-fixture and in the enhanced QMIT structure. Although a small number of training data has been used and the neural network has a simple structure, the model gives very smooth and accurate predictions.

Because of their flexibility, accuracy and fast response, neural models are good solutions for RF, microwave and millimeterwave modeling considering packaging effects.

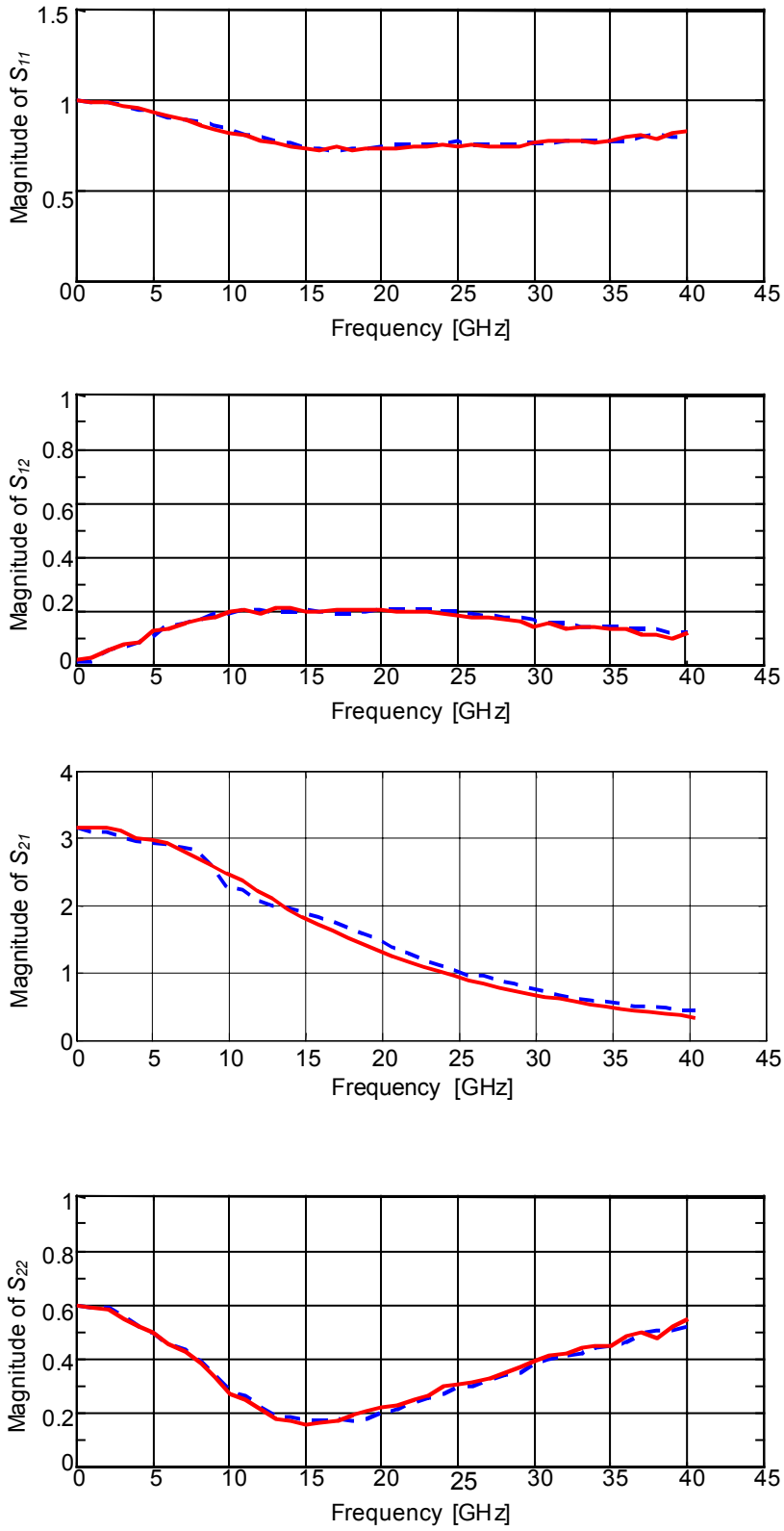


Figure 6-8: Predictions of the magnitudes of S-parameters by the neural model compared with measurements for the low noise Ka-band GaAs-based p-HEMT in the enhanced QMIT structure under the bias point of V_{ds} = 1.8 V and V_{gs} = - 0.4 V. Dashed-line represents the neural model results while solid-line represents measurement results.

Chapter 7

Conclusion and Future Prospects

7.1 Conclusion

In this dissertation, a novel technology of enhanced QMIT, for integrating III-V based microwave active devices into micomachined silicon substrates has been described. The new technology not only fulfils the requirements for high frequency design, but also is cost effective, reliable and reproducible. Two fabrication processes for coplanar and microstrip circuit realizations are introduced. To confirm the fabrication processes, the low noise Ka-band GaAs-based AFP02N3 p-HEMT and the power GaAs-based AFM08P2 MESFET from Alpha Industries were successfully integrated into a silicon substrate and the microwave characteristics of the low noise p-HEMT measured up to 40 GHz using an HP 8510B network analyzer.

Some of the advantages of the enhanced QMIT are:

- Using active devices based on different materials (Si, GaAs, InP, GaN...)
- Smaller size and weight than hybrid technology
- Better control of parasitic elements than hybrid technology
- Reproducible interconnections
- Broader bandwidth than hybrid technology
- Large area passive elements on a low cost Si-substrate
- Possible realization of high-Q passive element

- Possibility of batch processing and MCM
- Compatibility with coplanar interconnects without use of thin devices
- Higher temperature limitation of 300 °C, which is adequate for a successful realization of the passive elements
- A much lower induced thermo-mechanical stress distribution, which results in a significant improvement of the reliability and lifetime
- Elimination of air-bridges
- Direct contact of the source terminal to the ground plane, which minimizes the source inductance and improves the high frequency and high gain performance of the embedded active devices
- Possible realization of high-Q passive elements on low dielectric constant layers and low resistivity silicon substrates
- Possible fabrication of the rest of the circuit after measuring microwave parameters of the embedded transistor. This results in very accurate microwave and millimeterwave circuit designs.
- Extremely low thermal resistance, which improves lifetime of the packaging and electrical characteristics of the embedded devices.

To optimize the new structure and material properties, investigate the reliability and lifetime of the packaging and achieve an accurate model for the active devices in this technology, thermo-mechanical stress and thermal simulations and measurements in the earlier concept and enhanced QMIT and neural modeling of microwave active devices in the enhanced QMIT were performed in detail.

A novel method to achieve the thermo-mechanical stress distribution under different temperatures for the QMIT structures has been discussed. A closed-loop temperature measurement system consisting of a Pt-100 temperature sensor, a Peltier-element and a digitally controlled current source implemented allowing temperature measurements with a resolution of better than 0.1 °C. The surface profiles on the silicon substrate around the active devices have been measured using SPM, DEKTAK or white-light interferometery. Great agreement between calculated and measured results was demonstrated. In comparison with the earlier concept of QMIT, the simulation results confirm an excellent thermal resistance and a much lower induced thermo-mechanical stress for the enhanced QMIT.

The first successful application of a thermal nano-probe integrated into a piezoresistive AFM cantilever for two-dimensional thermal imaging of microwave active devices has been presented. Near-field, infrared measurement and nonlinear three-

dimensional simulation have been performed for a UHF-band power KT1305T GaAs-MESFET from OKI Electronic Components. The simulation and measurements confirm the capability of the thermal nano-probe for these applications.

Further, a systematic approach is presented to achieve a reliable neural model for microwave active devices with a different number of training data. The method is implemented for a small-signal bias dependent modeling of p-HEMT (AFP02N3 from Alpha Industries) in two different environments: on a standard test-fixture and in the enhanced QMIT. The errors for different number of training data have been compared and show that by using this method a reliable model is achievable even though the number of training data is considerably small. The method aims at constructing a model, which can satisfy the criteria of minimum training error, maximum smoothness and simplest neural network structure.

7.2 Future prospects

Many valuable and important tasks have been performed and the basis of the enhanced QMIT constructed and main critical points are solved, but as a new technology for realization of microwave and millimeterwave circuits, further research is required to provide designers with an accurate, flexible, reliable and easy to use technology.

Research in this field is broad and highly attractive. This dissertation aims at integrating devices into packages (first level packaging) but from now the research can target batch processing, MCM and higher level of packaging. All these require many efforts in the areas of design, modeling and simulation. From the technology point of view, the next steps include the fabrication of passive elements and integrating high power active devices in the substrate. GaN based devices are an extremely attractive choice for this purpose. EM modeling and simulations, heat transfer analysis and management, active device modeling and reliability studies etc. must support these activities. Some of the future research directions may include:

- Realization of passive elements and constructing a complete passive element models library in this technology
- Integration of newly developed active devices based on GaN.
- Three-dimensional packaging, batch processing and MCM in this technology
- Full wave three-dimensional EM simulations and modeling of the interconnects, discontinuities and lumped passive elements
- Electrothermal modeling and characterization of the active devices considering mechanical stress effects.
- Heat transfer analysis and management and reliability and lifetime studies.

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Curriculum vitae:

Name:	Mojtaba Joodaki
Date of Birth:	24th May, 1970
Place of Birth:	Khorram Abad Lorestan, Iran
Educations:	
Since Sept. 1999	Electrical and Electronic Engineering, Kassel University, Kassel, Germany. Pursuing Ph.D. degree in Microwave Engineering.
Sept.1997 - Sept. 1999	Electrical and Electronic Engineering, Tarbiat Modarres University, Tehran, Iran. Pursuing Ph.D. courses in Electronic Engineering.
Sept. 1994 – Aug. 1997	Electrical and Electronic Engineering, Tarbiat Modarres University, Tehran, Iran. Pursuing M.Sc. in Electronic Engineering Thesis: “Design and Fabrication of an SSL gate”.
Sept. 1989 to Aug. 1994	Electrical and Electronic Engineering, Iran University of Science and Technology, Tehran, Iran. Pursuing B.Sc. in Electronic Engineering. Final Year Project of B.Sc.: “Automatic Telephone Note-Book”.
Honours:	The highest grade for the master thesis in the dept. of electronic engineering, Tarbiat Modarres University, Tehran, Iran.
	Referee and session chairman of the First Iranian University Student Conference on Electrical Engineering, Tehran, Iran, 1998.
	German Research Community (DFG) scholarship to pursue a full time Ph.D. degree in the field of Electrical and Electronic Engineering in the dept. of High Frequency Engineering.
	Student paper award in 17th Annual IEEE Semiconductor Thermal Measurement and Management Symposium SEMI-THER XVII, CA, USA, March 2000 (travel stipend $500 and registration fee discount).
	Finalist in the Motorola/IEEE Components, Packaging, and Manufacturing Technology Society graduate fellowship of 2001 in the IEEE 51st Electronic Components & Technology Conference ECTC 51st, FL, USA, May 29 - June 1, 2001 ($1000).
	Student travel grant in the International Symposium on Optical Science and Technology (Annual Meeting of SPIE), July 29-Aug. 3, 2001 (travel stipend and registration fee discount $800).
	Winner of a Young Graduated Research Fellowship of GAAS Association in the European Microwave Week 2001, GaAs 2001, London, UK, Sept. 24-28, 2001 (€3000).

Student travel grant in the International Symposium on Optical Science and Technology (Annual Meeting of SPIE), July 2002 (travel stipend and registration fee discount $700).

Winner of F-Made Scholarship of SPIE 2002 ($4000).

Winner of a Young Graduated Research Fellowship of GAAS Association in the European Microwave Week 2002, GaAs 2002, London, UK, Sept. 2002 (€3000).